

**Advanced Vector
Extensions (AVX)
instruction set
architecture**

Advanced Vector Extensions

- Advanced Vector Extensions (AVX, also known as Sandy Bridge New Extensions) are extensions to the x86 instruction set architecture for microprocessors from Intel and AMD proposed by Intel in March 2008 and first supported by Intel with the Sandy Bridge processor shipping in Q1 2011 and later on by AMD with the Bulldozer processor shipping in Q3 2011. AVX provides new features, new instructions and a new coding scheme.

Advanced Vector Extensions

AVX uses sixteen YMM registers. Each YMM register contains:

- eight 32-bit single-precision floating point numbers or
- four 64-bit double-precision floating point numbers.

CPUs with AVX

- Intel
- Sandy Bridge processor, Q1 2011
- Sandy Bridge E processor, Q4 2011
- Ivy Bridge processor, Q1 2012
- Ivy Bridge E processor, Q3 2013
- Haswell processor, Q2 2013
- Haswell E processor, Q3 2014
- Broadwell processor, Q4 2014
- Broadwell E processor, Q2 2016
- Skylake processor, Q3 2015
- Kaby Lake processor, Q3 2016(ULV mobile)/Q1 2017(desktop/mobile)
- Coffee Lake processor, Q4 2017
- Cannonlake processor, expected in 2017
- Cascade Lake processor, expected in 2018
- Ice Lake processor, expected in 2018

Compiler and assembler support

- GCC starting with version 4.6 (although there was a 4.3 branch with certain support) and the Intel Compiler Suite starting with version 11.1 support AVX. The Visual Studio 2010/2012 compiler supports AVX via intrinsic and /arch:AVX switch. The Open64 compiler version 4.5.1 supports AVX with -mavx flag. Absoft supports with -mavx flag. PathScale supports via the -mavx flag. The Free Pascal compiler supports AVX and AVX2 with the -CfAVX and -CfAVX2 switches from version 2.7.1. The Vector Pascal compiler supports AVX via the -cpuAVX32 flag.

Operating system support

- AVX adds new register-state through the 256-bit wide YMM register file, so explicit operating system support is required to properly save and restore AVX's expanded registers between context switches. The following operating system versions support AVX:

Operating system support

- Apple OS X: Support for AVX added in 10.6.8 (Snow Leopard) update released on June 23, 2011.
- DragonFly BSD added support in early 2013.
- FreeBSD in a patch submitted on 21 January 2012, which was included in the 9.1 stable release
- Linux: supported since kernel version 2.6.30, released on June 9, 2009.
- OpenBSD added support on 21 March 2015.
- Solaris 10 Update 10 and Solaris 11
- Windows: supported in Windows 7 SP1 and Windows Server 2008 R2 SP1, Windows 8, Windows 10
- Windows Server 2008 R2 SP1 with Hyper-V requires a hotfix to support AMD AVX (Opteron 6200 and 4200 series) processors, KB2568088

Advanced Vector Extensions 2

- Advanced Vector Extensions 2 (AVX2), also known as Haswell New Instructions, is an expansion of the AVX instruction set introduced in Intel's Haswell microarchitecture. AVX2 makes the following additions:

Advanced Vector Extensions 2

- expansion of most vector integer SSE and AVX instructions to 256 bits
- three-operand general-purpose bit manipulation and multiply
- Gather support, enabling vector elements to be loaded from non-contiguous memory locations
- DWORD- and QWORD-granularity any-to-any permutes
- vector shifts.

CPUs with AVX2

- Intel
- Haswell processor, Q2 2013
- Haswell E processor, Q3 2014
- Broadwell processor, Q4 2014
- Broadwell E processor, Q3 2016
- Skylake processor, Q3 2015
- Kaby Lake processor, Q3 2016(ULV mobile)/Q1 2017(desktop/mobile)
- Coffee Lake processor, Q4 2017
- Cannonlake processor, expected in 2018
- Cascade Lake processor, expected in 2018
- Ice Lake processor, expected in 2018
- AMD
- Excavator processor, Q2 2015
- Zen processor, Q1 2017

AVX-512

- AVX-512 are 512-bit extensions to the 256-bit Advanced Vector Extensions SIMD instructions for x86 instruction set architecture proposed by Intel in July 2013, and scheduled to be supported in 2015 with Intel's Knights Landing processor.

AVX-512

- The amount of electricity used by the computer. This becomes especially important for systems with limited power sources such as solar, batteries, human power.

CPUs with AVX-512

- Xeon Phi x200 (aka Knights Landing, 2016)
- Skylake EP/EX Xeon "Purley" (Xeon E5-26xx V5) processors (expected in H2 2017)
- Cannonlake processors (expected in 2018)

Compilers supporting AVX-512

- GCC 4.9 and newer
- Clang 3.9 and newer
- ICC 15.0.1 and newer
- Microsoft Visual Studio 2017 C++ Compiler
- Java 9

Applications

- Suitable for floating point-intensive calculations in multimedia, scientific and financial applications (AVX2 adds support for integer operations).
- Increases parallelism and throughput in floating point SIMD calculations.
- Reduces register load due to the non-destructive instructions.
- Improves Linux RAID software performance (required AVX2, AVX is not sufficient)

Software

- Blender uses *AVX2* in the render engine cycles.
- OpenSSL uses *AVX* and *AVX2* optimized cryptographic functions since version 1.0.2.
- Prime95/MPrime, the software used for GIMPS, started using the *AVX* instructions since version 27.x.
- dnetc, the software used by distributed.net, has an *AVX2* core available for its RC5 project and will soon release one for its OGR-28 project.
- Einstein@Home uses *AVX* in some of their distributed applications that search for gravitational waves.