A large, circular, blue-tinted image of a microchip die, showing a grid of circuitry, is positioned on the right side of the slide.

Мікропроцесорна техніка (лекція 2) Благітко Б.Я. 2018 р.

PSoC Designer 5.4
Designing with PSoC

PSoC's Routing Resources

Цифрова частина системи

Digital PSoC Blocks

- Counter
 - PWM
 - Timer

PWMs, Timers and Counters

- PWMs, Timers and Counters share many capabilities but each provides specific capabilities.

- **When to Use a PWM**

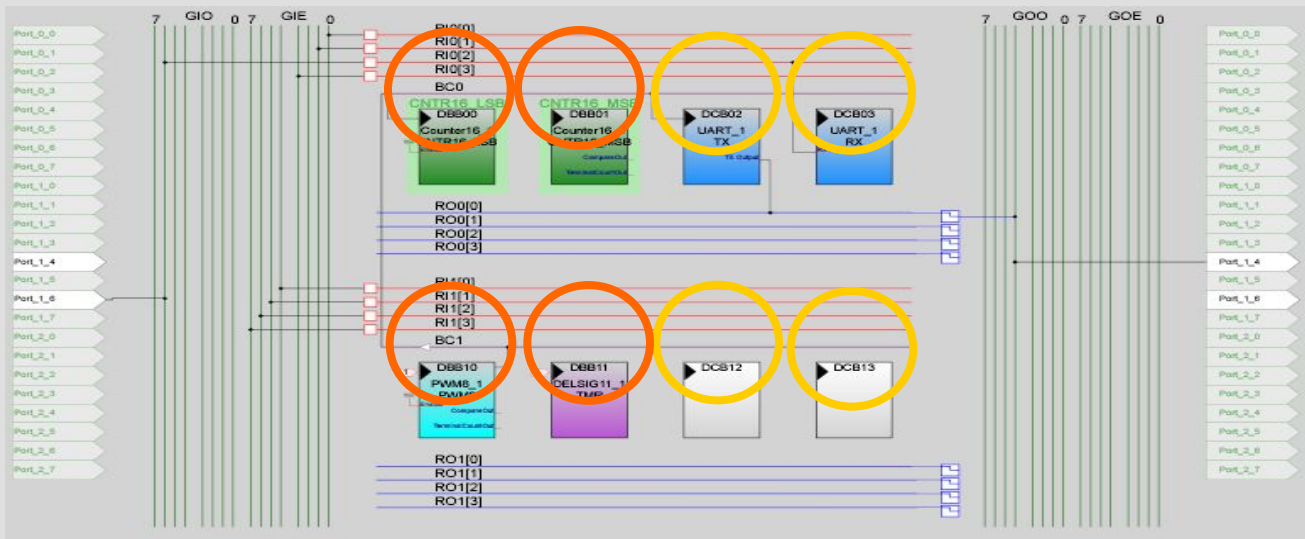
- The most common use of the **PWM** is to generate periodic waveforms with adjustable duty cycles. The PWM also provides optimized features for power control, motor control, switching regulators and lighting control. The PWM can also be used as a clock divider by driving a clock into the clock input and using the terminal count or a PWM output as the divided clock output.

PWMs, Timers and Counters

- **When to Use a Counter**
 - A **Counter** component is better used in situations that require the counting of a number of events but also provides rising edge capture input as well as a compare output.
 - **When to Use a Timer**
 - A **Timer** component is better used in situations focused on timing the length of events, measuring the interval of multiple rising and/or falling edges, or for multiple capture events.

Цифрові блоки

- Multiple Rows of Digital Blocks*
- Each Row Contains:
 - Two Digital Basic Blocks (DBB)
 - Two Digital Communication Blocks (DCB)

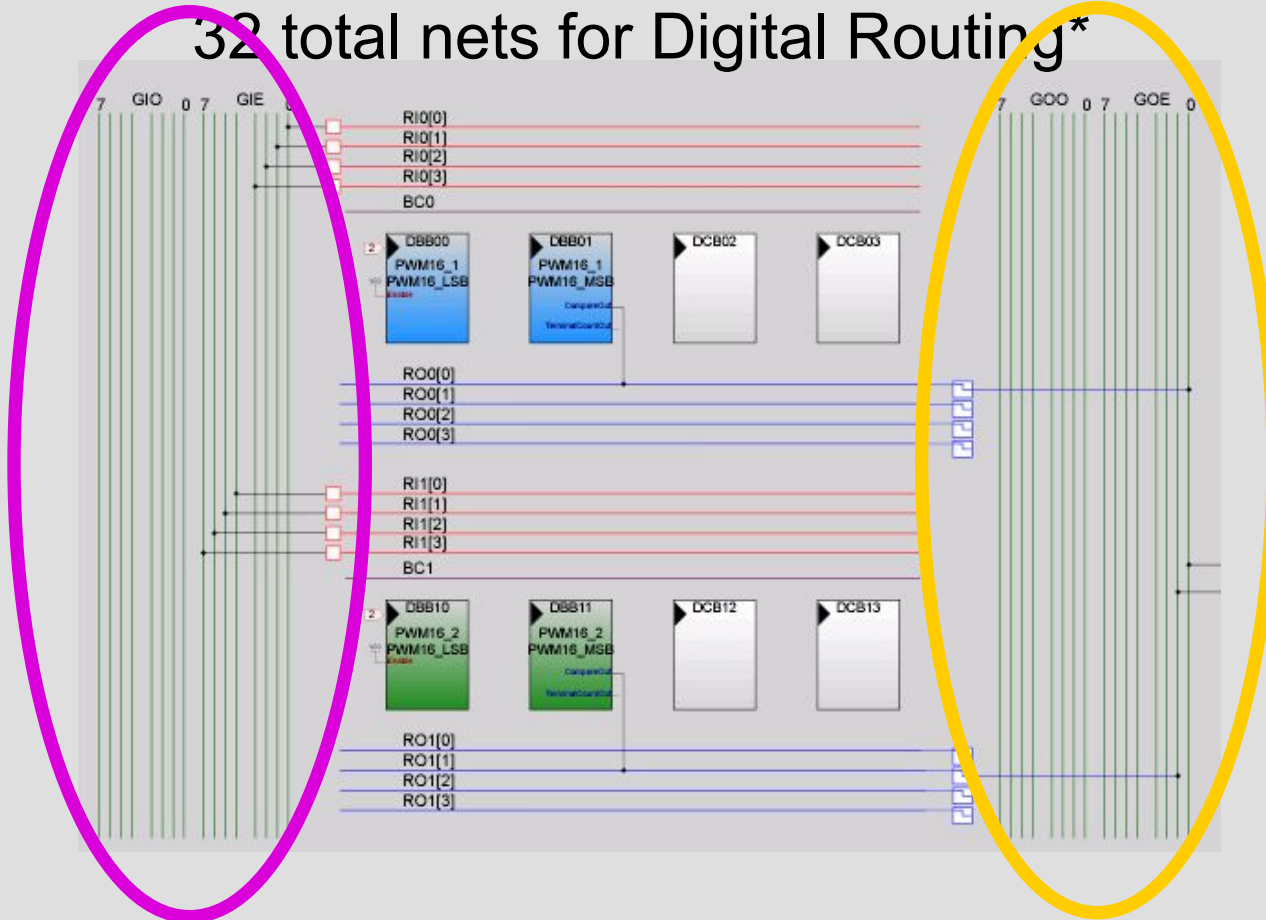


*Number of rows depends on the family

Global Digital Interconnect

32 total nets for Digital Routing*

16
Окремих
загальних
ВХОДІВ*



16
Окремих
загальних
ВИХОДІВ*

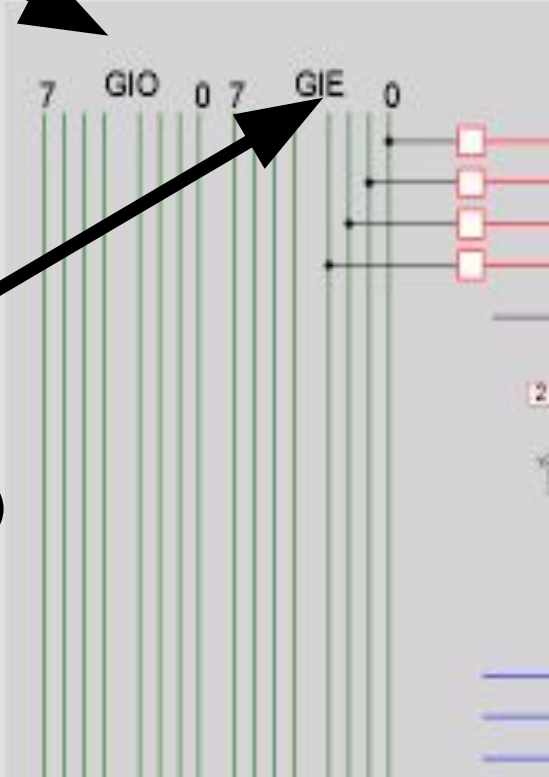
*Depends on the PSoC family

Global Digital Interconnect

Окремі загальні входи/ виходи
поділяються на парні та непарні

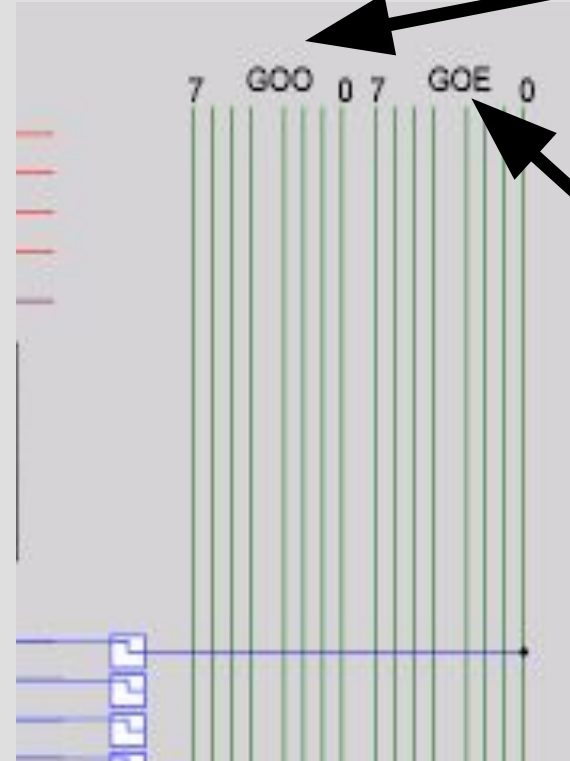
GIO =
Окремі
загальні
входи
(парні)

GIE =
Окремі
загальні
входи
(непарні)



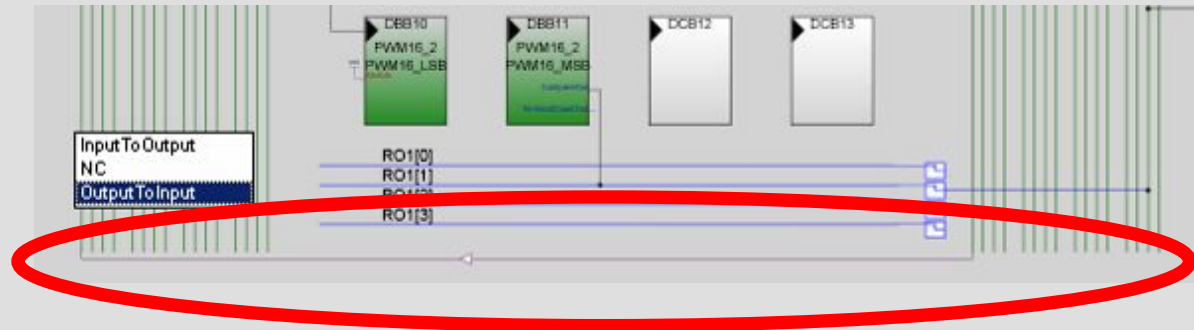
GOO =
Окремі
загальні
виходи
(парні)

GOE =
Окремі
загальні
виходи
(непарні)

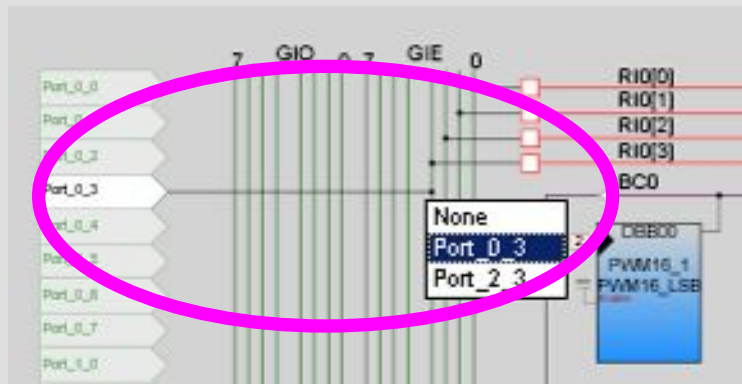


Global Digital Interconnect

- Global nets can be used to:
 - Під'єднання до інших Global nets
 - Під'єднання до Pins



Вхід:

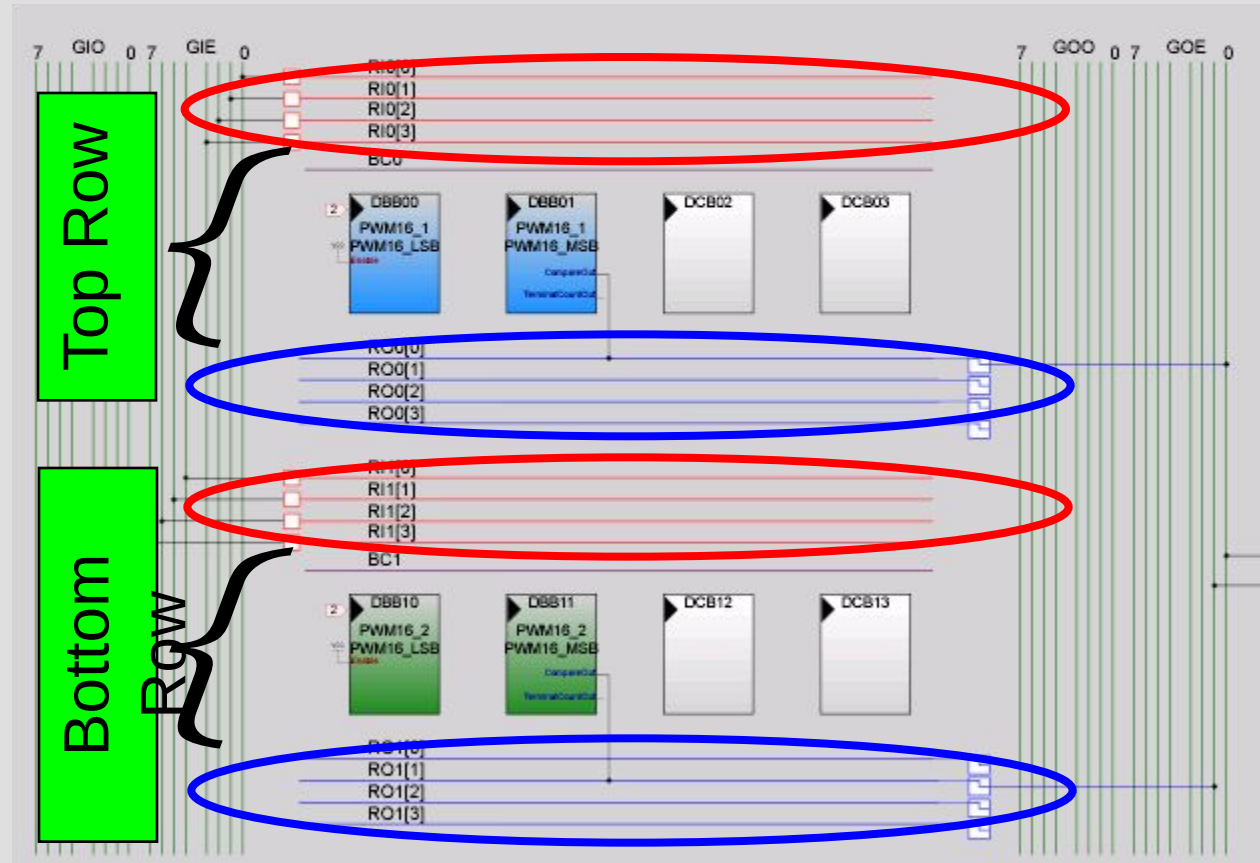


Вихід:



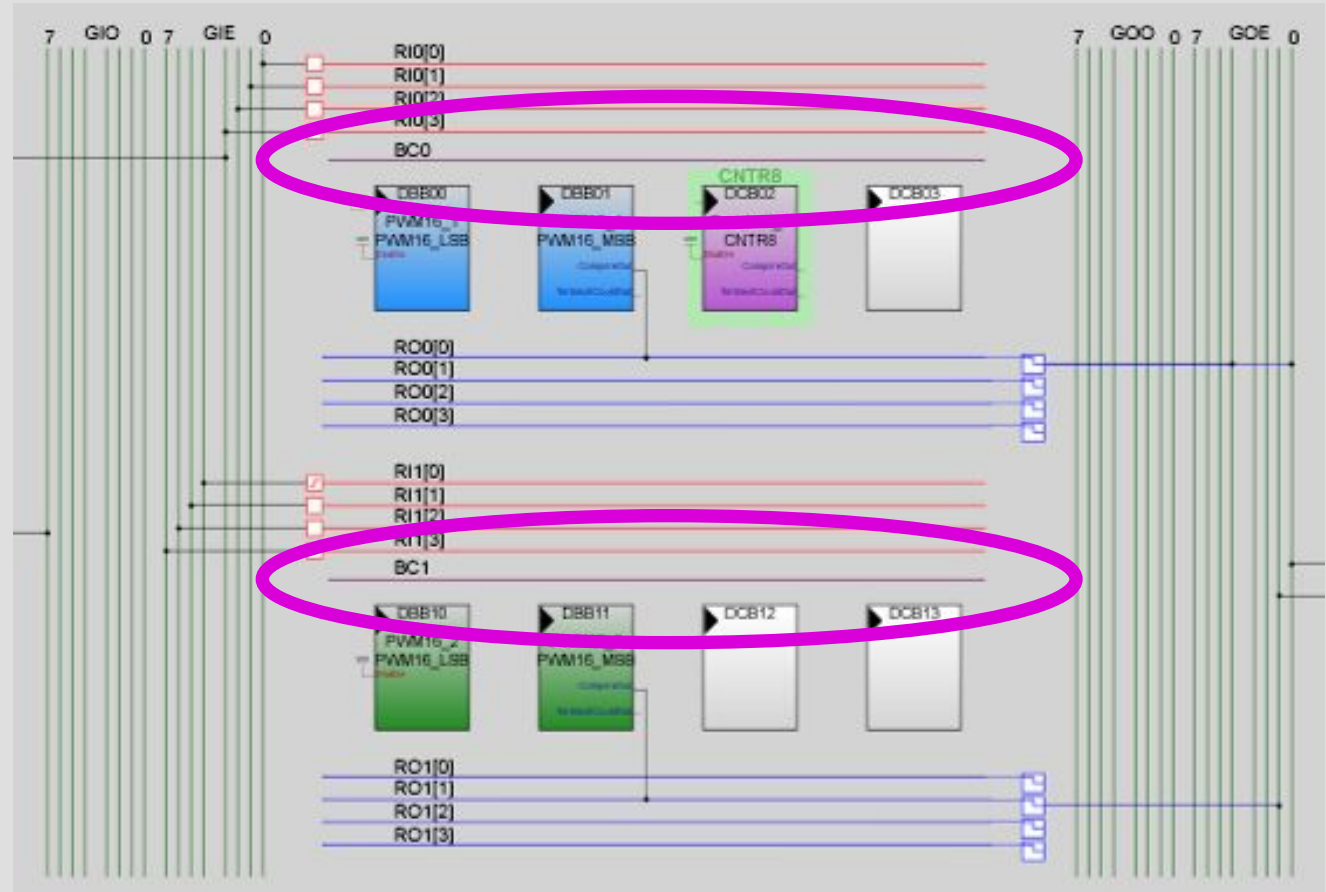
Row Digital Interconnect

- Each row of Digital Blocks has its own set of Row Interconnects
- 4 Input Rows and
- 4 Output Rows for the top row of digital blocks
- 4 Input Rows and
- 4 Output Rows for the bottom row of digital blocks



Row Broadcast Nets for Digital Signals

For every digital block row, there is one Row Broadcast Net



Global Resources

Global Resources	
Power Setting [\	5.0V / 24MHz
CPU_Clock	SysClk/1
32K_Select	Internal
PLL_Mode	Disable
Sleep_Timer	512_Hz
VC1= SysClk/N	3
VC2= VC1/N	16
VC3 Source	VC2
VC3 Divider	256
SysClk Source	Internal
SysClk*2 Disable	No
Analog Power	SC On/Ref Low
Ref Mux	[Vdd/2]+/-BandGap
AGndBypass	Disable
Op-Amp Bias	Low
A_Buff_Power	Low
SwitchModePurr	OFF
Trip Voltage [LVI	4.81V (5.00V)
LVDThrottleBack	Disable
Watchdog Enab	Disable

Power Setting [Vcc / SysClk freq]

Module Objectives

At the end of this module, you should be able to:

- List the three types of PSoC datasheets
- Give examples of when to use each type of datasheet
- Describe the process of routing user modules out to pins
- Outline the various design considerations of using PSoC

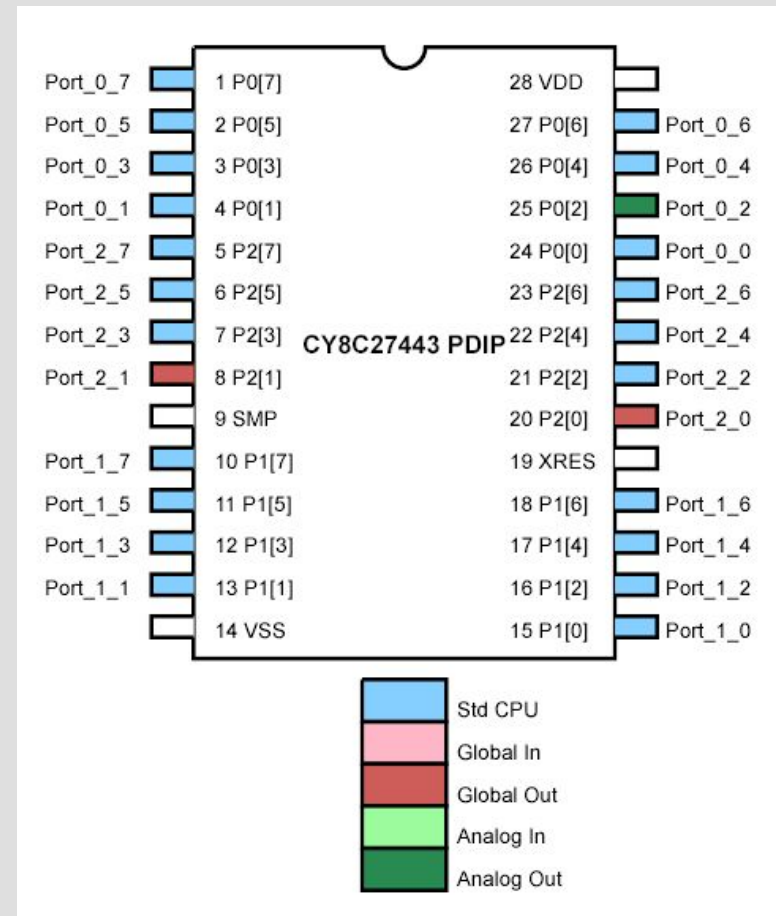
User Module Datasheets

Each user module has its own datasheet contained within the PSoC Designer software

- User module block diagrams
- Detailed user module specifications
- Placement considerations
- Example code

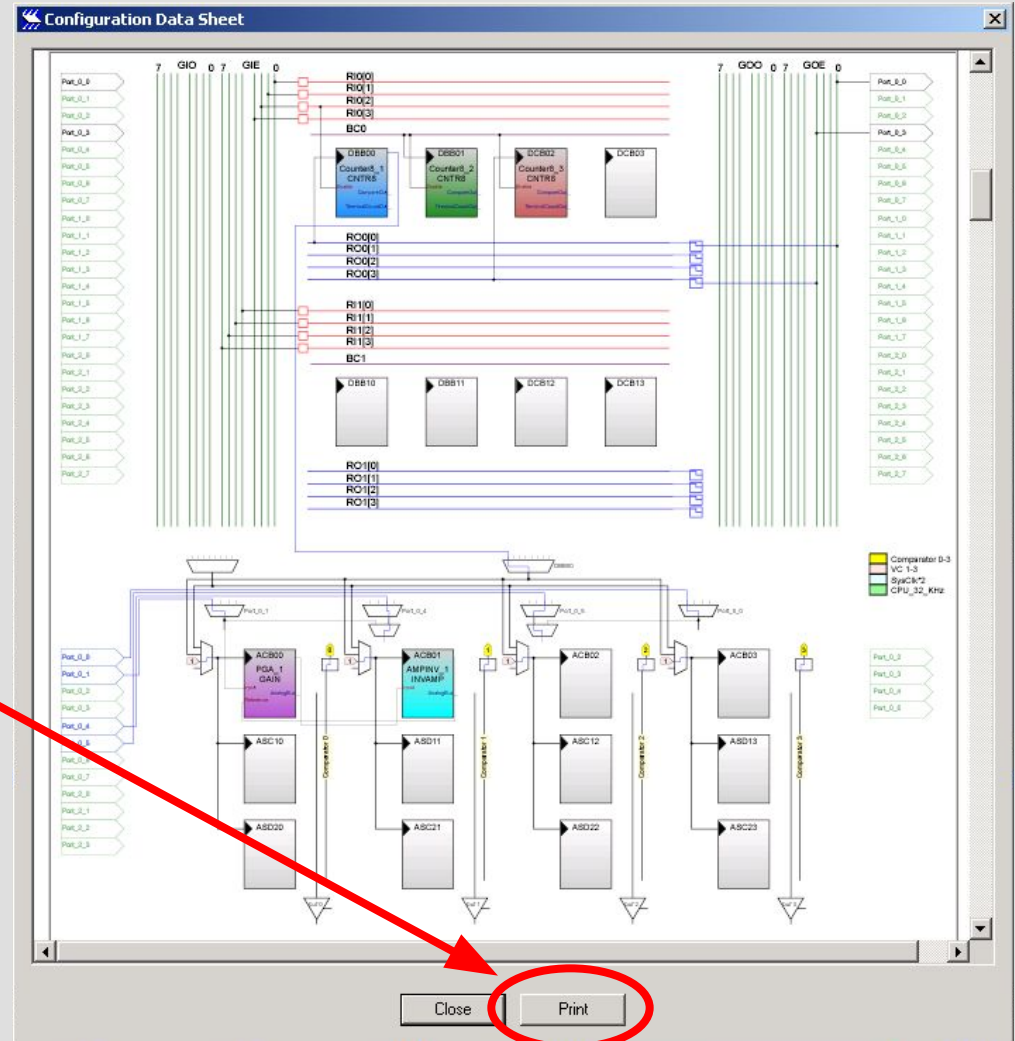
PSoC Project Configuration Datasheet

- User-defined pin outs are color-coded and detailed in the project configuration datasheet.

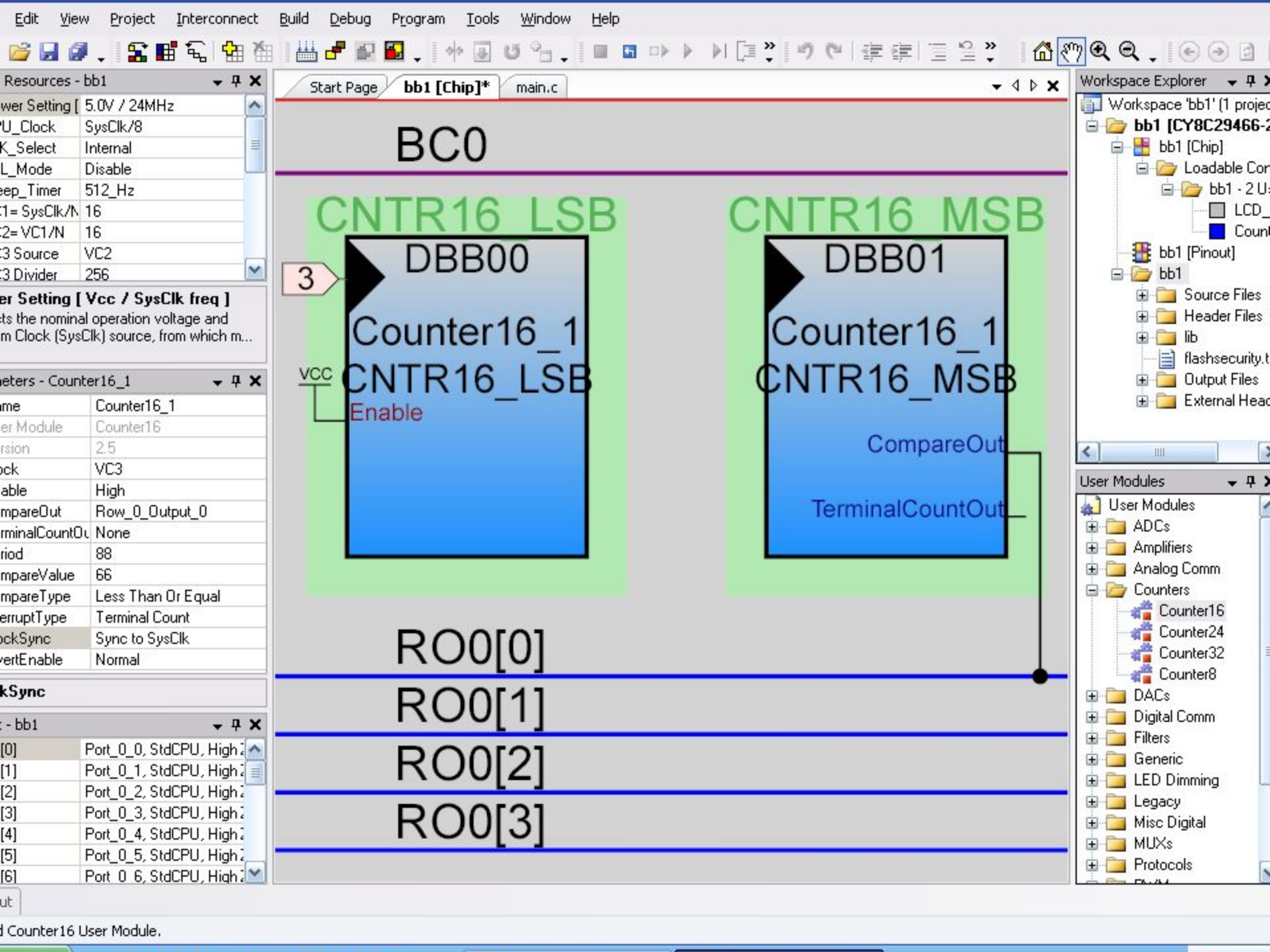


PSoC Project Configuration Datasheet

- Project configuration datasheets also contain the placement and routing of user modules
- Project configuration datasheets are printable with the click of a button



Секція 1: Counters



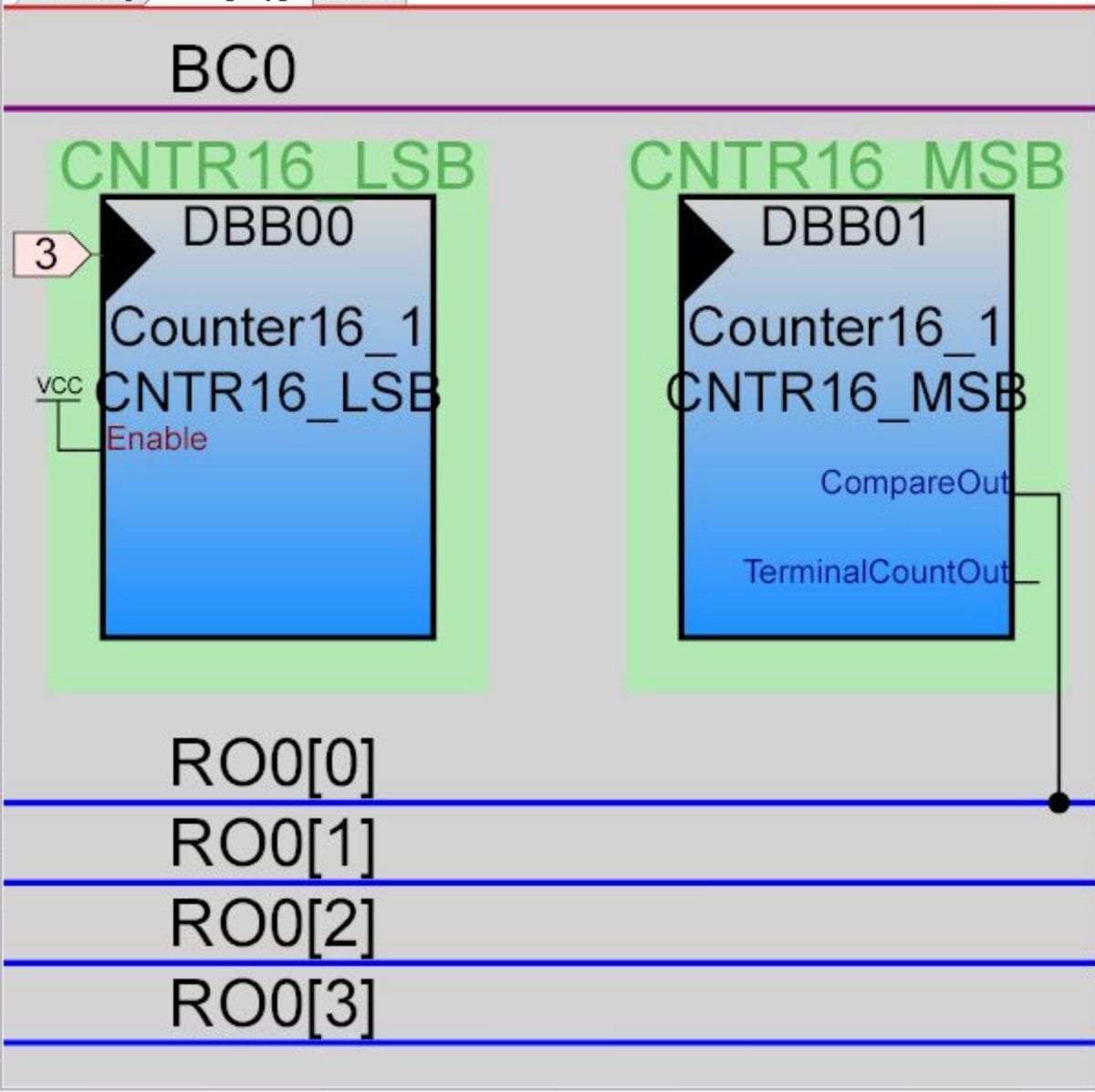
Power Setting [5.0V / 24MHz

PU_Clock	SysClk/8
K_Select	Internal
L_Mode	Disable
Keep_Timer	512_Hz
VC1= SysClk/N	16
VC2= VC1/N	16
VC3 Source	VC2
VC3 Divider	256

Power Setting [Vcc / SysClk freq]
 Sets the nominal operation voltage and
 the system Clock (SysClk) source, from which m...

Name	Counter16_1
User Module	Counter16
Version	2.5
Block	VC3
Mode	High
CompareOut	Row_0_Output_0
TerminalCountOut	None
Period	88
CompareValue	66
CompareType	Less Than Or Equal
InterruptType	Terminal Count
BlockSync	Sync to SysClk
InvertEnable	Normal

[0]	Port_0_0, StdCPU, HighZ
[1]	Port_0_1, StdCPU, HighZ
[2]	Port_0_2, StdCPU, HighZ
[3]	Port_0_3, StdCPU, HighZ
[4]	Port_0_4, StdCPU, HighZ
[5]	Port_0_5, StdCPU, HighZ
[6]	Port_0_6, StdCPU, HighZ



Workspace 'bb1' (1 project)

- bb1 [CY8C29466-2]
 - Loadable Components
 - bb1 - 2 User Modules
 - LCD Controller
 - Counter16
 - bb1 [Pinout]
 - bb1
 - Source Files
 - Header Files
 - lib
 - flashsecurity.t
 - Output Files
 - External Headers

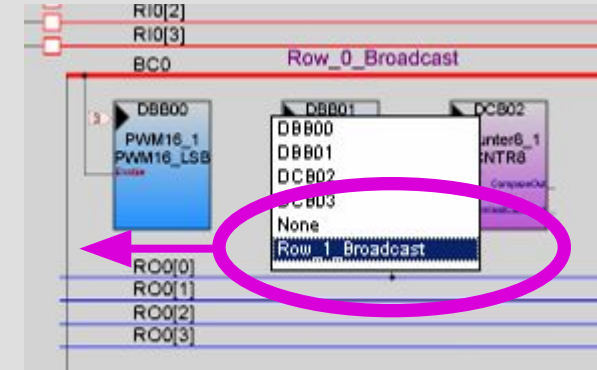
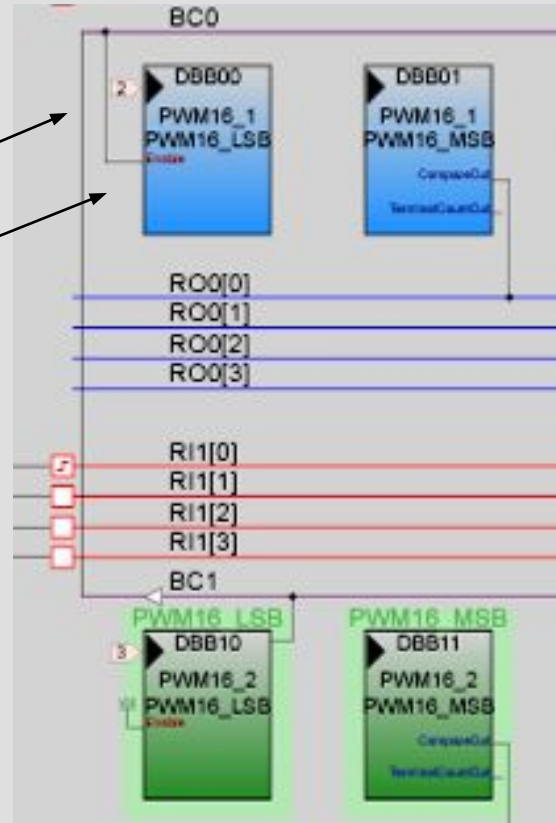
- User Modules
 - ADCs
 - Amplifiers
 - Analog Comm
 - Counters
 - Counter16
 - Counter24
 - Counter32
 - Counter8
 - DACs
 - Digital Comm
 - Filters
 - Generic
 - LED Dimming
 - Legacy
 - Misc Digital
 - MUXs
 - Protocols

Properties Counter

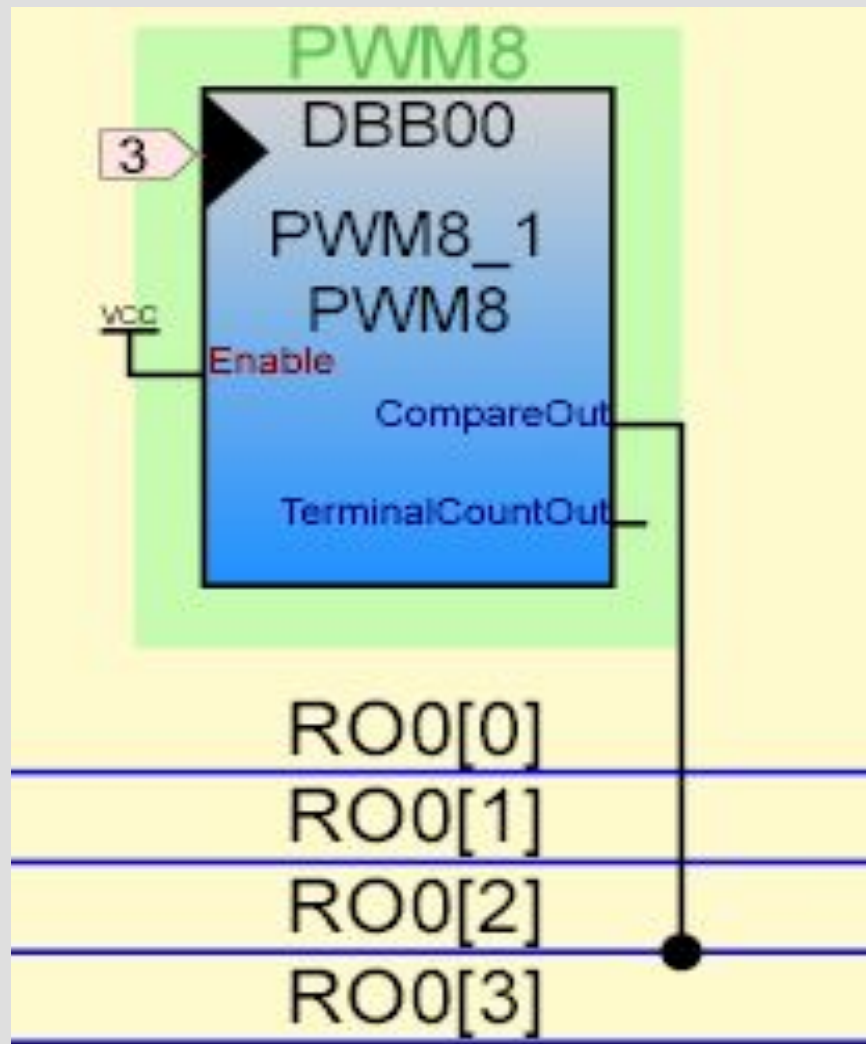
Properties - LEDFlashTimer	
Name	LEDFlashTimer
User Module	Timer8
Version	2.5
Clock	VC3
Capture	Low
TerminalCountOut	Row_0_Output_2
CompareOut	None
Period	255
CompareValue	0
CompareType	Less Than
InterruptType	Terminal Count
ClockSync	Sync to SysClk
TC_PulseWidth	Full Clock
InvertCapture	Normal

Row Broadcast Nets for Digital Signals

- Row Broadcast Nets can be connected to
 - Each other
 - A digital block
- Thus, any digital block can drive any other digital block or blocks



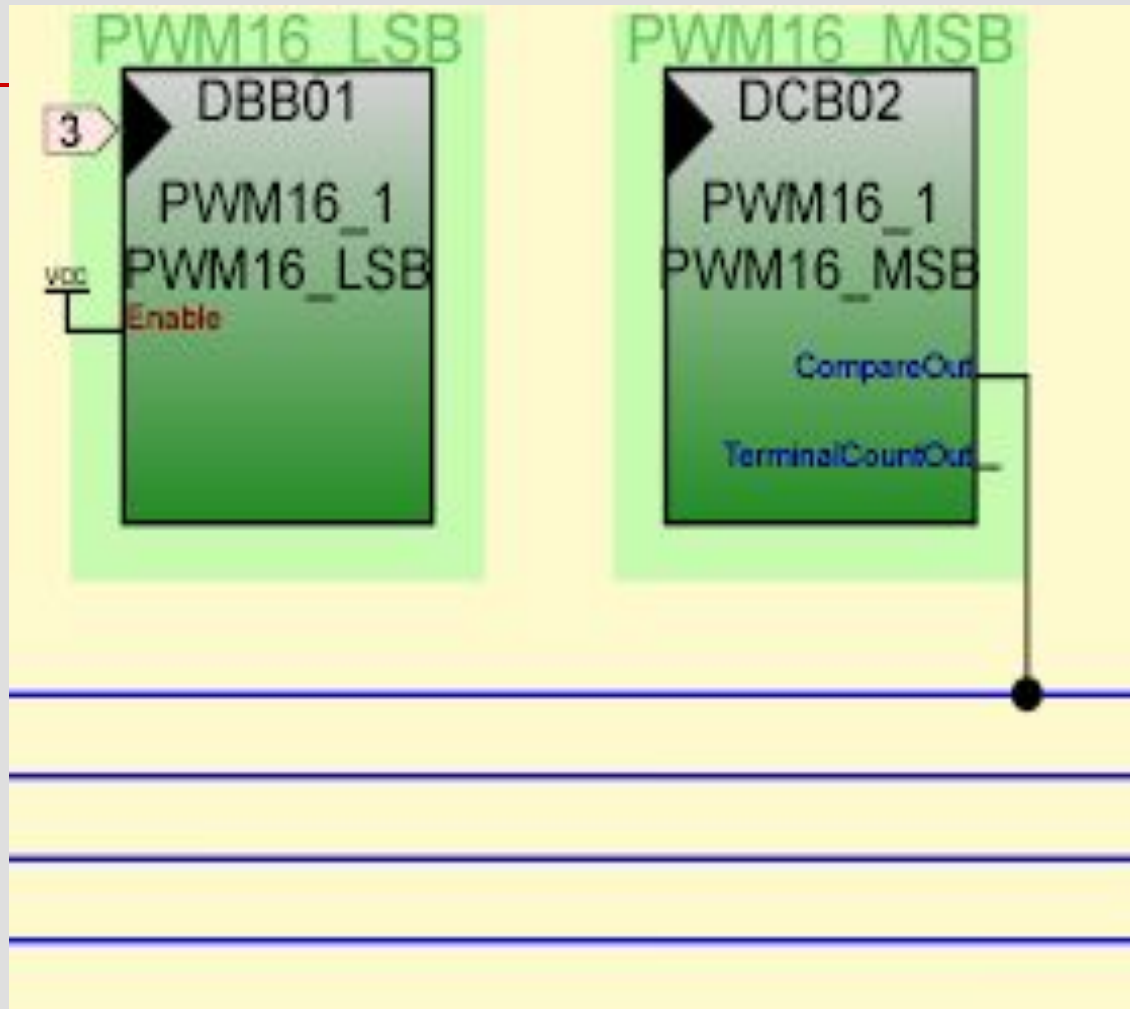
Секція 2: PWM



Properties PWM

Name	PWM8_1
User Module	PWM8
Version	2.60
Clock	VC3
Enable	High
CompareOut	Row_0_Output_2
TerminalCountOut	None
Period	255
PulseWidth	125
CompareType	Less Than Or Equal
InterruptType	Terminal Count
ClockSync	Sync to SysClk
InvertEnable	Normal

InvertEnable



Properties PWM

Parameters - PWM16_1	
Name	PWM16_1
User Module	PWM16
Version	2.5
Clock	VC3
Enable	High
CompareOut	Row_0_Output_0
TerminalCountOut	None
Period	1024
PulseWidth	600
CompareType	Less Than Or Equal
InterruptType	Terminal Count
ClockSync	Sync to SysClk <input type="button" value="v"/>
InvertEnable	Normal

ClockSync

Секція 3: TIMER



Resources - bb1

Power Setting	5.0V / 24MHz
PU_Clock	SysClk/8
K_Select	Internal
L_Mode	Disable
Keep_Timer	512_Hz
VC1= SysClk/N	16
VC2= VC1/N	16
VC3 Source	VC2
VC3 Divider	256

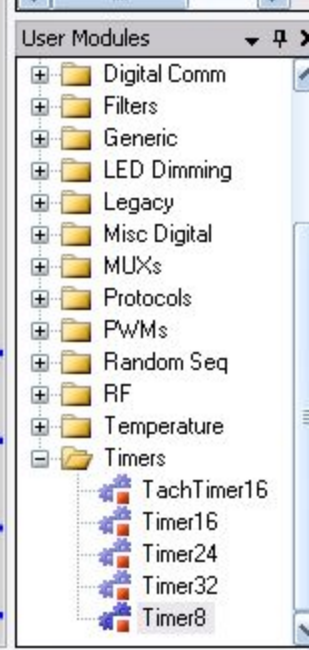
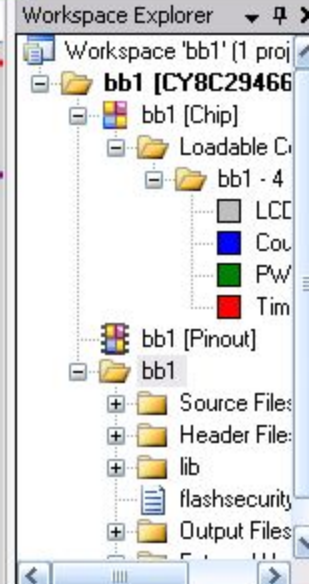
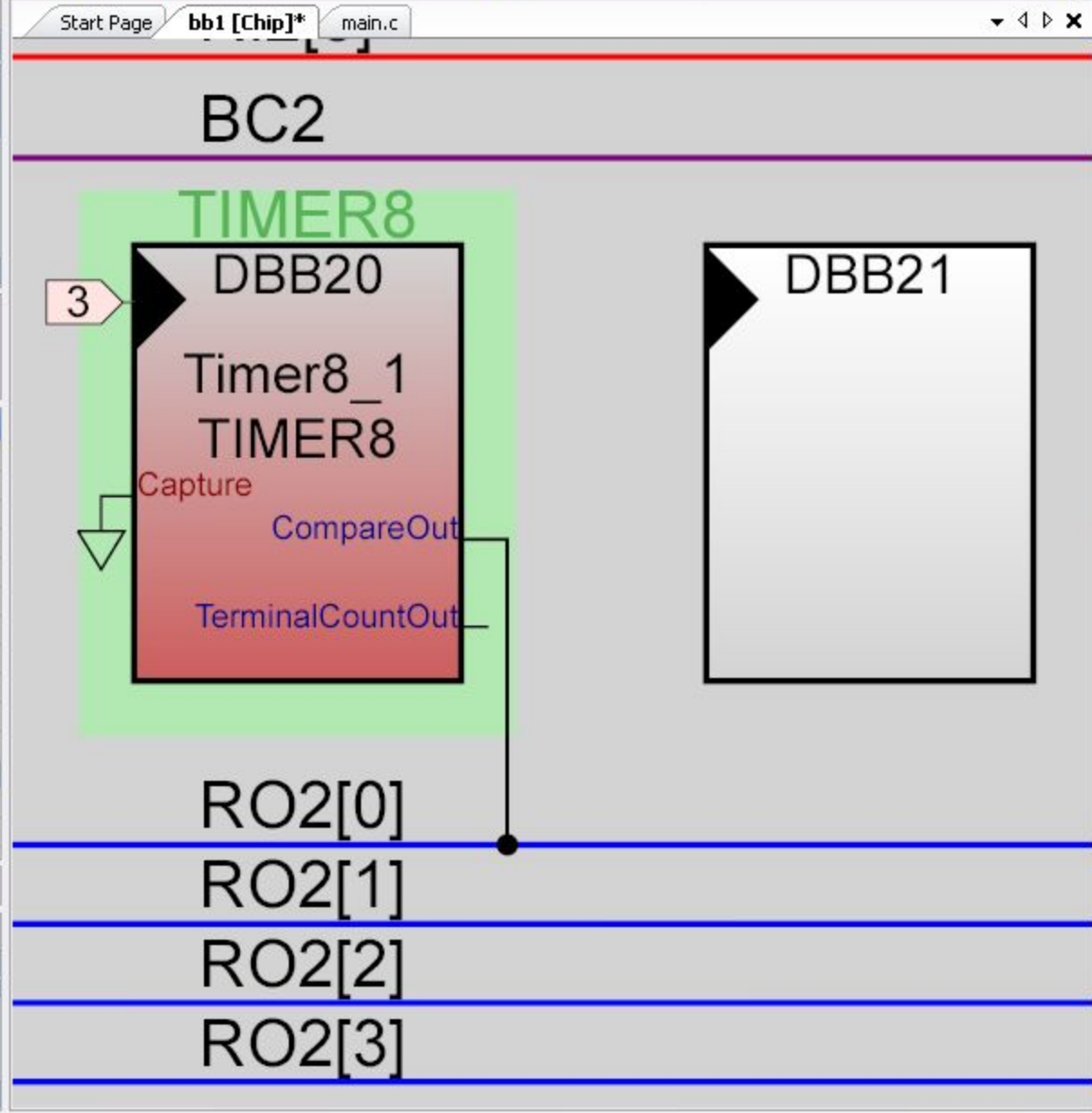
Power Setting [Vcc / SysClk freq]
sets the nominal operation voltage and
system Clock (SysClk) source, from which m...

Parameters - Timer8_1

Name	Timer8_1
Timer Module	Timer8
Version	2.70
Block	VC3
Capture	Low
TerminalCountOut	None
CompareOut	Row_2_Output_0
Period	87
CompareValue	45
CompareType	Less Than Or Equal
InterruptType	Terminal Count
BlockSync	Sync to SysClk
ComparePulseWidth	Full Clock
InterruptCapture	Normal

BlockSync

Port	bb1
[0]	Port_0_0, StdCPU, High
[1]	Port_0_1, StdCPU, High
[2]	Port_0_2, StdCPU, High
[3]	Port_0_3, StdCPU, High
[4]	Port_0_4, StdCPU, High
[5]	Port_0_5, StdCPU, High



Properties Timer8

Properties - LEDFlashTimer	
Name	LEDFlashTimer
User Module	Timer8
Version	2.5
Clock	VC3
Capture	Low
TerminalCountOut	Row_0_Output_2
CompareOut	None
Period	255
CompareValue	0
CompareType	Less Than
InterruptType	Terminal Count
ClockSync	Sync to SysClk
TC_PulseWidth	Full Clock
InvertCapture	Normal

The 8-bit timer is used to flash the LED periodically. It uses the interrupt generated by the timer to toggle the LED.

- 1. Place a **Timer8** user module and rename it *LEDFlashTimer*.
- 2. Set the **Clock** to **VC3**.
- 3. Set **Capture** to **Low**.
- 4. Set **TerminalCountOut** to **Row_0_Output_2**.
- You'll route the Terminal Count output to a pin so you can get some practice routing resources in PSoC Designer. You will connect the pin to an LED and set the Drive mode on the pin so that it will flash the LED for a single clock cycle every time the timer reaches terminal count.
- 5. Set **CompareOut** to **None**.
- 6. Set the **Period** to **250**.

The 8-bit timer is used to flash the LED periodically. It uses the interrupt generated by the timer to toggle the LED.

- 7. Set the **CompareValue** to **0**.
- 8. Set the **CompareType** to **Less Than**.
- 9. Set the **InterruptType** to **Terminal Count**.
- 10. Set **ClockSync** to **Sync to SysClk**.

The 8-bit timer is used to flash the LED periodically. It uses the interrupt generated by the timer to toggle the LED.

- The flash rate of the LED will be 1/4 second.
(24 Mhz \div 3 (VC1) \div 16 (VC2) \div 250 (VC3 Divider) \div 250 (Period)) The timer will hit terminal count 8 times per second and each of these terminal counts toggles the LED.

Мікропроцесорна техніка (лекція 2, кінець) Благітко Б.Я. 2018р.

PSoC Designer 5.4
Designing with PSoC

