MICROELECTRONIC FRONT-END of RECEIVERS for WIRELESS SYSTEMS

(микроэлектронная реализация интерфейсной части радиоприемных систем)

Prof. Dr.Sc. Alexander Korotkov

St.Petersburg State Polytechnical University, Russia,
korotkov@rphf.spbstu.ru

Wireless communication systems

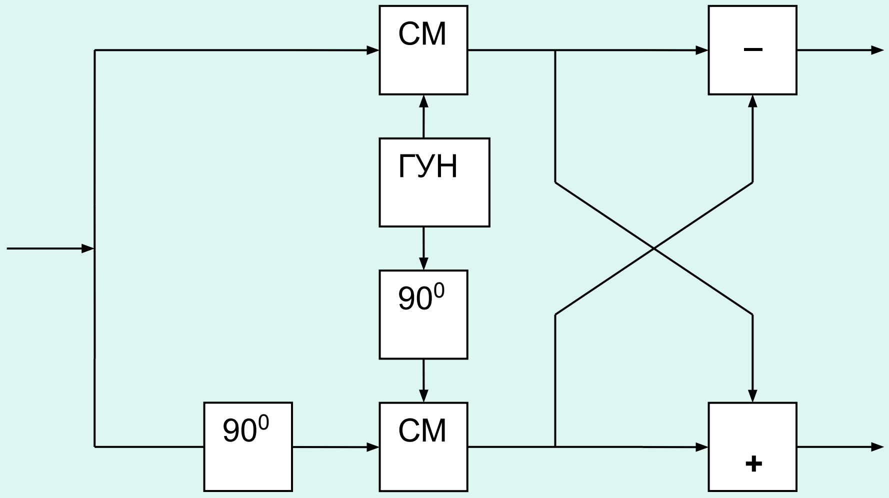
- *Cell phones* (GSM, WCDMA),
- *Bluetooth*,
- *Wireless local area network* (WLAN),
- *Digital enhanced cordless telecommunications* (DECT).

The architecture of the systems is oriented in general to realization of direct conversion receivers, also called

- zero IF receivers or

- low IF receivers.

Transceiver quadratur modulator



Input signal $U_{in}(t) = U_I(t) = U_m(t)\cos(\omega_m t)$

$U_Q(t) = -U_m(t)\sin(\omega_m t)$

Heterodyne $U_0(t) = U_{0m}\cos(\omega_0 t)$

Mixers

$$U_{MIX1}(t) = 0.5KU_m(t)U_{0m}(\cos(\omega_0 - \omega_m)t + \cos(\omega_0 + \omega_m)t)$$

$$U_{MIX2}(t) = 0.5KU_m(t)U_{0m}(\cos(\omega_0 - \omega_m)t - \cos(\omega_0 + \omega_m)t)$$

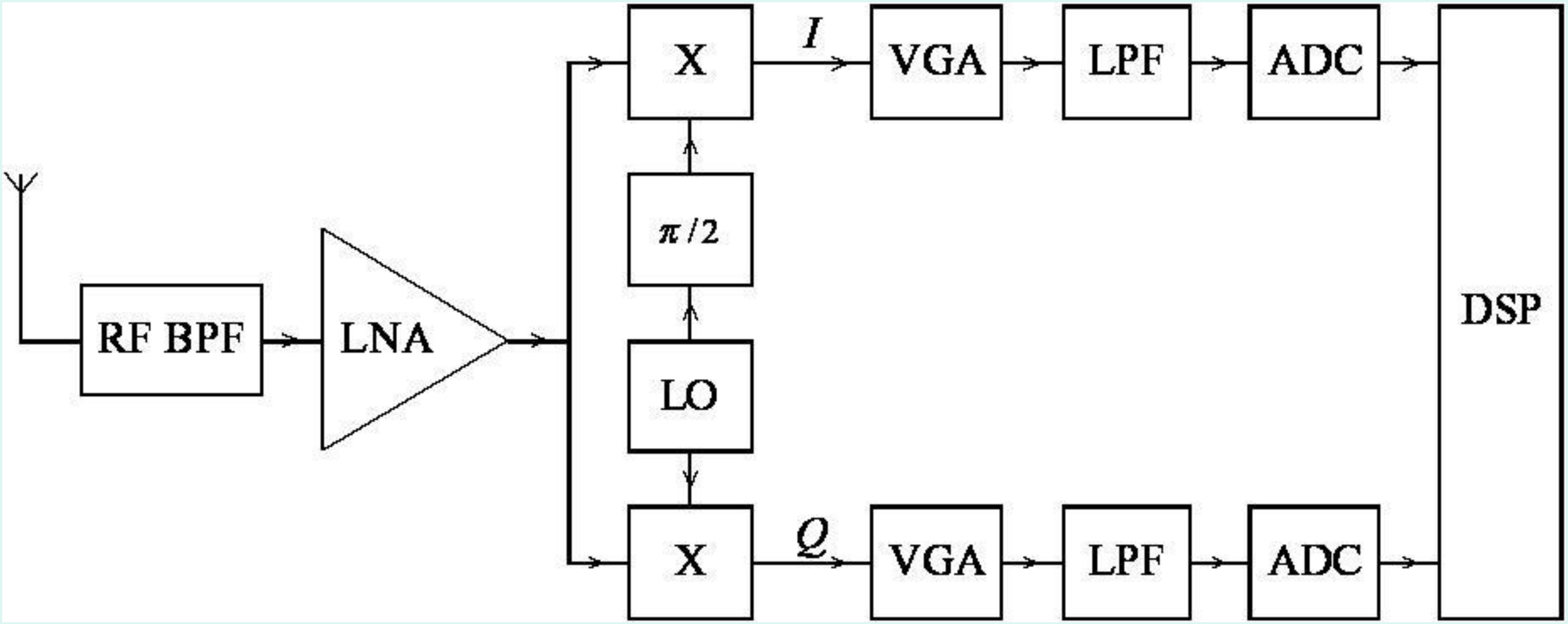
Output signals

$$U_{OUT+}(t) = KU_m(t)U_{0m}\cos(\omega_0 + \omega_m)t$$

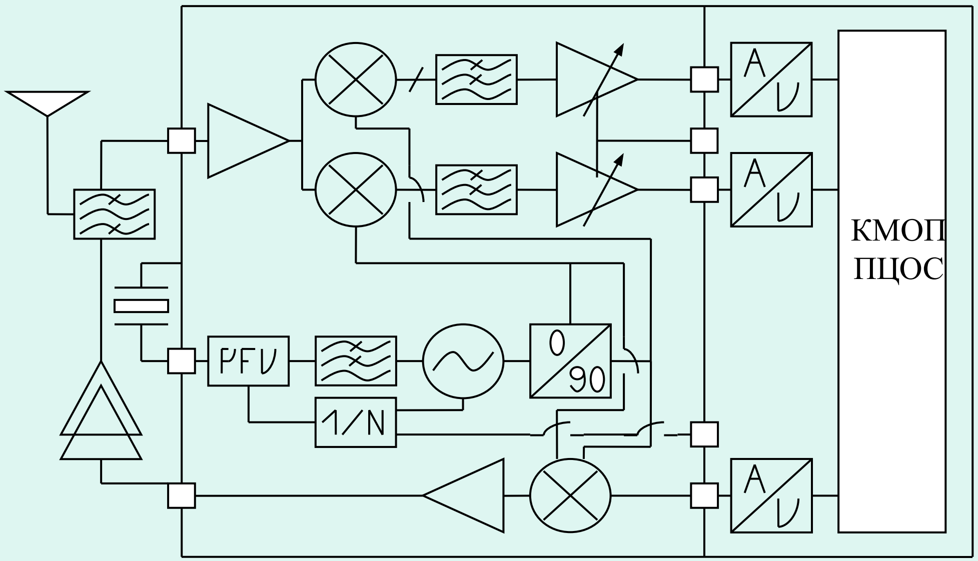
$$U_{OUT-}(t) = KU_m(t)U_{0m}\cos(\omega_0 - \omega_m)t$$

Receiver architecture

RF bandpass filter (RF BPF), low noise amplifier (LNA)
I/Q channels:
2 mixers, local oscillator (LO), phase shifter, variable gain amplifiers (VGA), channel selected low-pass filters (LPF), analog-to-digital converters (ADC), DSP.



Transceiver architecture



Структурная схема приемопередающего устройства стандарта GSM.

Signals in the receiver interface

Let us consider an input signal as

$$U(t) = aU_m(t)\cos(\omega_0 + \omega_m)t$$

Signals from mixers are (VCO has the same frequency as in the transceiver modulator)

$$U_{MIX1}(t) = 0.5aKU_m(t)U_{0m}(\cos(\omega_m t) + \cos(2\omega_0 + \omega_m)t) \qquad U_{MIX2}(t) = -0.5aKU_m(t)U_{0m}(\sin(\omega_m t) - \sin(2\omega_0 + \omega_m)t)$$

After Low-pass filters we have

$$U_I(t) = 0.5aKU_m(t)U_{0m}\cos(\omega_m t)$$

$$U_Q(t) = -0.5aKU_m(t)U_{0m}\sin(\omega_m t)$$

Advantages of zero IF receiver

- High-performance off-chip bandpass filter in the IF part of receivers can be changed to on-chip low-pass filter.
- Way to realization of fully CMOS technology based system (System on Chip design).
- Small size
- Low realization costs
- Low power consumption
- Multi-functionality

General requirements for receivers

Система	Назначение	Полоса тракта частот модуляции	Разрешение (динамический диапазон)	Несущая частота
		МГц	число разрядов	ГГц
WCDMA	Передача данных и речи	3.8 – 5	6 – 8	1.9
GSM900 DCS1800 PCS1900	Передача речи	0.2	12 – 14	0.9 1.8 1.9
802.11b 802.11a 802.11g	Передача данных	22 20 20 – 22	6 – 8 10 – 14 10 – 14	2.4 5.1 2.4
Bluetooth	Передача данных	1	13	2.4

General requirements for multistandard receivers

Блок, стандарт	Максимальный коэффициент усиления	Коэффициент шума или спектральная плотность	Коэффициент сжатия по уровню 1 дБ	Параметр IIP3	Параметр IIP2
МШУ, WLAN	18 дБ	3 дБ	–15 дБм	–5 дБм	–
МШУ, GSM	23 дБ	3 дБ	–15 дБм	–5 дБм	–
МШУ, WCDMA	18 дБ	3 дБ	–10 дБм	0 дБм	–
Универсальный МШУ	23 дБ	3 дБ	–10 дБм	0 дБм	–
Смеситель, WLAN	12 дБ	4 нВ/sqrt(Гц)	–5 дБм	5 дБм	+60 дБм
Смеситель, GSM	12 дБ	9 нВ/sqrt(Гц)	–3 дБм	7 дБм	+75 дБм
Смеситель, WCDMA	15 дБ	4.5 нВ/sqrt(Гц)	+2 дБм	12 дБм	+60 дБм
Универсальный смеситель	15 дБ	4 нВ/sqrt(Гц)	+2 дБм	12 дБм	+75 дБм

Non-linear parameters

«характеристические точки мощности интермодуляционных искажений N–ого порядка» *IIP*N

(N-th order Intermodulation Intercept Point). N равно 2, 3.

Пусть на схему воздействует входной сигнал вида:

$$x(t) = A\cos\omega_1 t + A\cos\omega_2 t$$

С учетом нелинейностей второго порядка, выходной сигнал:

$$y(t) = y_1(t) + y_2(t) = a_1 x(t) + a_2 x^2(t)$$

Определение: *IIP*2 – это мощность входного сигнала на одной из частот, например *ω*1, при которой гармоника $\omega_1 \pm \omega_2$ интермодуляционных искажений на частоте равна гармонике основной частоты *ω*1:

$$y_{1m}(t) = y_{2m}(t) \Rightarrow a_1 A_{IIP2} = a_2 A_{IIP2}^2 \Leftrightarrow A_{IIP2} = \frac{a_1}{a_2} \qquad IIP_2 = \frac{A_{IIP2}^2}{2R} = \left|\frac{a_1}{2a_2 R}\right| \qquad IIP_2 = 10\lg\frac{1}{0.001}\left|\frac{a_1}{2a_2 R}\right|$$

R – нагрузочное сопротивление

IIP3

Выходной сигнал

$$y(t) = y_1(t) + y_3(t) = a_1 x(t) + a_3 x^3(t)$$

В этом случае *IIP*3 – это мощность входного сигнала на одной из частот, например *ω*1, при которой гармоника

интермодуляционных искажений на частоте $2\omega_1 \pm \omega_2$

равна гармонике основной частоты *ω*1:

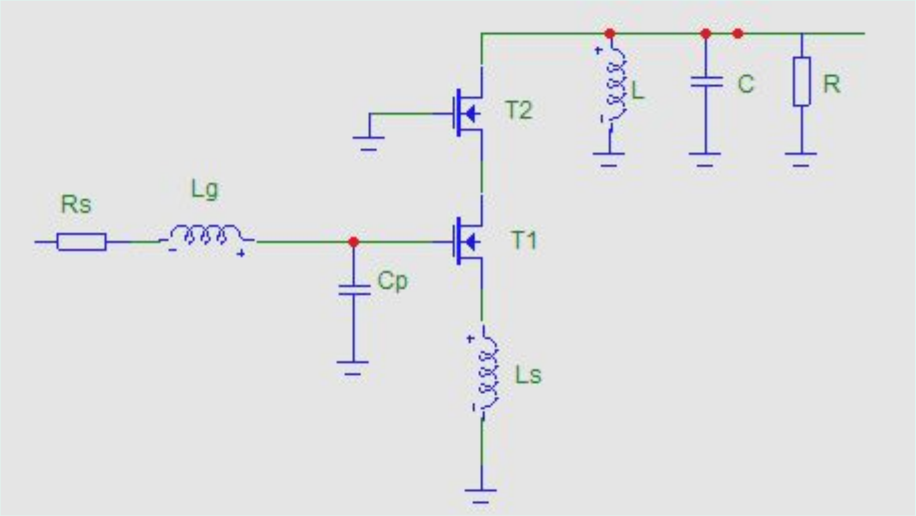
$$y_{1m}(t) = y_{3m}(t) \Rightarrow a_1 A_{IIP3} = \frac{3}{4} a_3 A_{IIP3}^3 \Leftrightarrow A_{IIP3} = \sqrt{\frac{4}{3}\frac{a_1}{a_3}}$$

$$IIP_3 = \frac{A_{IIP3}^2}{2R} = \left|\frac{2a_1}{3a_3 R}\right| \qquad IIP_3 = 10\lg\frac{1}{0.001}\left|\frac{2a_1}{3a_3 R}\right|$$

$$\frac{1}{K_{ÍÈ\ 3}} = \left|\frac{a_1 A}{0.25 a_3 A^3}\right| = \left|4\frac{a_1}{a_3}\right|\frac{1}{A^2}$$

$$K_{ÍÈ\ 3} = \frac{A^2}{6 IIP_3 R}$$

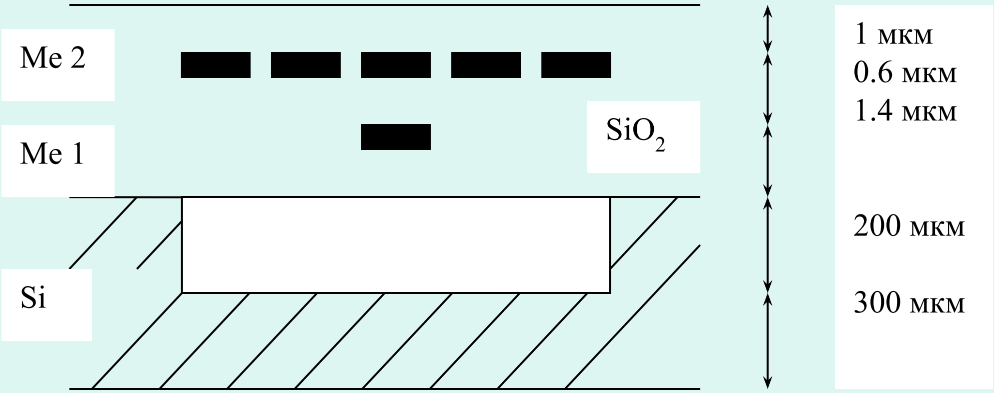
Low-Noise Amplifier for Receiver



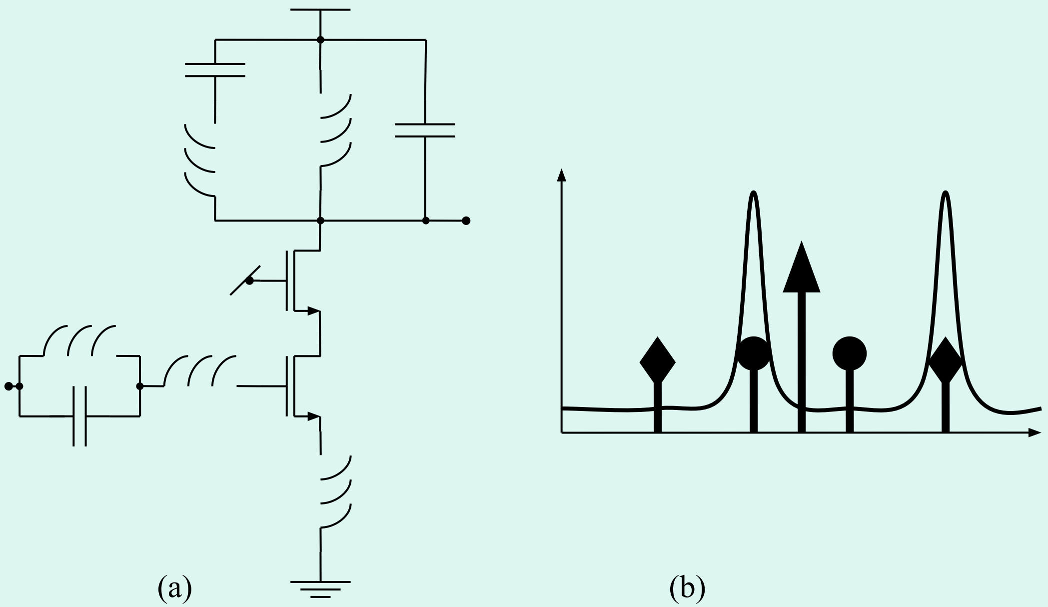
$$Z_{in} = p(L_G + L_S) + \frac{1}{pC_p} + \omega_T L_S$$

$$\omega_T = g_m / C_{GS}$$

Согласование по мощности в узкой полосе частот осуществляется *Lg*, в то время как коэффициент шума минимизируется соответствующим выбором *Ls*.

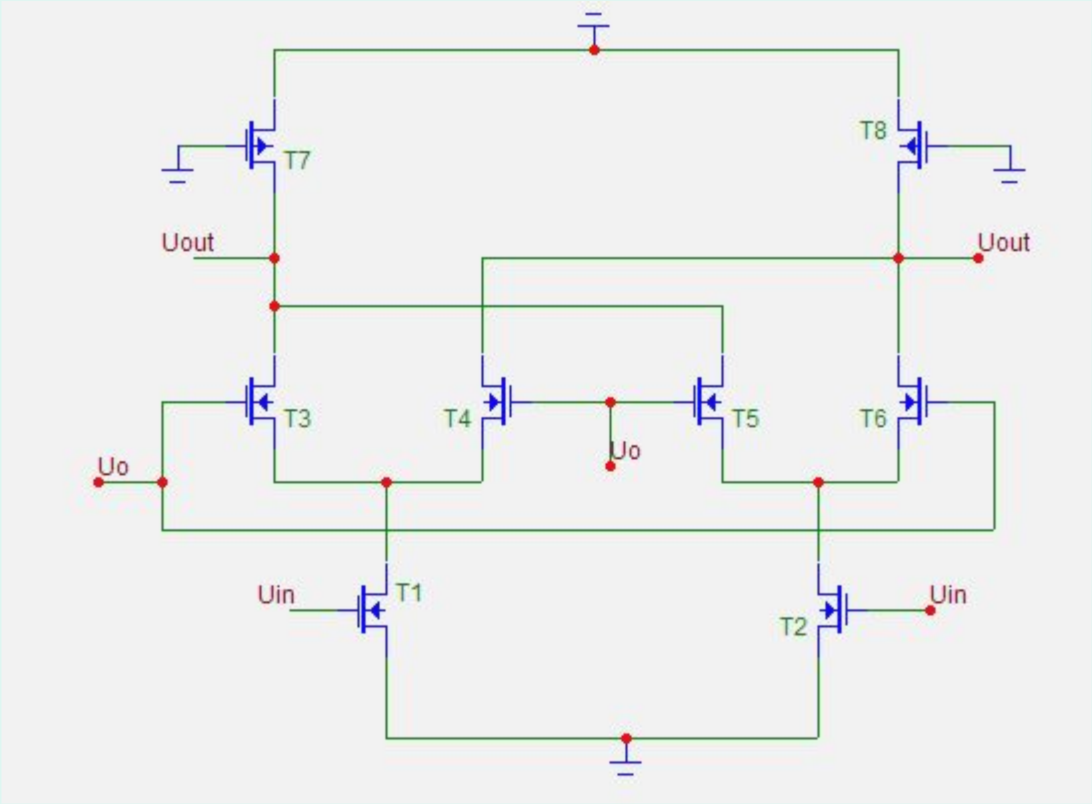


Low-Noise Amplifier for Multistandard Receiver



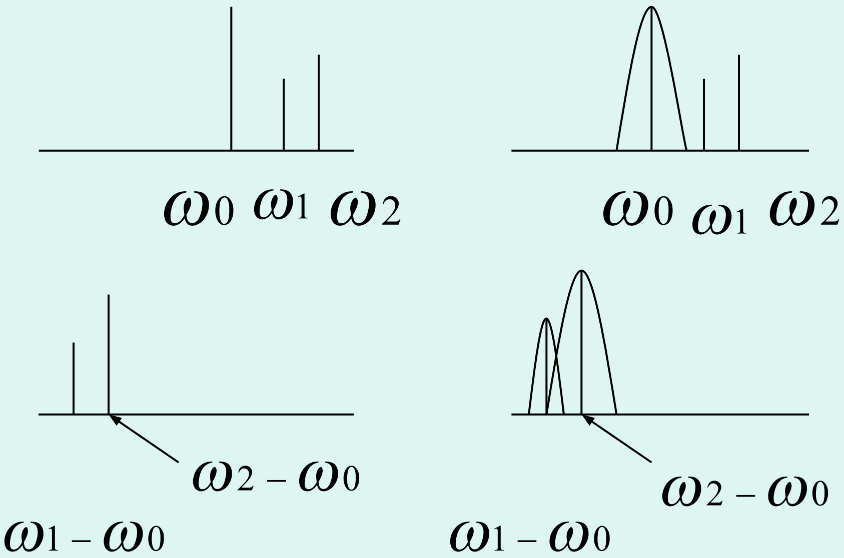
(a) (b)

Mixers for Receiver (Multistandard Receiver)



Эквивалентная схема преобразователя Гильберта по переменному току.

Voltage-Controlled Oscillator for Receiver

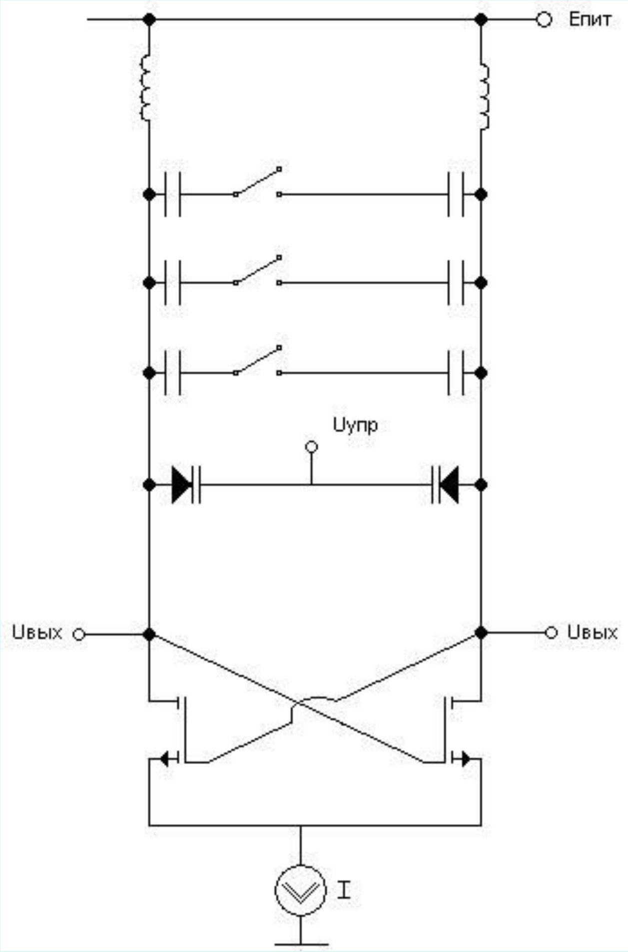


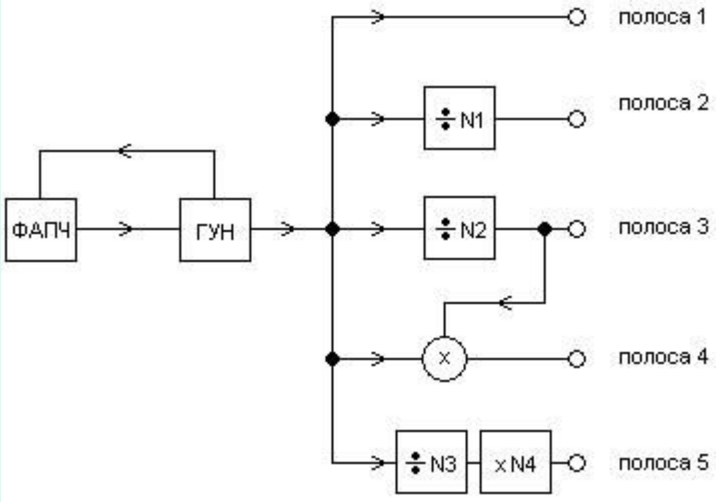
Фазовые шумы,
отстройка 100 кГц
- 100 -110 дБ/Гц

Типовой диапазон перестройки
ГУН составляет
порядка 20%,
в лучших случаях – до 50%

Основные типы задающих генераторов
кольцевой генератор
релаксационный генератор
LC-генератор по трехточечной схеме

Voltage-Controlled Oscillator for Multistandard Receiver





Filter Design:
Some common features

- The order of filters is of 5th at least.
- The cut-off frequency is about some megahertz.
- More strict requirements are mainly made to filters of voice communication systems.
- Methods of the filter implementation are **cascaded design based of current buffers, cascaded design based on voltage buffers, transconductance based realization (Gm-C filter), and SC-filter design.**

Low-pass channel selected filter requirements

System	*Cell phones*	*Bluetooth*	*WLAN*	*DECT*
Cut-off frequency, MHz	0.10 – 2.1	0.5 – 1.0	0.625 – 10.0	0.7
IIP3, dBm	11 – 60	10 – 28	22.5	47
Noise, nV/sqrtHz	25 – 150	30 – 80	15 – 50	30
Power Consumption, mW	2 – 50	2 – 17	18 – 50	15 – 35
Filter type	CT, 5 – 7 order	CT, 5 – 6 order	CT, 5 order	SC, 6 – 8 order

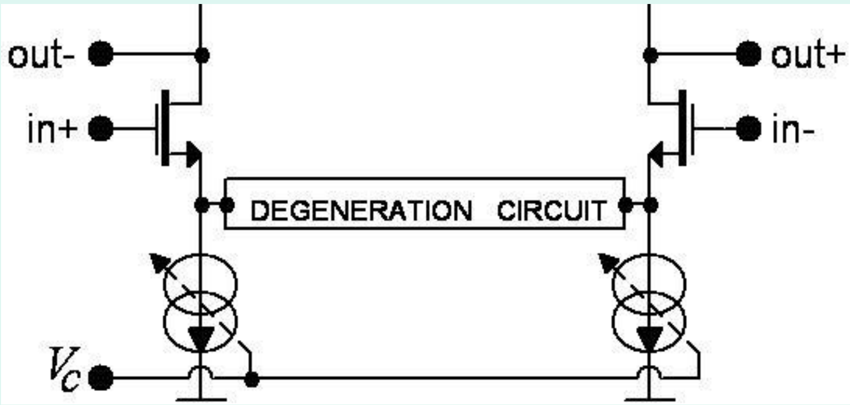
Conception

- Cascaded design allows implementation of high performance filters.
- Cascaded realizations are not optimal from a technological point of view, because it needs CMOS implementation of resistors that is a relatively expensive and undesirable operation.
- Gm-C filters and SC-filters have got some advantages, because these circuits can be realized without resistive elements.
- The concept of multistandard cell phone filter realization considered by H.A.Alzaher, H.O.Elwan, and M.Ismail, 2002, can be extended to the design of the universal LPF for communication systems in a whole.
- The universal filter should be of the 5th-7th order and has tuning range from 100 kHz to 10 MHz.

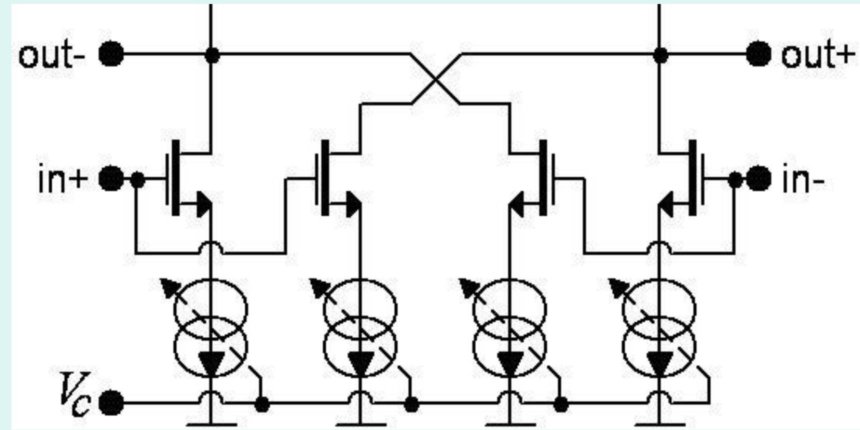
- **These are reasons that efforts have been concentrated under the synthesis of the 5th order LPF with the cut off frequency equal to 1MHz.**

Gm-C filter design

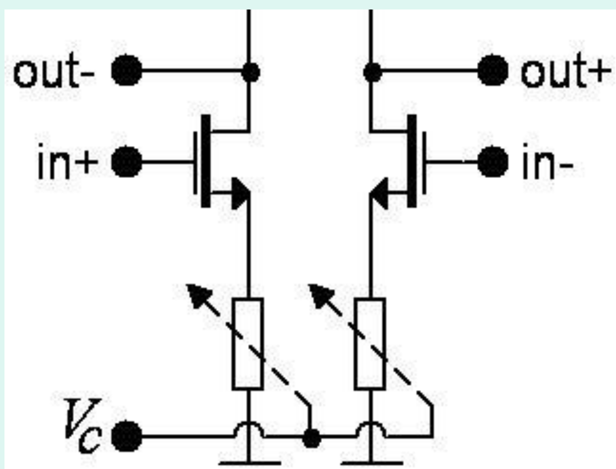
a) CMOS transconductance amplifier design

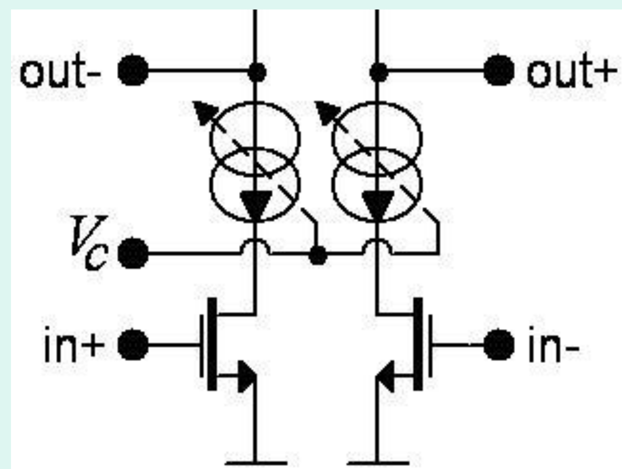


Stage with degeneration



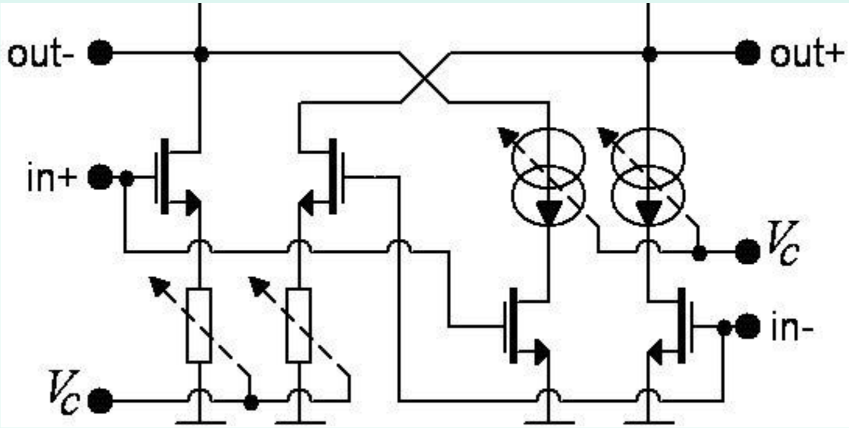
Cross-coupled stage



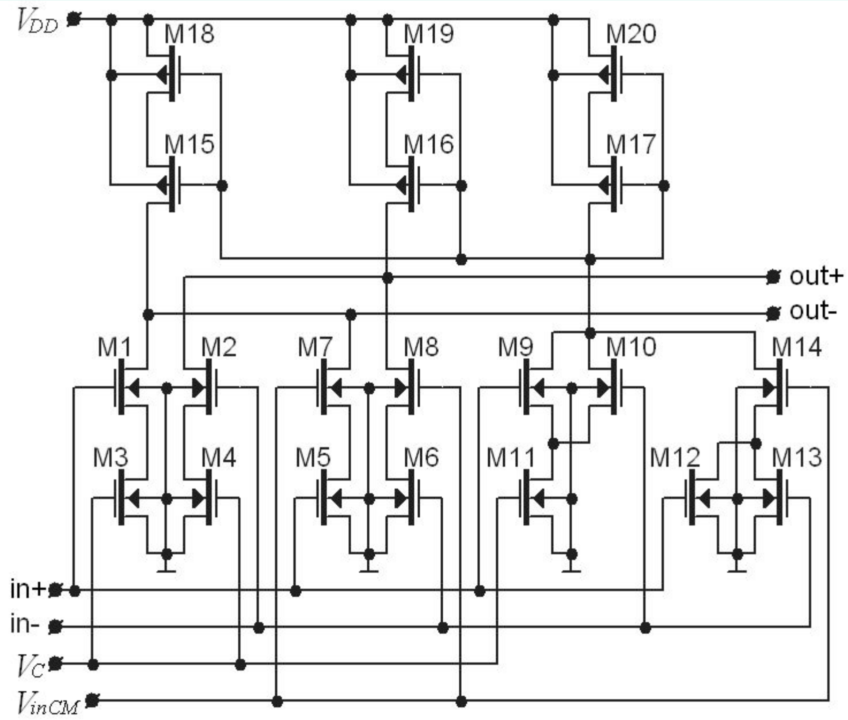


Low-voltage stages: 2 transistors are in linear region

Proposed transconductor circuit

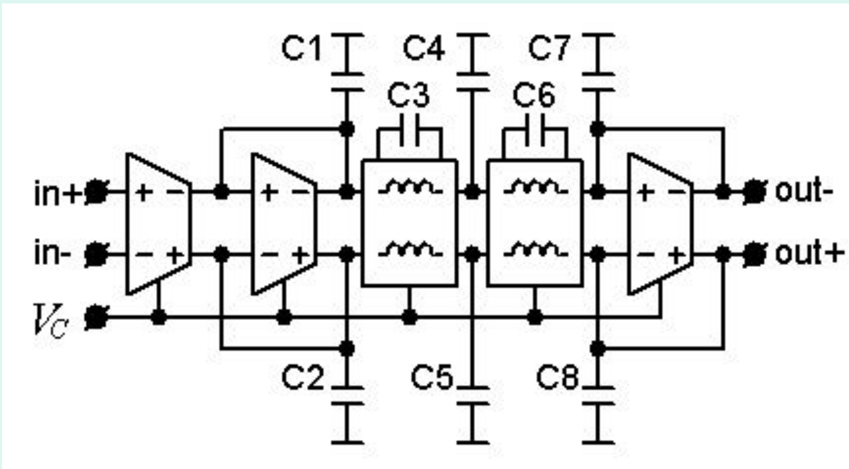


Input stage [1]

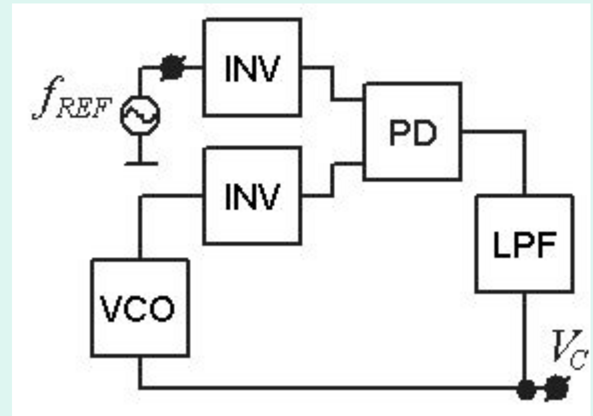


Complete structure [2], [3]

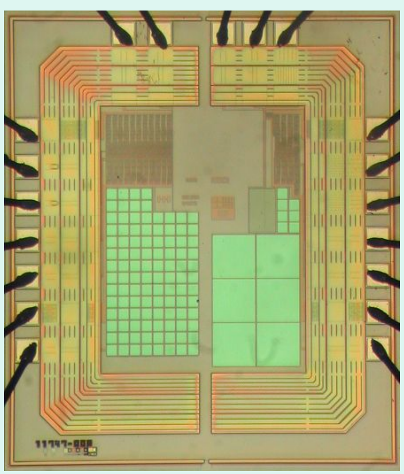
b)Gm-C filter design



Structure of the filter [2], [3]



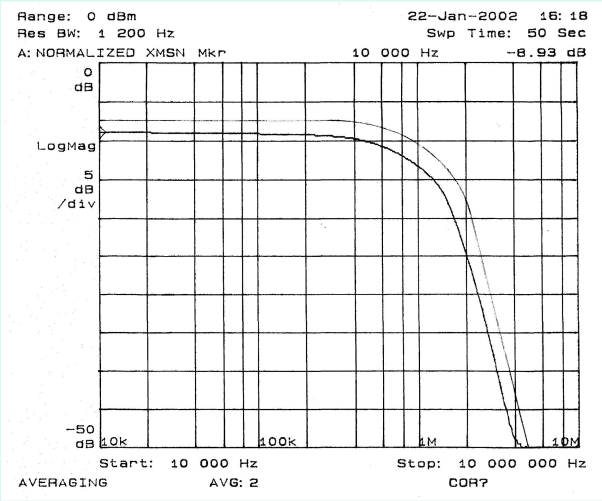
Tuning system



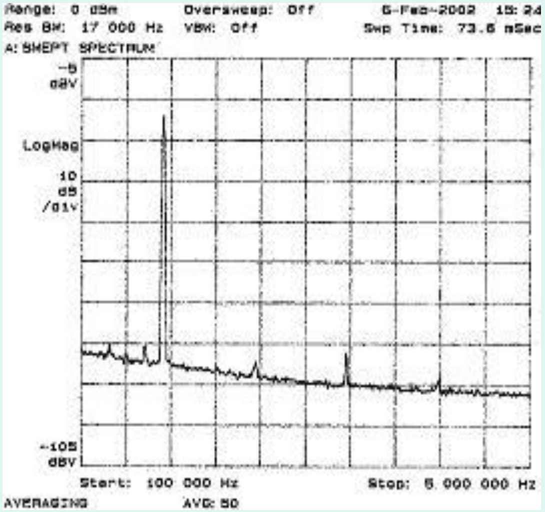
Layout

Filter type	5th order, Bessel
Cutoff frequency	1 MHz
Technology	0.35µ CMOS

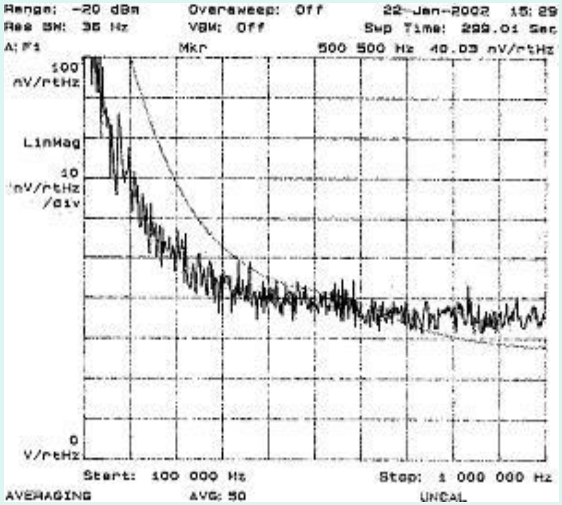
Practical results



Amplitude response



Output spectrum



Noise spectrum (simulation and experiment)

Filter characteristics

Test chip area	2.625 mm2	HD3, F = 1 MHz, V_{in} p-to-p =1 V	−54 dB
Filter area	0.340 mm2	Input noise	85 nV/sqrtHz
Tuning system area	0.280 mm2	RMS noise	120 μVrms
Voltage supply	+2.5 V	Power consumption	
V_{inCM}	+1.25 V	including tuning system	11.25 mW
V_{C}	+1.41 ÷+1.47 V	without tuning system	8.25 mW
F_{ref}	2 MHz		

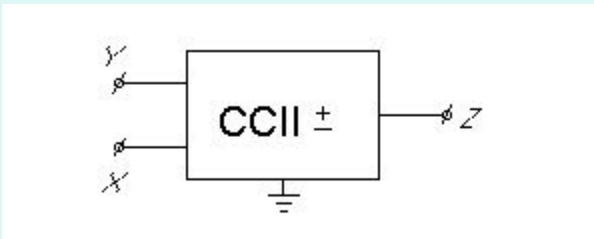
Current conveyor (CCII) based filter design

An alternative way for the high-frequency filter realization is using of current-mode circuits. One of the promising approaches is the circuit synthesis based on the second generation current conveyors (CCII). A new way to the design of high-frequency filters which can operate without the tuning system is proposed. An idea of the approach is based on a combination of switched-capacitor (SC) and mixed current/voltage mode techniques.

One of the main factors limiting the working frequency range of the existing SC-filters in the order of 100-200 kHz is the limited gain-bandwidth product

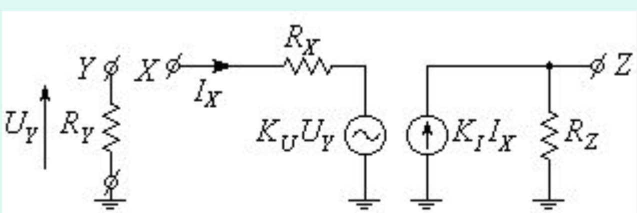
The main advantage of the CCII is the larger frequency range in comparison with the standard OpA.

CCII and SC-integrators on its basis



$$\begin{bmatrix} I_Y \\ v_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ k & 0 & 0 \\ 0 & \pm\alpha & 0 \end{bmatrix} \begin{bmatrix} v_Y \\ I_X \\ v_Z \end{bmatrix}$$

$$Z_{in.X} = 0, \quad Z_{in.Y} = \infty, \quad Z_{out.Z} = \infty.$$



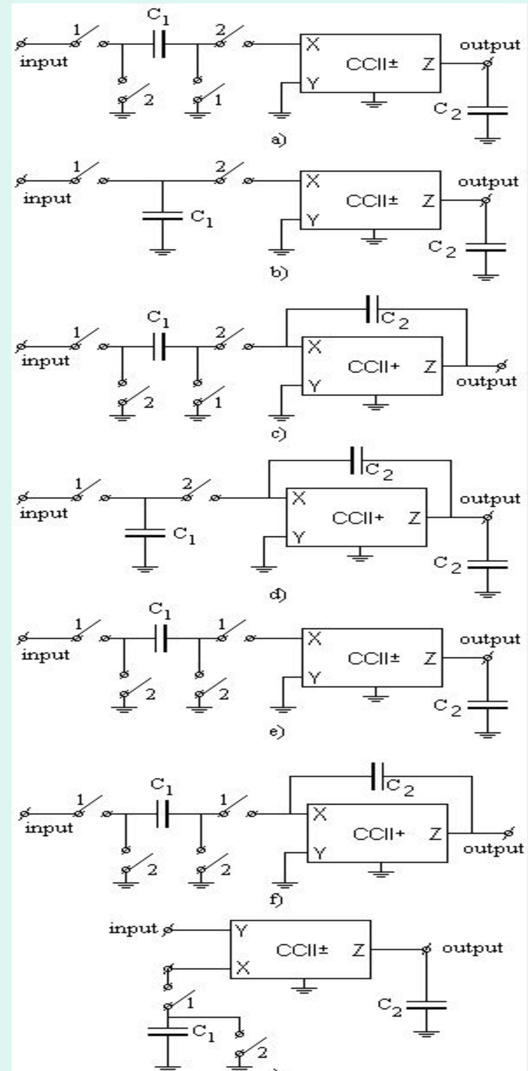
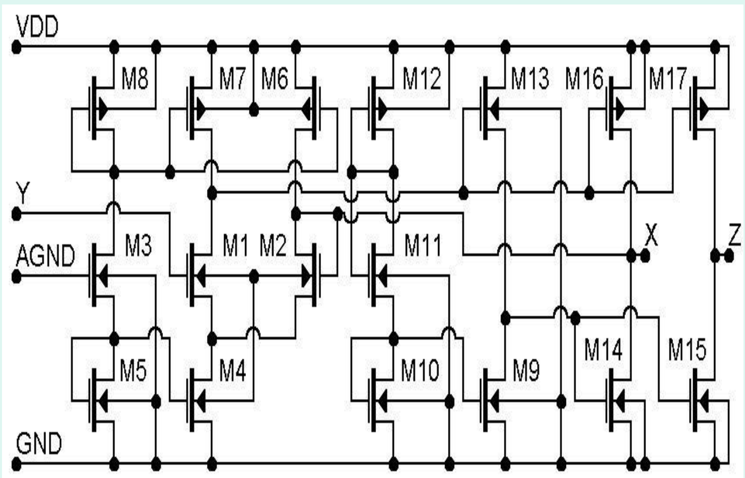
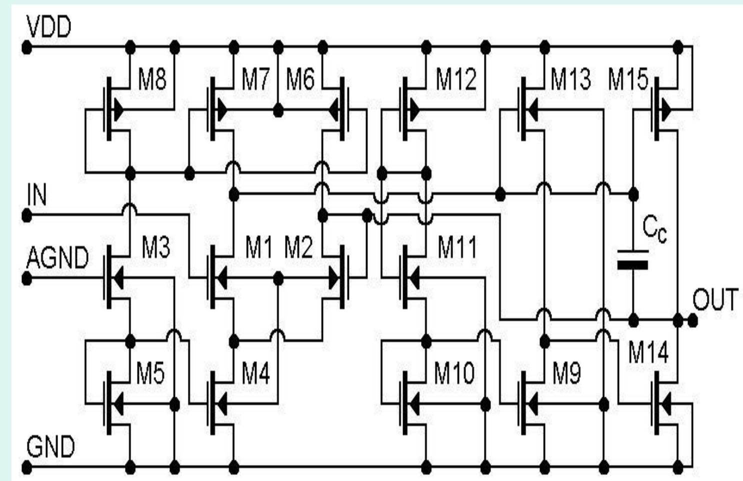


Fig. 2. CCII based SC-integrators.

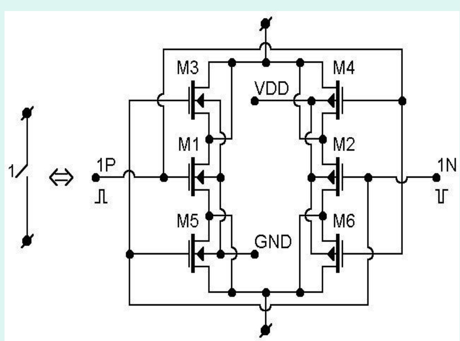
a) Filter blocks



Current conveyor [5]

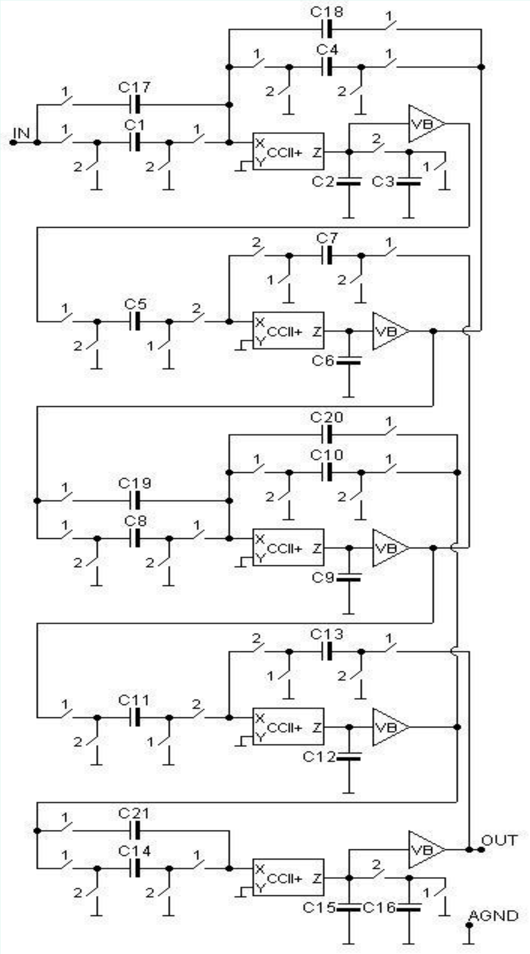


Voltage buffer [5]



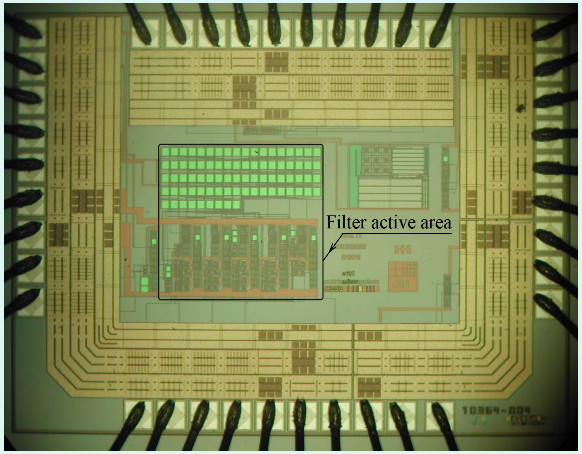
CMOS dummy switch

b) Filter structure



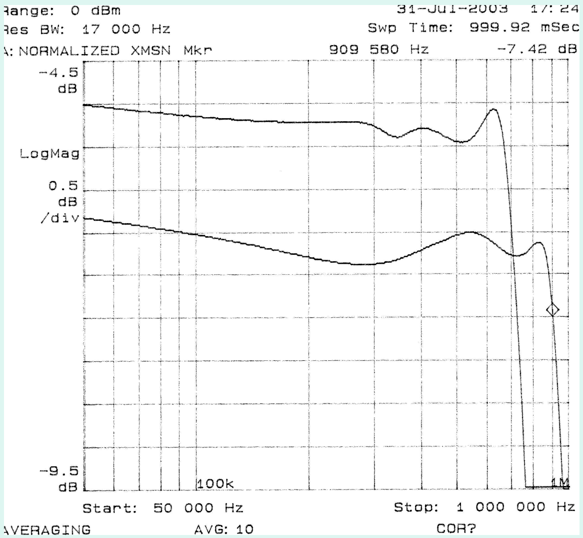
The synthesized filter is based on the parasitic insensitive integrators [4].

The filter has been realized by means of Operational simulation method when the structure of the circuit corresponds to the serial chain of integrators with multi feedback loops

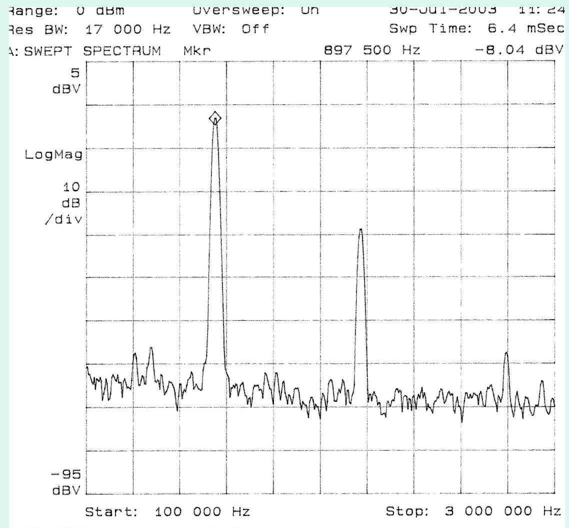


Filter layout

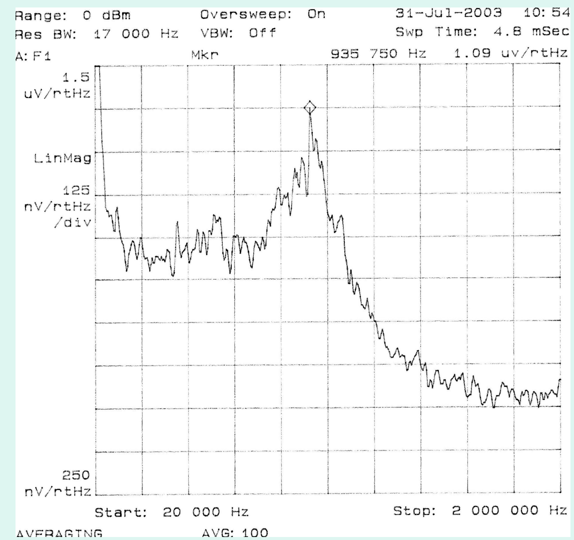
Practical results



Amplitude response



Output spectrum



Noise spectrum

Filter characteristics

Filter type	5th order, Chebyshev	
Technology	0.35μm CMOS	
Filter area	0.25 mm2	
Voltage supply	+3.0 V	+2.5 V
V_{agnd}	+1.50 V	+1.25 V
Cut-off frequency	900 kHz	700 kHz
Power consumption	9.9 mW	3.0 mW
HD3, HD2	**−54dB, −26dB (*Vin*P-to-P = 2 V, *f* = 900 kHz)**	**−49dB, −24dB (*Vin*P-to-P = 1 V, *f* = 700 kHz)**
Input noise	1.34μV/sqrtHz	1.27μV/sqrtHz

Analog-to-Digital Converters

- Main types of ADC's are

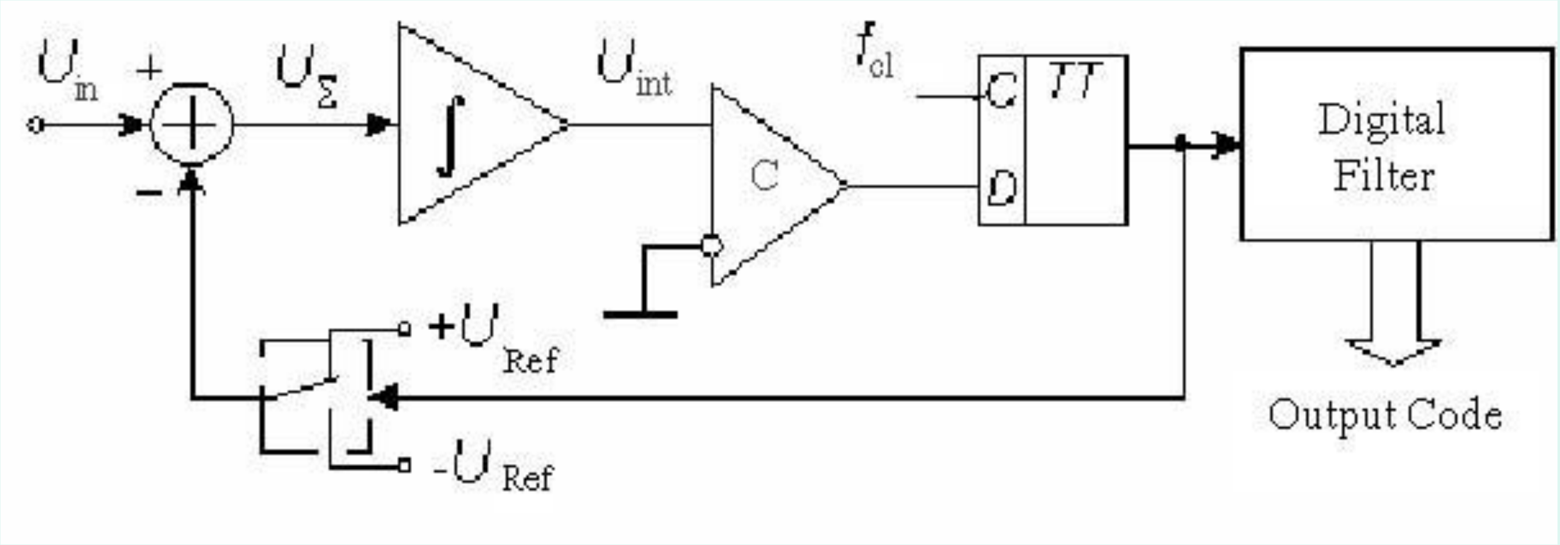
- Parallel-flash (параллельный)
- Successive Approximation (последовательных приближений)
- Pipeline (конвейерный)
- Delta-Sigma (на основе дельта-сигма модулятора)

SWITCHED-CAPACITOR DELTA-SIGMA MODULATORS

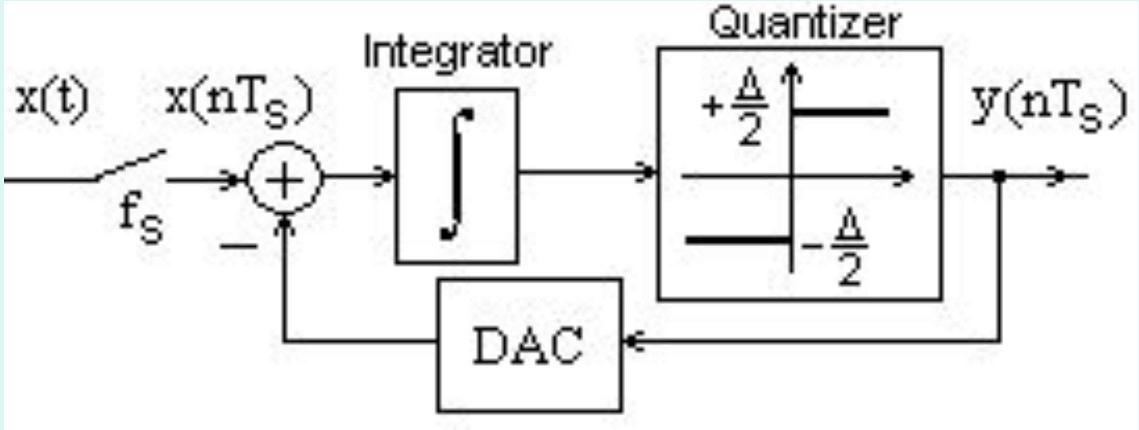
Advantages:

- Wide dynamic range;
- Low noise;
- High linearity;
- Low power supply.

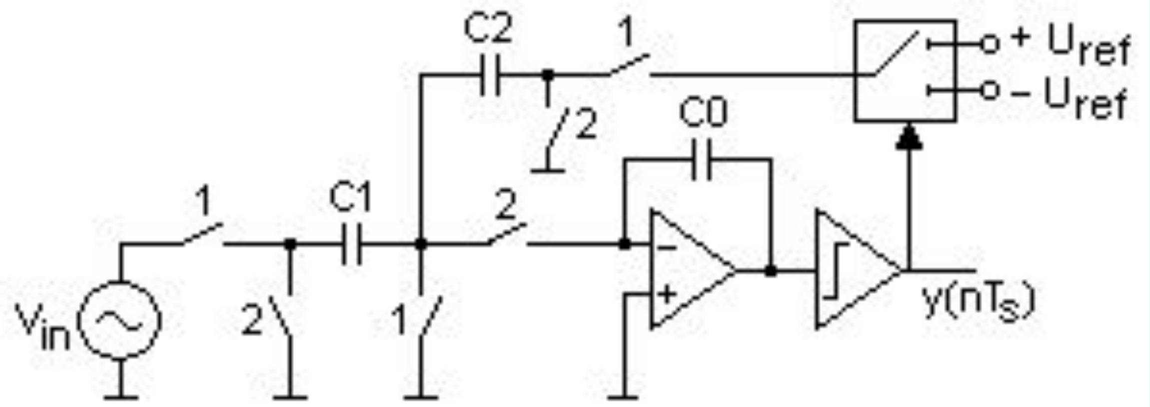
First Order Delta-Sigma ADC Block Diagram



DELTA-SIGMA MODULATOR



A representation of the first-order delta-sigma (ΔΣ) modulator



SC implementation of first-order ΔΣ modulator

SIMULATION PROGRAMS OVERVIEW

Program	Analysis approach (method)	Analysis in time domain	Analysis in frequency domain	Thermal noise analysis	Linear imperfections		Non-linear properties
					Switch resistance	OpA bandwidth	
TOSCA	presents circuits as a set of macroblocks described in terms of internal state variables	+	+			+	+
AWEswit	presents circuits as a low order dominant pole model	+			+	+	
ASIDES	presents circuits as a set of macroblocks described in terms of internal state variables	+		+	+	+	+
ZSIM	tableau method	+					
SWITCAP2	performs transient MNA based analysis for linear circuits	+					
SDSIM	formulates a set of finite difference equations of the circuit	+			+	+	*
SCNAP5	formulates set of the difference equation by using MNA	+			+	+	

SOLVING OF LINEAR CIRCUIT EQUATIONS

A representation of the SC circuit by the set of linear differential equations in the nodal analysis form

$$\mathbf{C}_k \frac{d}{dt} u_k(t) + \mathbf{G}_k u_k(t) = w_k(t), \quad k = 1, \ldots, N$$

$\boldsymbol{C}_k$ and $\boldsymbol{G}_k$ are capacitance and conductance matrices,
w_k is the input source vector,
u_k is the vector of unknown nodal voltages,
N is the number of phases.

After Laplace transformation of the set its solution is expressed as

$$u_k(t) = L^{-1}\left\{\left[s\mathbf{C}_k + \mathbf{G}_k\right]^{-1} \cdot \left(\mathbf{C}_k u_{k-1}(t) + W_k(s)\right)\right\}$$

where the symbol $L^{-1}\{.\}$ means the operator of inverse Laplace transformation.

SOLVING OF NONLINEAR CIRCUIT EQUATIONS

A representation of the SC circuit by the set of nonlinear differential equations in the nodal analysis form

$$\mathbf{C}_k \frac{d}{dt} u_k(t) + \mathbf{G}_k u_k(t) = w_k(t) + f\left(u_k(t), \frac{d^i}{dt^i} u_k(t) \right),$$

where $f(\cdot)$ is a function describing nonlinear properties of elements.

The circuit node variable vector using a truncated Volterra series expansion is expressed by

$$u_k(t) \approx u_{1k}(t_1) + u_{2k}(t_1, t_2) + u_{3k}(t_1, t_2, t_3) \Big|_{\substack{t_1 = t \\ t_2 = t \\ t_3 = t}}$$

For analysis of the second and the third harmonics the excitation vectors are presented in general form as

$$\begin{aligned} w_{2k}(t) &= f_2(u_{1k}(t)), \\ w_{3k}(t) &= f_3(u_{1k}(t), u_{2k}(t_1, t_2)). \end{aligned}$$

A. Capacitance nonlinearities

Nonlinear properties of the each parasitic drain-bulk and source-bulk capacitors of MOS transistors as switches are approximated by polynomial expression

$$c(u(t)) = c_0 + a_1\, u(t_1) + a_2\, (u(t_1))^2 + \cdots$$

The nonlinear capacitance matrix is rewritten as

$$\mathbf{C}(u(t)) = \mathbf{C}_0 + \mathbf{C}_1\, u_{1k}(t_1) + \mathbf{C}_2\, u_{1k}(t_1) u_{1k}(t_1) + \cdots$$

where expression "$u \cdot u$" means multiplication of corresponding elements of the vectors .
The nodal analysis model of SC circuit can be rewritten as

$$\mathbf{C}_{0k} \frac{d}{dt} u_{2k}(t_1, t_2) + \mathbf{G}_k u_{2k}(t_1, t_2) = -\mathbf{C}_{1k}\, u_{1k}(t_1) \frac{d}{dt} u_{1k}(t_2),$$

After two-dimensional Laplace transform the solution of the set is expressed as

$$\mathrm{U}_{2k}(s_1,s_2)=\left[\mathbf{C}_0(s_1+s_2)+\mathbf{G}\right]^{-1}\cdot\left[-\mathbf{C}_0\frac{(s_1+s_2)}{2}\mathrm{U}_{1k}(s_1)\mathrm{U}_{1k}(s_2)+\mathbf{C}_0\,\mathrm{U}_{2k}(0,s_2)\right.$$
$$\left.+\mathbf{C}_0\,\mathrm{U}_{2k}(s_1,0)+\frac{\mathbf{C}_1}{2}u_{1k}(0)\left(\mathrm{U}_{1k}(s_1)+\mathrm{U}_{1k}(s_2)\right)\right],$$

where $\mathrm{U}_{2k}(0,s_2)$, $\mathrm{U}_{2k}(s_1,0)$ are *partial* initial conditions of the nodal voltage vector for k-th phase. The partial initial conditions are obtained from nodal analysis model given t_1=0, t_2=0 respectively.

$$\mathrm{U}_{2k}(s_1,0)=\left[\mathbf{C}_0\,s_1+\mathbf{G}\right]^{-1}\left[\mathbf{C}_0\,u_{2k}(0,0)\right.$$
$$\left.+\mathbf{C}_1\,u_{1k}(0)u_{1k}(0)-\mathbf{C}_1 s_1\,\mathrm{U}_{1k}(s_1)u_{1k}(0)\right],$$

$$\mathrm{U}_{2k}(0,s_2)=\left[\mathbf{C}_0\,s_2+\mathbf{G}\right]^{-1}\left[\mathbf{C}_0\,u_{2k}(0,0)\right.$$
$$\left.+\mathbf{C}_1\,u_{1k}(0)u_{1k}(0)-\mathbf{C}_1 s_2\,u_{1k}(0)\mathrm{U}_{1k}(s_2)\right],$$

B. Active elements nonlinearities

The nonlinear DC characteristic of balanced amplifier can be approximated as following polynomial expression

$$u_{\text{out}}(t) = \mu_0 \Delta u_{\text{in}}(t) + \mu_3 (\Delta u_{\text{in}}(t))^3 + \cdots$$

Taking into account only the third order harmonic the nodal voltage vector can be expressed by

$$u_k(t) \approx u_{1k}(t_1) + u_{3k}(t_1, t_2, t_3),$$

The nodal analysis model of SC circuit can be rewritten as

$$\mathbf{C}_k \frac{d}{dt} u_{3k}(t_1, t_2, t_3) + \mathbf{G}_k u_{3k}(t_1, t_2, t_3) = -\mathbf{G}_{3k}\; u_{3k}(t_1, t_2, t_3) u_{3k}(t_1, t_2, t_3) u_{3k}(t_1, t_2, t_3),$$

where $\mathbf{G}_{3k}$ is conductance matrix of coefficients corresponding to nonlinear items in polynomial expression describing active elements.
After three-dimensional Laplace transform the solution of the set is expressed as

$$\mathrm{U}_{3k}(s_1, s_2, s_3) = [\mathbf{C}(s_1 + s_2 + s_3) + \mathbf{G}]^{-1} \cdot [\mathbf{C}\,\mathrm{R}(s_1, s_2, s_3) - \mathbf{G}_{3k}\,\mathrm{U}_{1k}(s_1)\mathrm{U}_{1k}(s_2)\mathrm{U}_{1k}(s_3)],$$

where $\mathrm{R}(s_1, s_2, s_3) = \mathrm{U}_{3k}(0, s_2, s_3) + \mathrm{U}_{3k}(s_1, 0, s_3) + \mathrm{U}_{3k}(s_1, s_2, 0).$

The partial initial conditions are obtained from nodal analysis model given t_1=0, t_2=0, t_3=0 respectively.

$$\mathrm{U}_{3k}(0,s_2,s_3)=[\mathbf{C}(s_2+s_3)+\mathbf{G}]^{-1}[\mathbf{C}(\mathrm{U}_{3k}(0,0,s_3)+\mathrm{U}_{3k}(0,s_2,0))-\mathbf{G}_{3k}\,u_{1k}(0)\mathrm{U}_{1k}(s_2)\mathrm{U}_{1k}(s_3)],$$

$$\mathrm{U}_{3k}(s_1,0,s_3)=[\mathbf{C}(s_1+s_3)+\mathbf{G}]^{-1}[\mathbf{C}(\mathrm{U}_{3k}(0,0,s_3)+\mathrm{U}_{3k}(s_1,0,0))-\mathbf{G}_{3k}\,\mathrm{U}_{1k}(s_1)u_{1k}(0)\mathrm{U}_{1k}(s_3)],$$

$$\mathrm{U}_{3k}(s_1,s_2,0)=[\mathbf{C}(s_1+s_2)+\mathbf{G}]^{-1}[\mathbf{C}(\mathrm{U}_{3k}(0,s_2,0)+\mathrm{U}_{3k}(s_1,0,0))-\mathbf{G}_{3k}\,\mathrm{U}_{1k}(s_1)\mathrm{U}_{1k}(s_2)u_{1k}(0)],$$

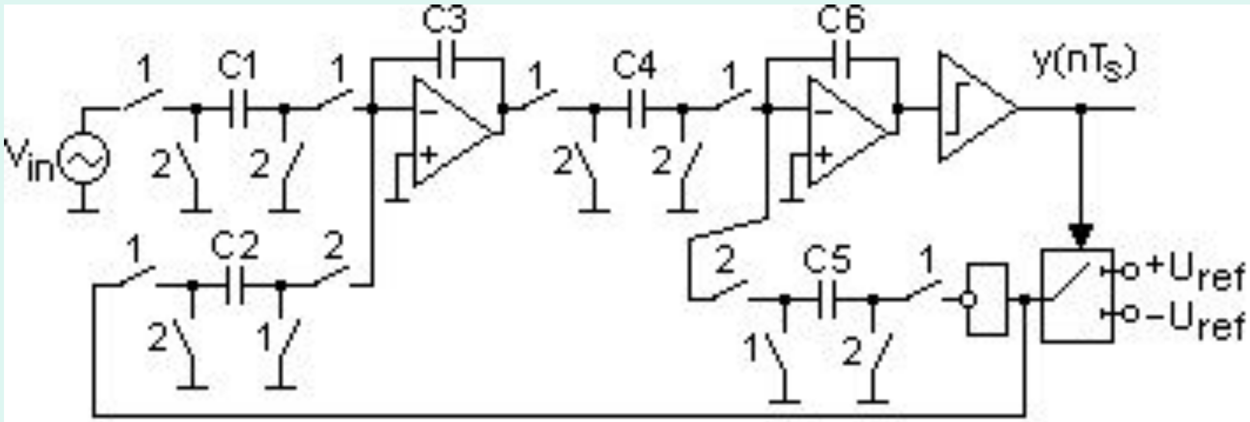
$$\mathrm{U}_{3k}(s_1,0,0)=[\mathbf{C}s_1+\mathbf{G}]^{-1}[\mathbf{C}u_{3k}(0,0,0)-\mathbf{G}_{3k}\,\mathrm{U}_{1k}(s_1)u_{1k}(0)u_{1k}(0)],$$

$$\mathrm{U}_{3k}(0,s_2,0)=[\mathbf{C}s_2+\mathbf{G}]^{-1}[\mathbf{C}u_{3k}(0,0,0)-\mathbf{G}_{3k}\,u_{1k}(0)\mathrm{U}_{1k}(s_2)u_{1k}(0)],$$

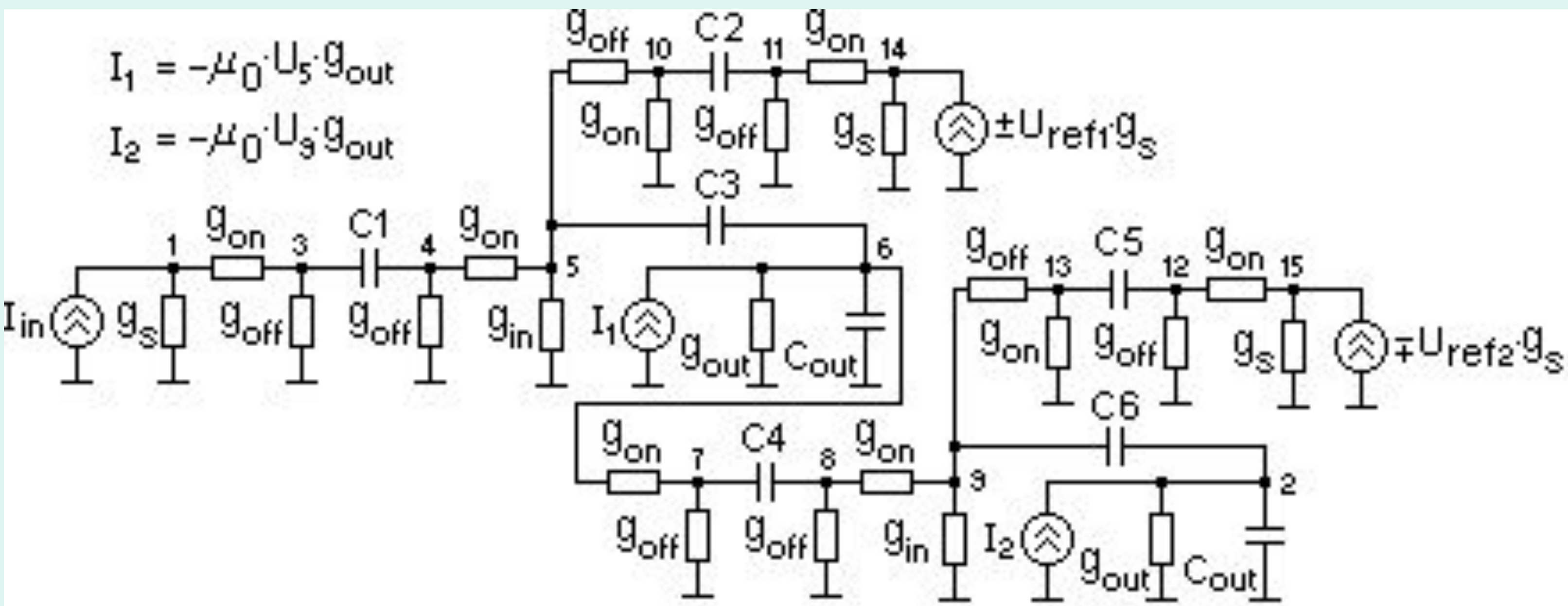
$$\mathrm{U}_{3k}(0,0,s_3)=[\mathbf{C}s_3+\mathbf{G}]^{-1}[\mathbf{C}u_{3k}(0,0,0)-\mathbf{G}_{3k}\,u_{1k}(0)u_{1k}(0)\mathrm{U}_{1k}(s_3)].$$

SIMULATION EXAMPLE

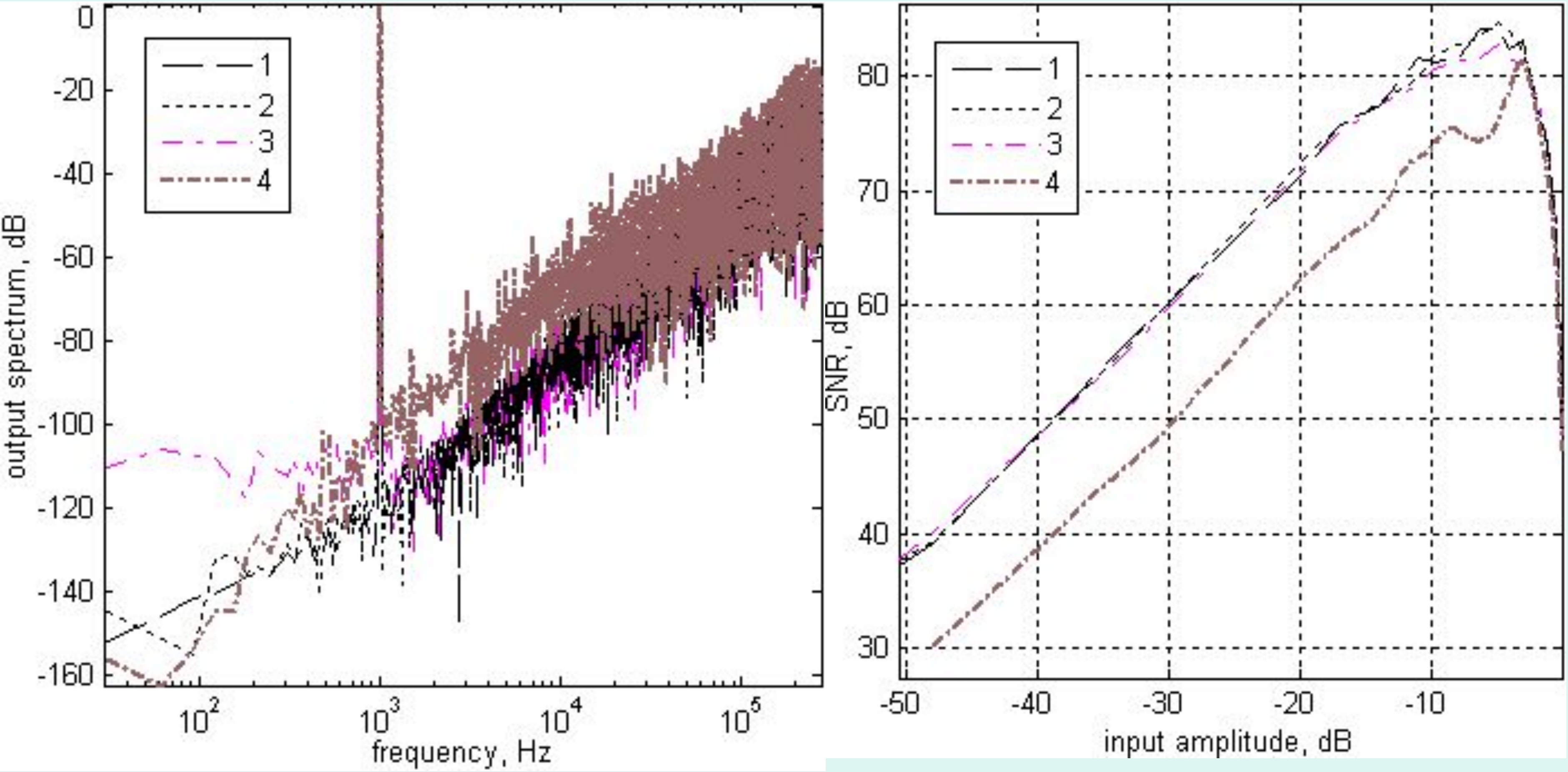
Implementation of second-order ΔΣ modulator



The equivalent circuit of the second-order ΔΣ modulator SC part in the first phase

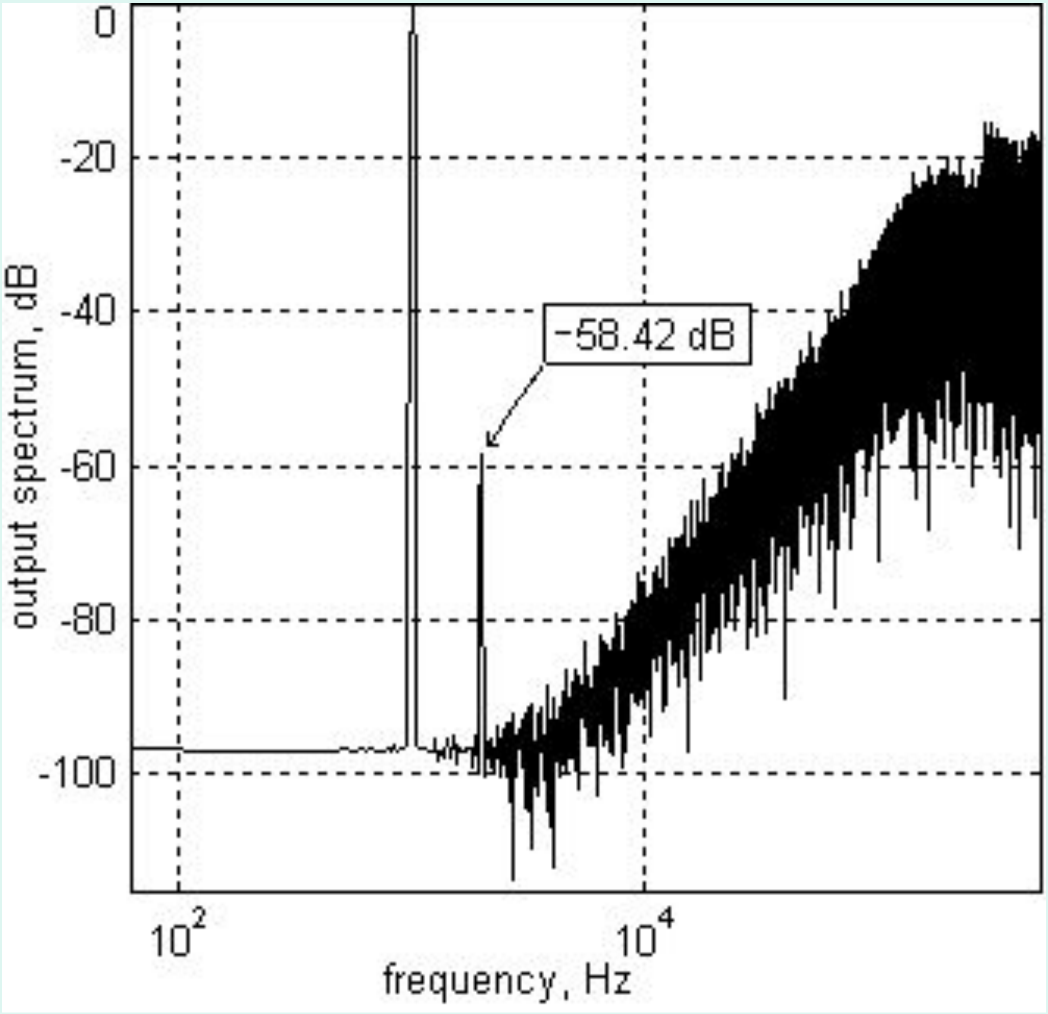


SIMULATION EXAMPLE

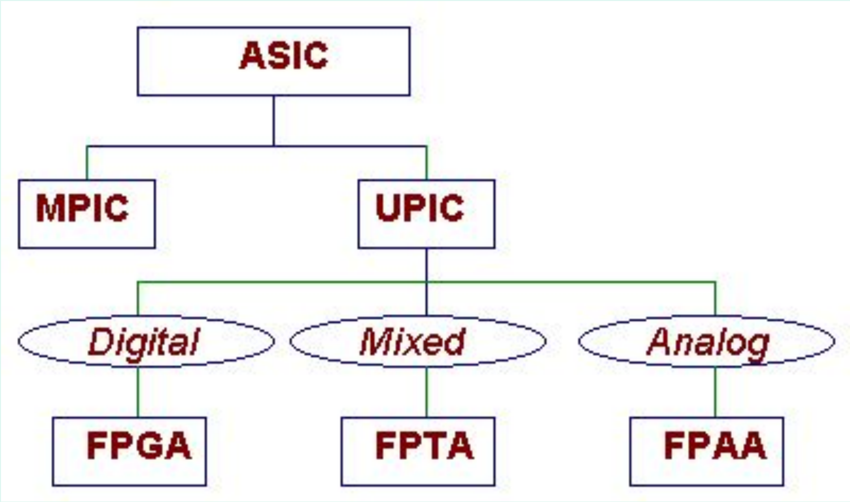


- line 1 – results of behavioral simulation using Simulink,
- line 2 – g_{on}=1 1/Ohm, ideal OpA,
- line 3 – g_{on}=1 1/Ohm, ideal OpA, sampling jitter with deviation of $0.05 \cdot 10^{-6}$ sec,
- line 4 – g_{on}=1e-4 1/Ohm, GBW=200kHz).

Simulation results of second-order ΔΣ modulator for stray capacitor nonlinearities

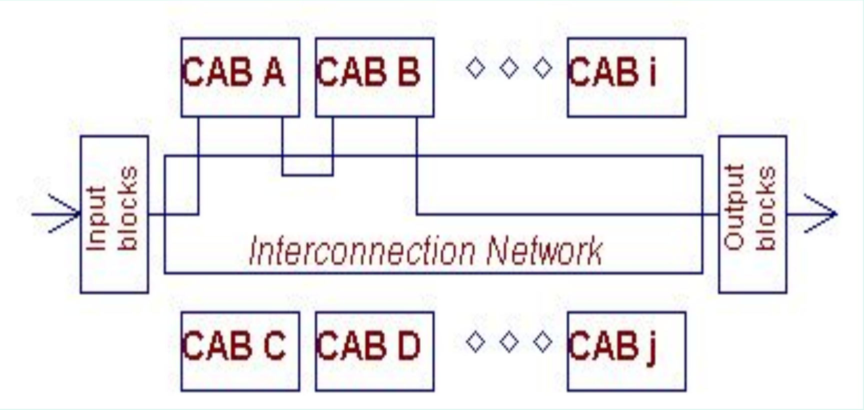


Classification of Integrated Circuits



- ASIC – Application Specific IC
- MPIC – Mask Programmed IC
- UPIC – User Programmable IC
  - *FPGA – Field Programmable Gate Array*
  - *FPTA – Field Programmable Transistor Array*
  - *FPAA – Field Programmable Analog Array*

Typical FPAA Block Diagram



- Input/Output Blocks – For Antialiasing and Smoothing purposes
- CAB (Configurable Analog Block) – For Analog Function implementation
- Interconnection Network – provides Internal Connection between CABs and I/O blocks

Main FPAA Vendors

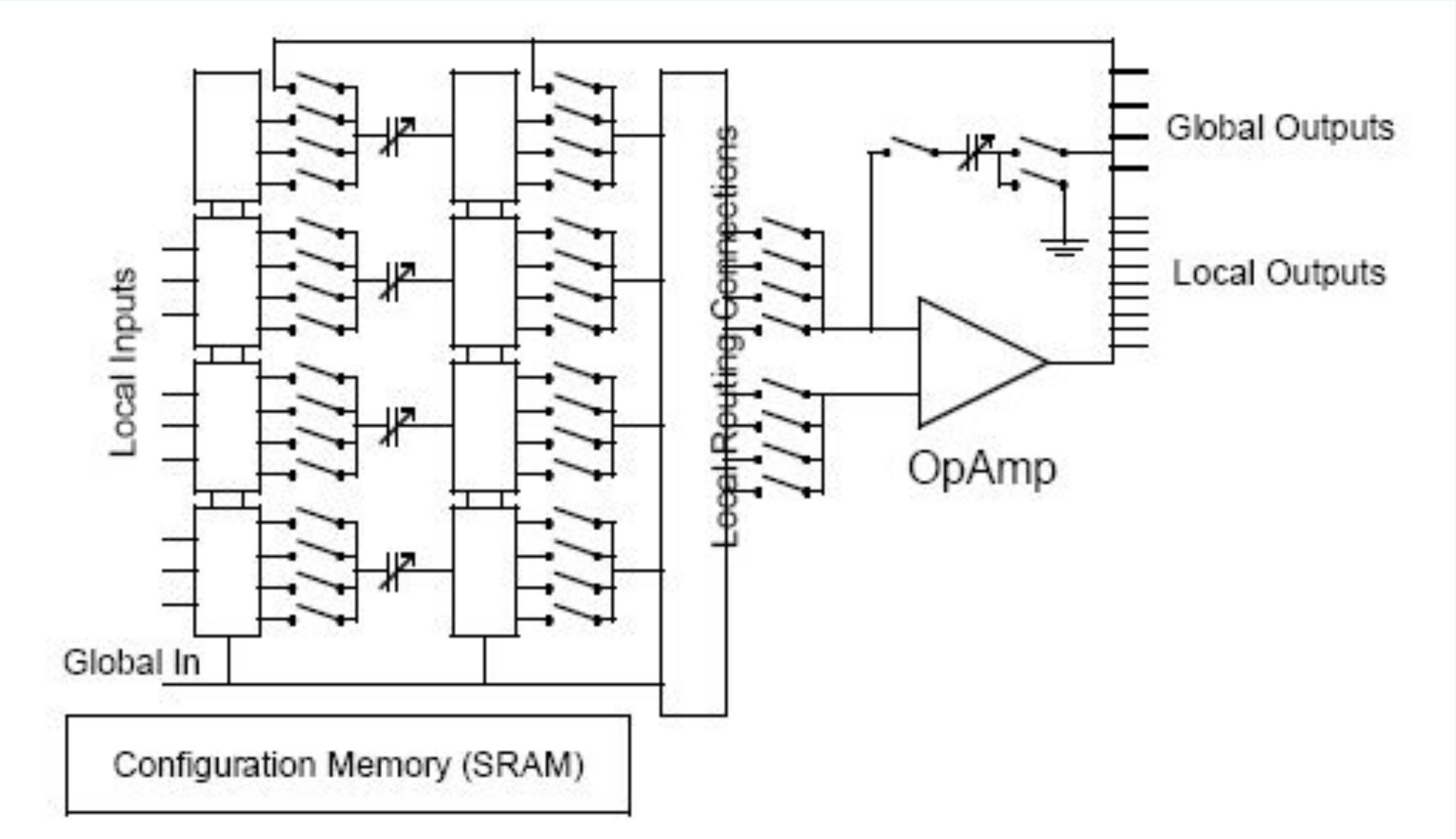
- *Anadigm* – specialized on switched capacitor ICs
- *Motorola* – specialized on switched capacitor ICs
- *Zetex* – specialized on continuous time ICs
- *Lattice semiconductor* – specialized on continuous time ICs

Basic features of FPAA's AN10E40, MPAA020,TRAC020LH and ispPAC20

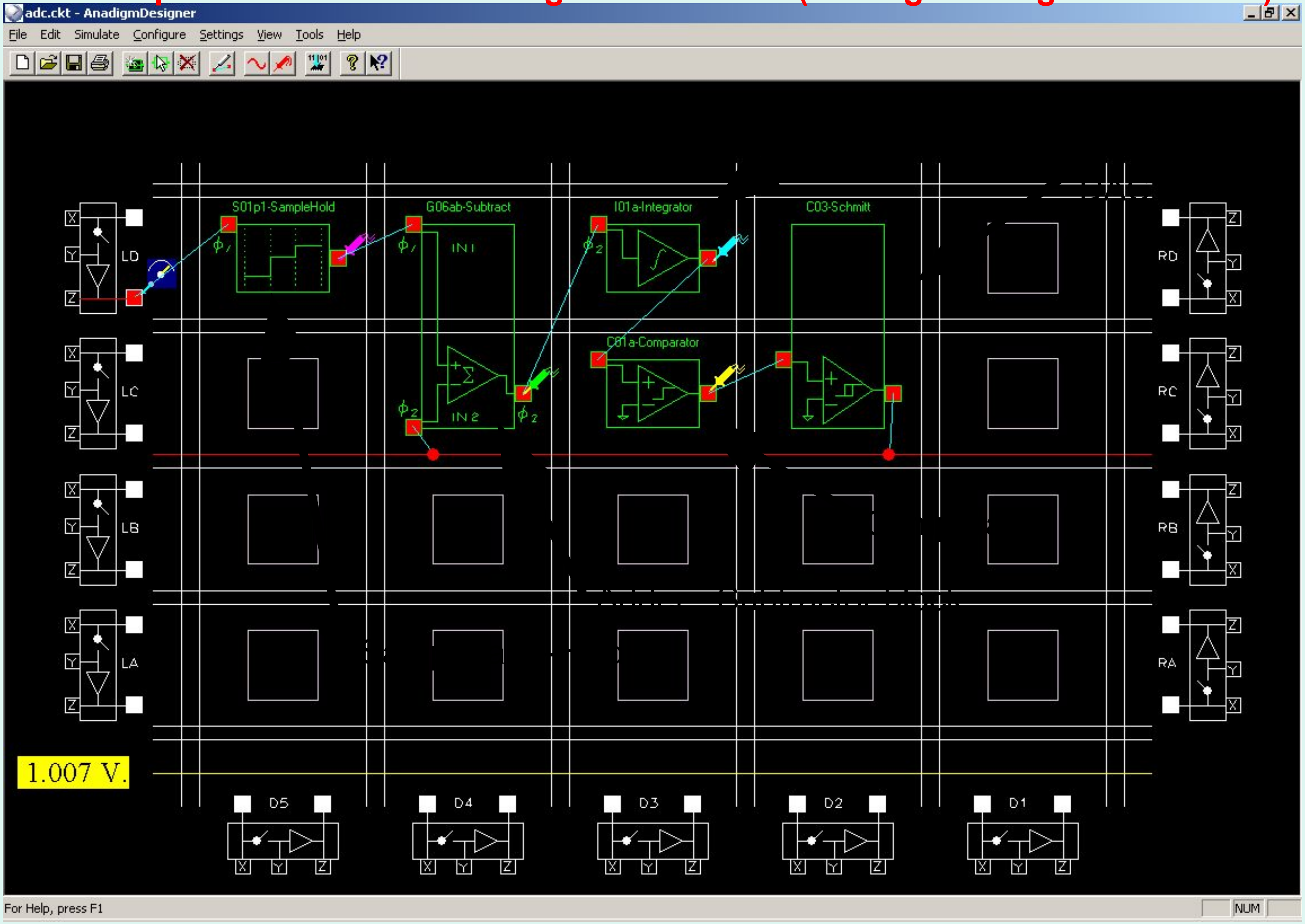
Parameter	AN10E40	MPAA020	TRAC020LH	ispPAC20
Vendor	*Anadigm*	*Motorola*	*Zetex*	*Lattice Semiconductor*
Type	SC*	SC*	CT*	CT*
DC power supply ,V	Unipolar +5	Unipolar +5	Bipolar -2 – +3	Unipolar +5
Number of Configurable Cells	20	20	20	2CAB+2 Comparators+DAC
Number of I/O Cells	13	13	----	2 CAB I/O Cells, 1 Input Comparator Cell, 2CAB Output , 2 Comparator Outputs, DAC Output
Analog Input Voltage, V	0,5-4,5	0,5-4,5	-1 – +1	1-4
3dB Bandwidth, MHz	10	----	----	----
Maximum Signal Frequency (Recommended), kHz	200	200	3 – 12 MHz	550
Slew Rate, V/μS	18	10	4	7,5

*) SC – switched capacitor circuit   CT – continuous time circuit

Anadigm's CAB Block Diagram



FPAA implementation of Delta-Sigma Modulator (Anadigm Designer Software)

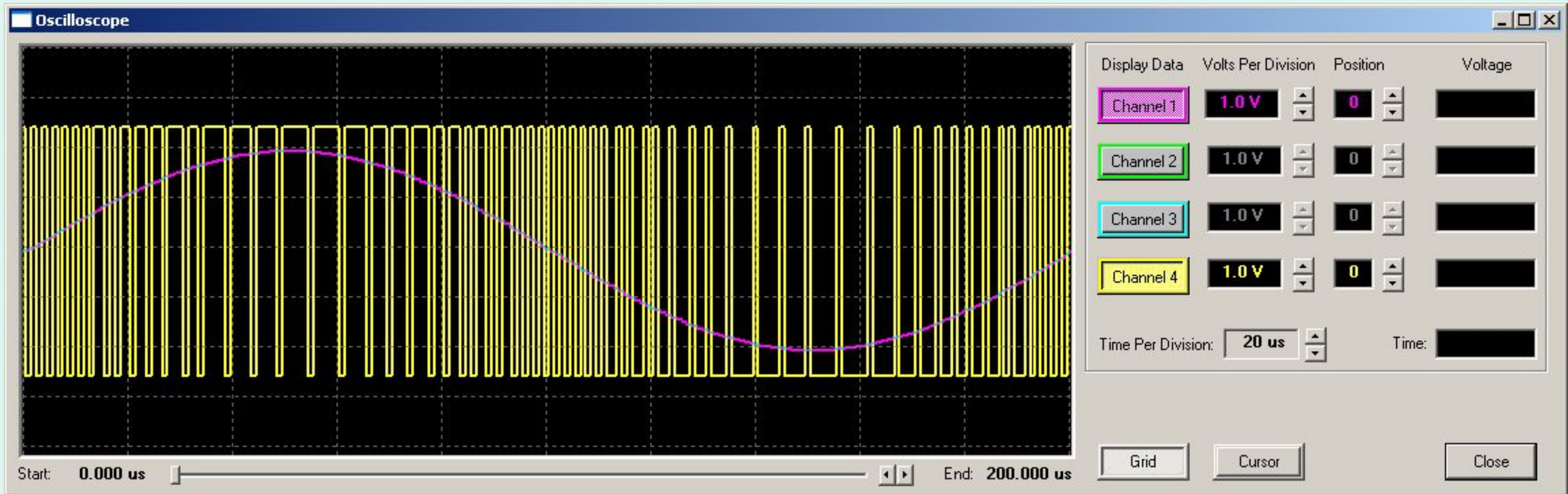


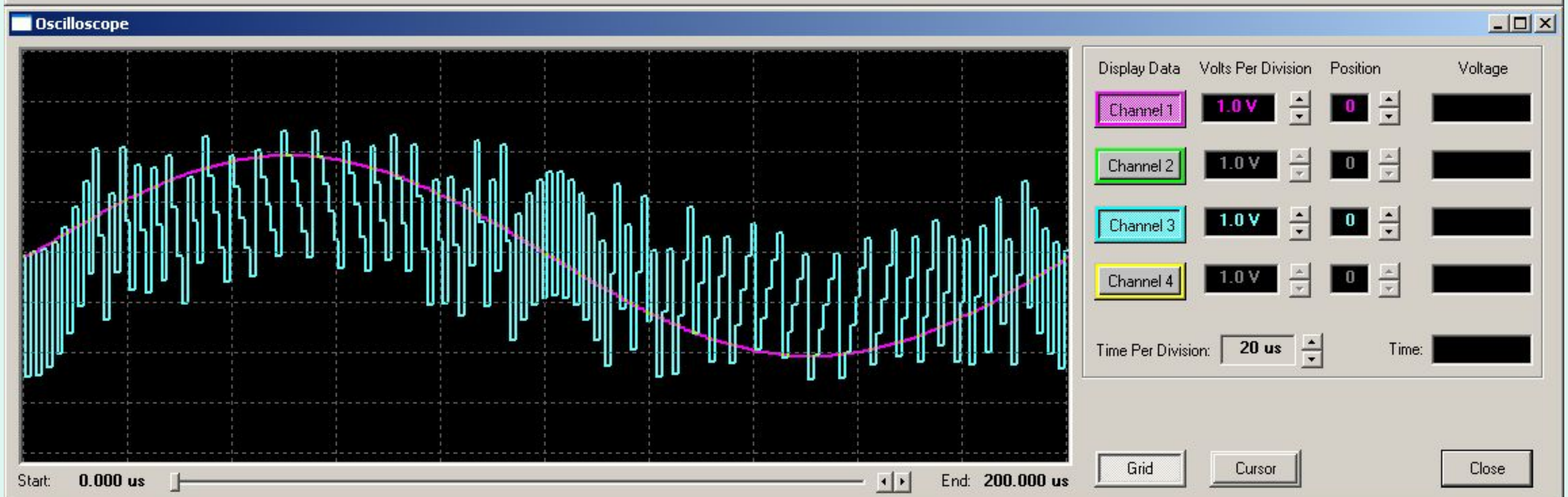
Computer Simulation

Initial Conditions

- Clock Frequency 1MHz
- Test signal Frequency 5kHz
- Amplitude of test signal 2V
- Integration Constant of Integrator 10e6/s

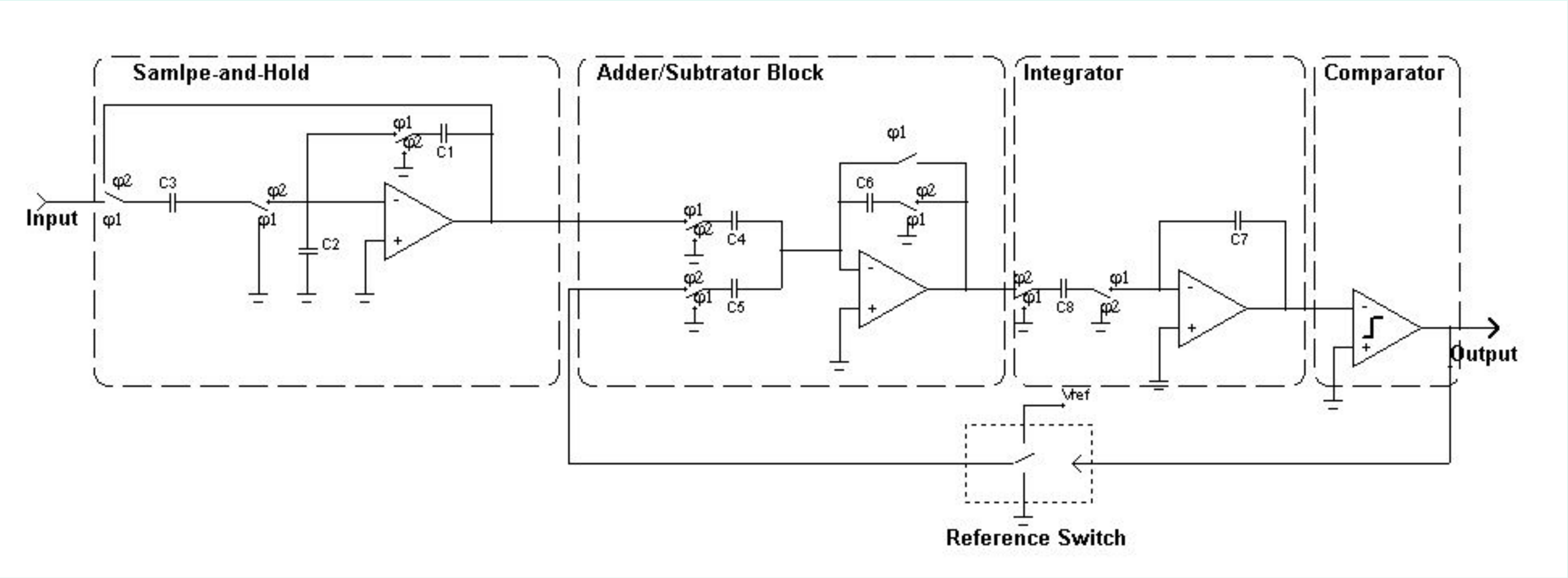
Voltage oscillogramms: output of Sample-and-Hold (Magenta), output of Delta-Sigma Modulator (Yellow), output of integrator (Blue)



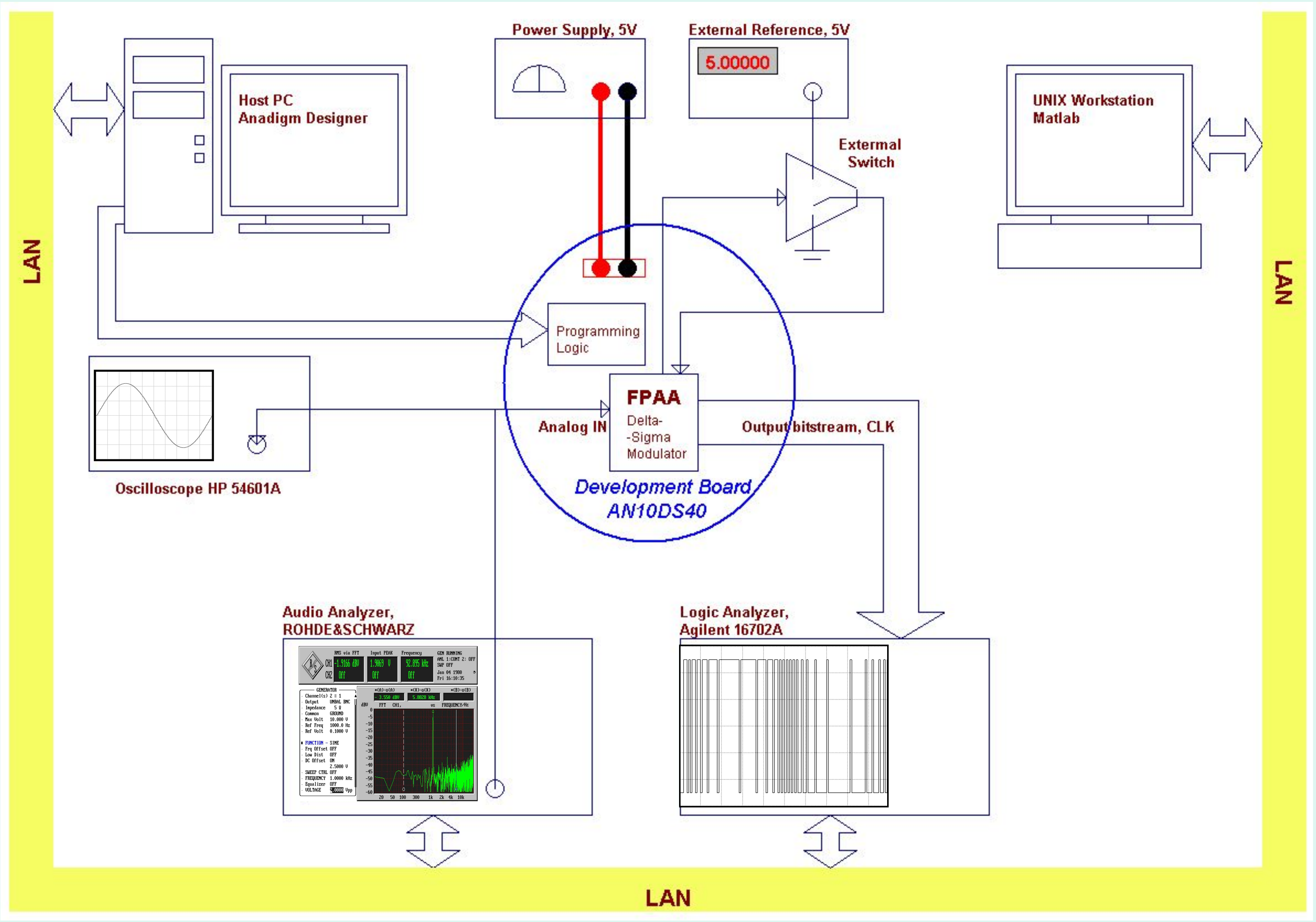


*Anadigm Desigmer Software

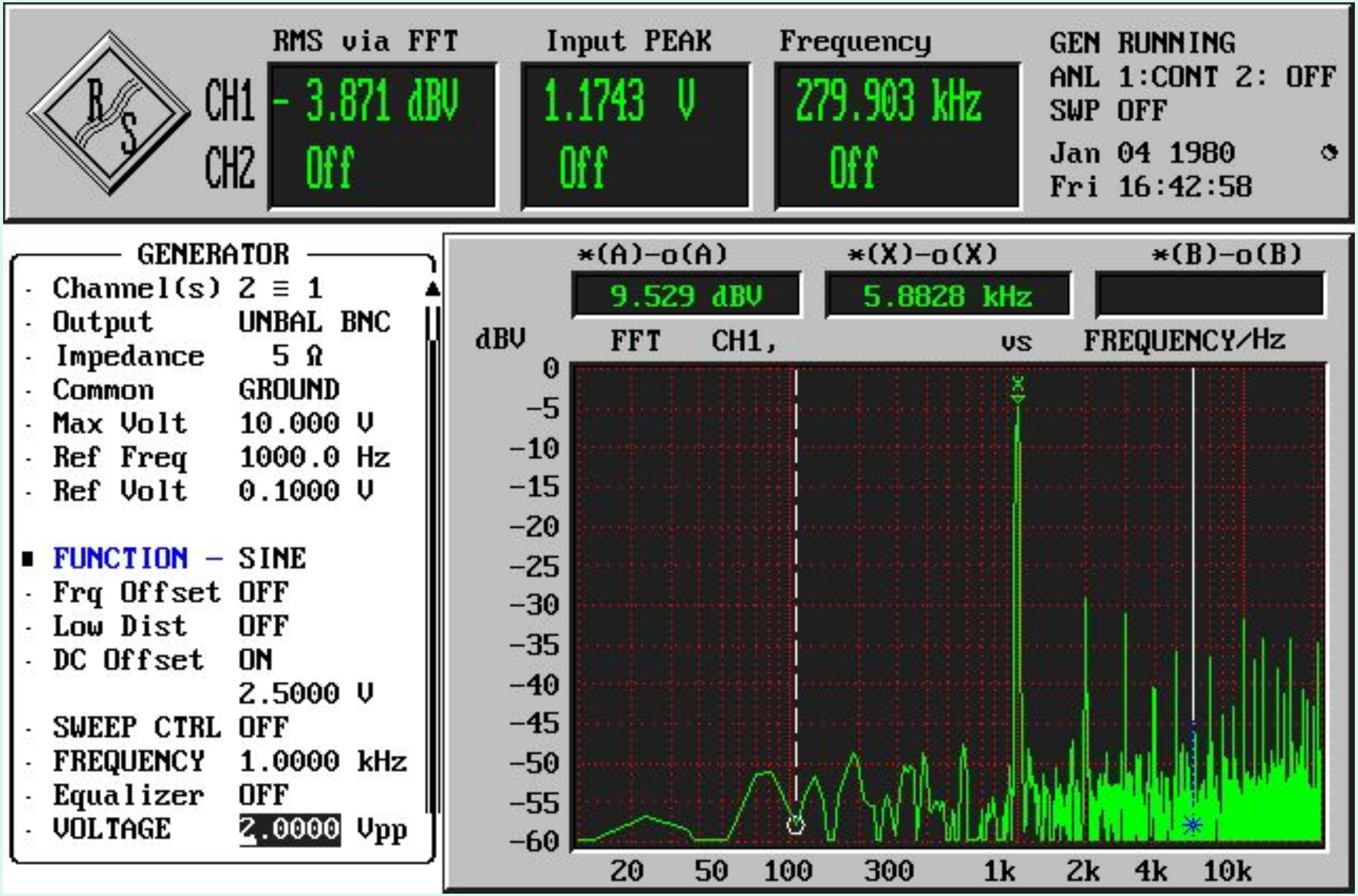
Switched Capacitor Schematic of 1-st Order Delta-Sigma Modulator based on FPAA



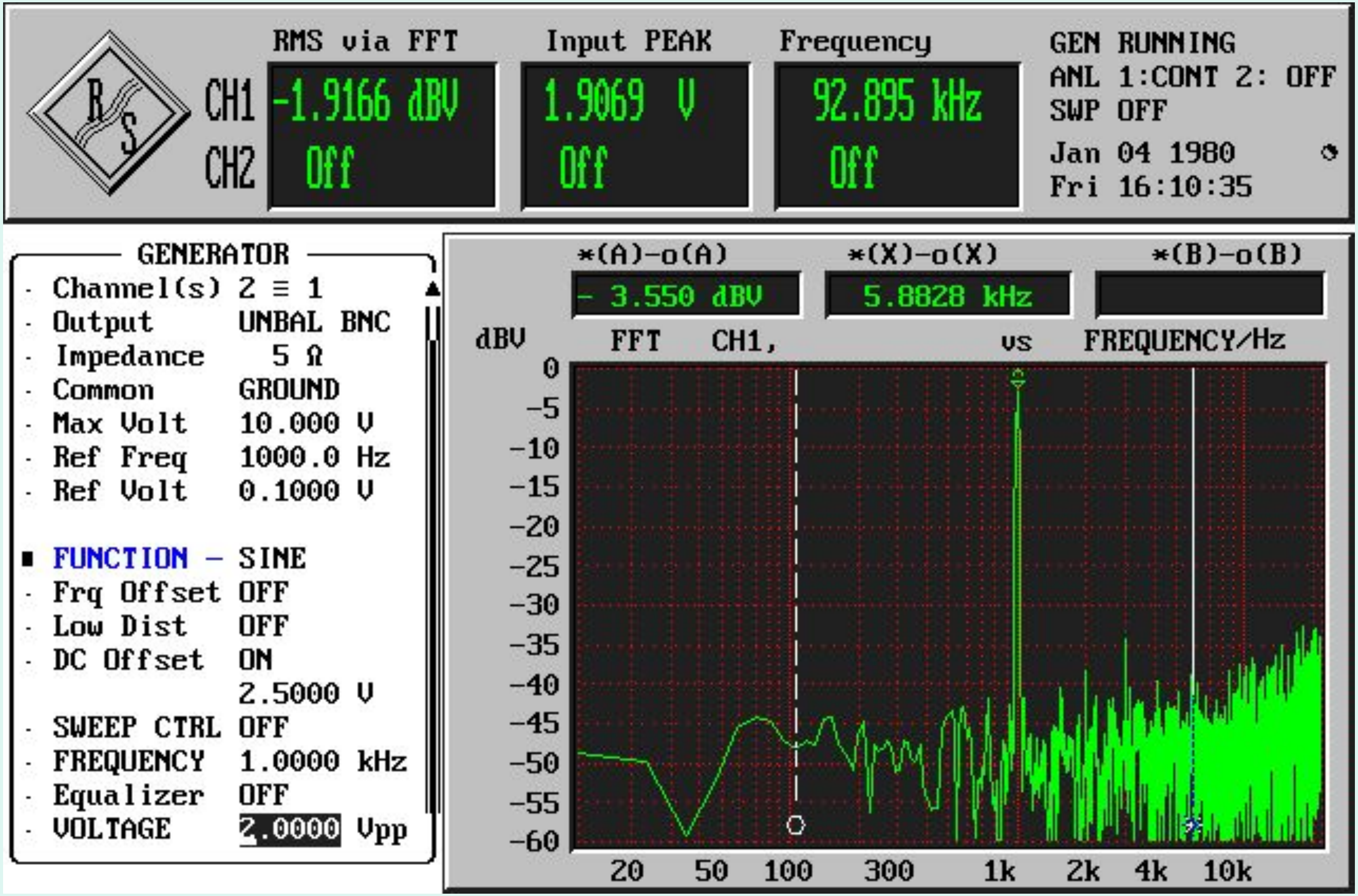
Measuring Scheme

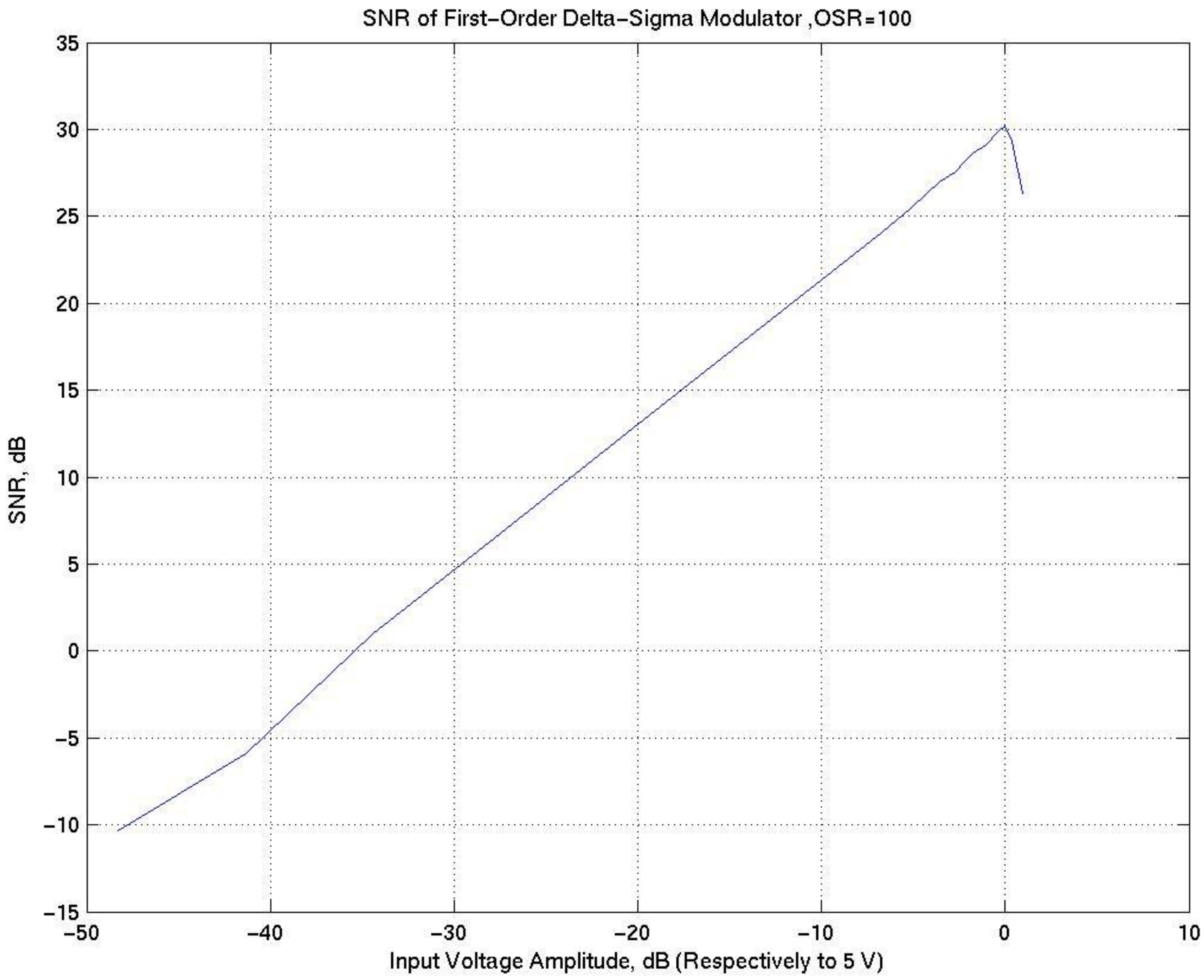


Output signal spectrum of 1-st order Delta-Sigma Modulator with 1Mhz clock frequency



Output signal spectrum of 1-st order Delta-Sigma Modulator with 250kHz clock frequency




SNR of First-Order Delta-Sigma Modulator ,OSR=100
SNR, dB
Input Voltage Amplitude, dB (Respectively to 5 V)
35
30
25
20
15
10
5
0
−5
−10
−15
−50
−40
−30
−20
−10
0
10

Conclusions

1. Proposed approaches are perspective and can be used for the CMOS design of selective circuits for wireless communication systems.

2. Characteristics of the synthesized filters correspond to practical requirements.

3. Main advantages of the circuits are their low supply voltage and power consumption as well as their small sizes and good compatibility with CMOS technology.

CONCLUSIONS

4. Simulation program has been proposed for analysis of oversampled switched-capacitor Delta-Sigma modulator.
5. The developed program is based on direct circuit response calculation using nodal approach with matrix presentation of circuits in the frequency domain and Volterra series method.
6. The program is written in MATLAB and allows
   – analysis of switched-capacitor circuit taking into account non-ideal imperfections including limited switch resistances and gain-bandwidth product of active devices.
   – analysis of switched-capacitor circuit taking into account nonlinear parasitic capacitance of switches and active elements dynamic limitations

CONCLUSIONS

- Delta-Sigma modulator has been realized on a basis of FPAA Anadigm AN10E40;
- For the proposed design the Dynamic Range is not more than 40 dB and the Frequency Range is about 20 kHz;
- The limiting factors:
  - OSR not more than 100. It depends on FPAA properties;
  - Properties of comparator;
  - Possibly, schematic of the integrators as well.

References

- **[1] D.V.Morozov and A.S.Korotkov, "A realization of low-distortion CMOS transconductance amplifier;"** ***IEEE Trans. Circuits Syst.-I*****, vol.48, pp.1138-1141, Sept. 2001.**
- **[2] A.S.Korotkov, D.V.Morozov, and R.Unbehauen, "Low-voltage continuous time filter based on a CMOS transconductor with enhanced linearity,"** ***Int. J. Electronics and Comm*****. (*****AEÜ*****), vol.56, no.6, pp.416- 420, Dec. 2002.**
- **[3] A.S.Korotkov, D.V.Morozov, H.Hauer, and R.Unbehauen, "A 2.5-V, 0.35 um CMOS transconductance-capacitor filter with enhanced linearity," In** ***Proc. MWSCAS'02*****, Tulsa, USA, vol.3, pp.141- 144, Aug. 2002.**
- **[4] A.A.Tutyshkin, A.S.Korotkov, "Current conveyor based switched-capacitor integrator with reduced parasitic sensitivity," in** ***Proc 1st IEEE ICCSC'02*****, St.Petersburg, Russia, pp.78- 81, June 2002.**
- **[5] A.S.Korotkov, D.V.Morozov, A.A.Tutyshkin, H.Hauer and R.Unbehauen, "Design of a CMOS high frequency current conveyor based switched-capacitor filter with low power consumption," in** ***Proc. MWSCAS'03*****, Cairo, Dec. 2003.**

THANK YOU