LIN protocol description

LOCAL INTERCONNECT NETWORK

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Automotive Body Network
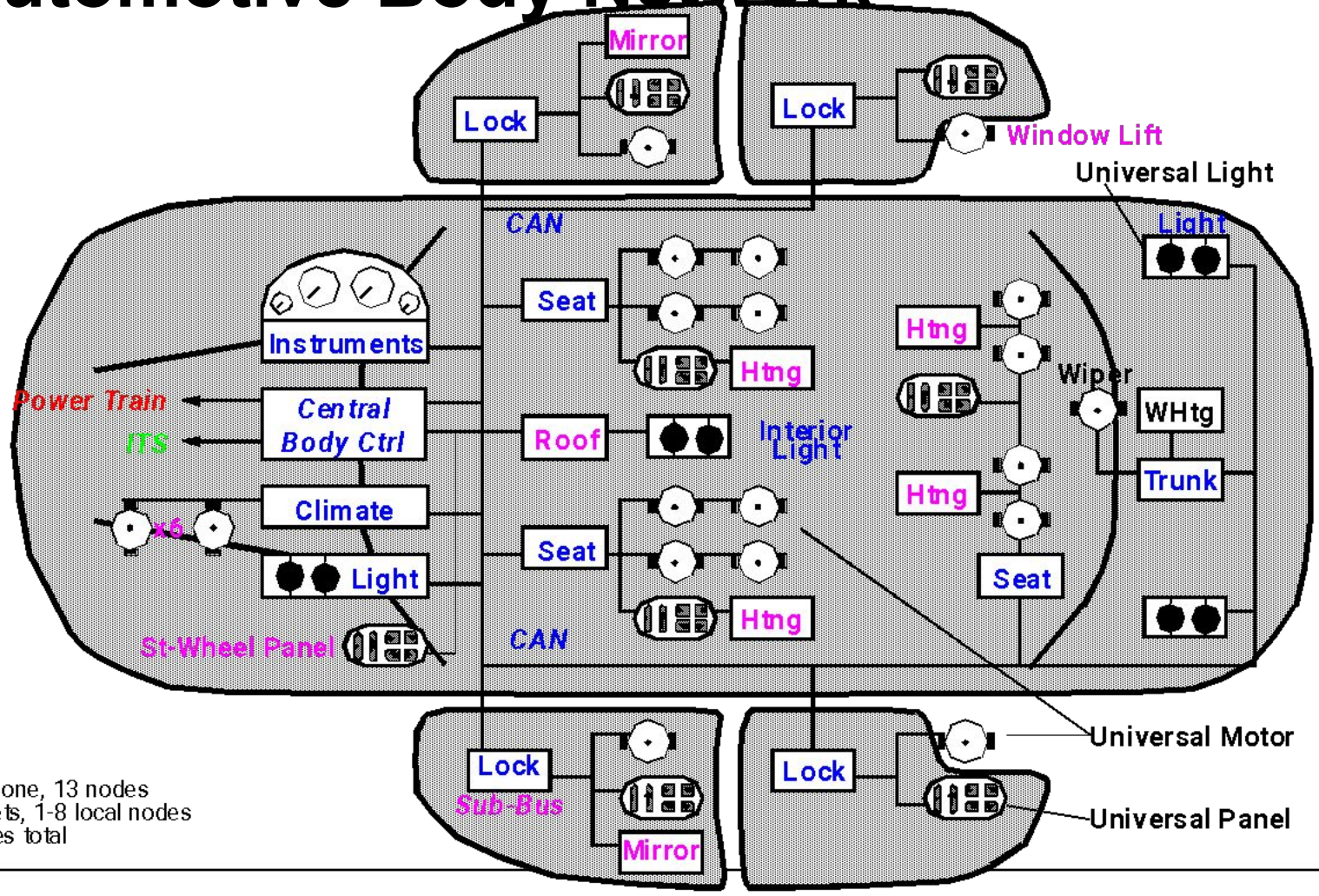
1 backbone, 13 nodes
8 subnets, 1-8 local nodes
52 nodes total

LIN / µ Bus
W. Specks, A. C. Wense

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Typical LIN Applications

Roof:
(high amount of wiring)
   Rain Sensor, Light Sensor,
   Light Control, Sun Roof
   …
   (Rain Sensor needs to be
   interrogated every 10-20ms)

Steering Wheel:
(very many controls are going to be
positioned on the steering wheel)
   Cruise Control, Wiper,
   Turning Light, …
   Optional: Climate Control,
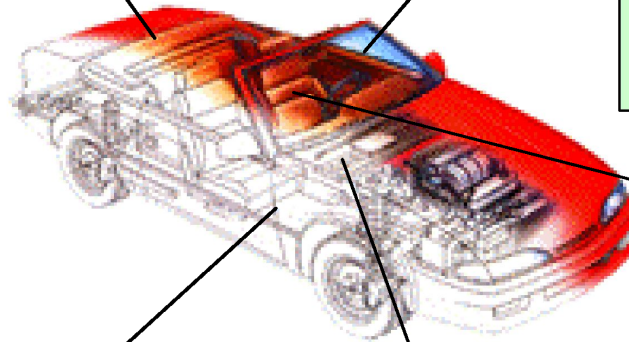   Radio, Telephone, etc.

Seat:
   many Seat Position Motors,
   Occupancy Sensor,
   Control Panel

• **Door/window/seat:**
   Mirror,Central ECU,
   Mirror, Switch, Window
   Lift,
   Seat Control Switch,
   Door Lock, etc.

Climate:
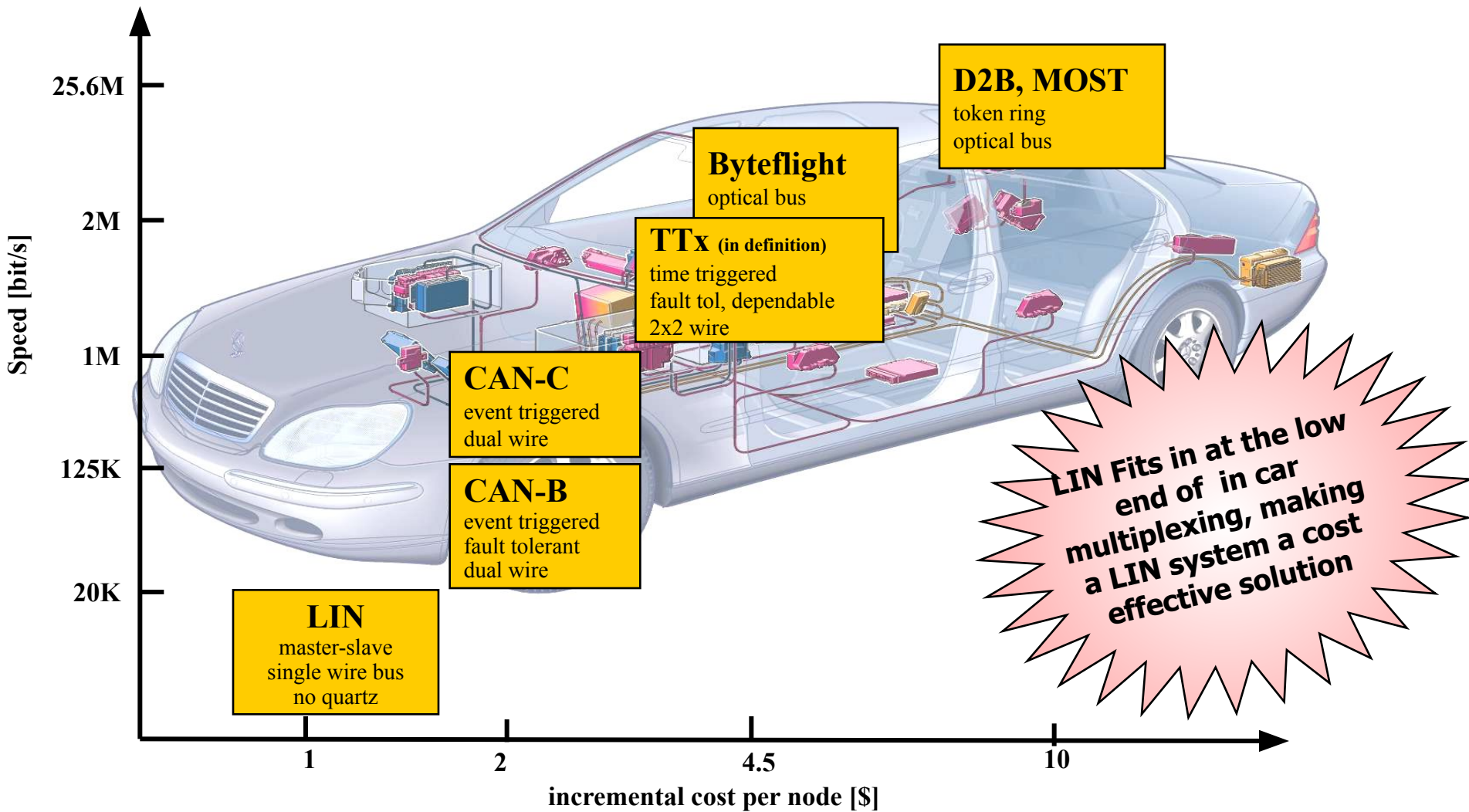   many Small Motors
   Control Panel

MUX Standards (Costs and Speeds)

Speed [bit/s]

- 25.6M
- 2M
- 1M
- 125K
- 20K

D2B, MOST
token ring
optical bus

Byteflight
optical bus

TTx (in definition)
time triggered
fault tol, dependable
2x2 wire

CAN-C
event triggered
dual wire

CAN-B
event triggered
fault tolerant
dual wire

LIN
master-slave
single wire bus
no quartz

LIN Fits in at the low end of in car multiplexing, making a LIN system a cost effective solution

incremental cost per node [$]

- 1
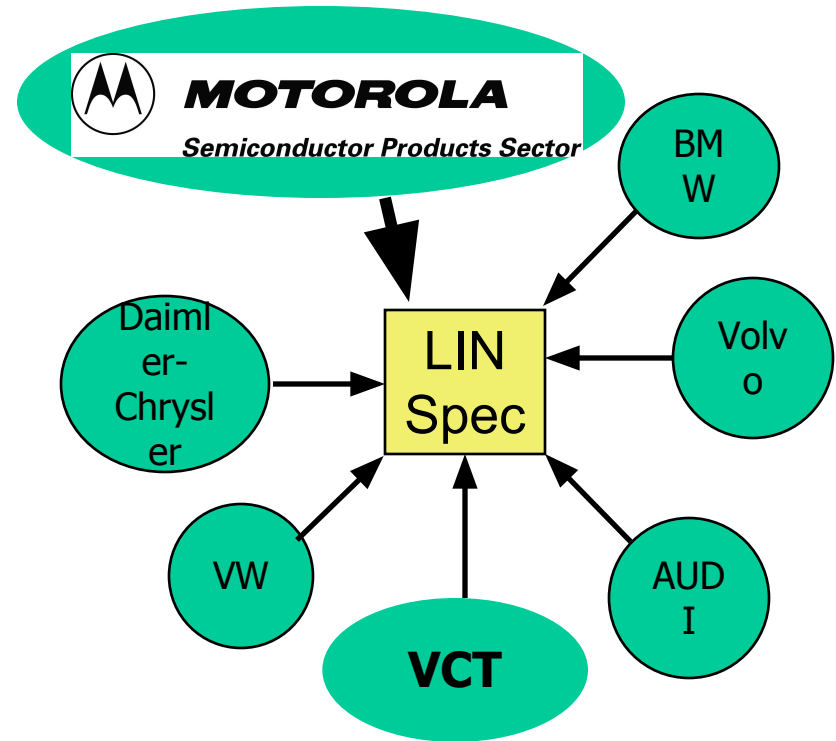- 2
- 4.5
- 10

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LIN Consortium

Consortium formed in 1998.
Five Car manufacturers
ONE Semiconductor Supplier (Motorola)
One tool Supplier (VCT)

Specification finalised on 02/02/00
Official Launch at SAE March '00
Open Specification.

Motorola Ready to support LIN with
    extensive
device families and new parts already in the
discussion/ spec finalization loop.
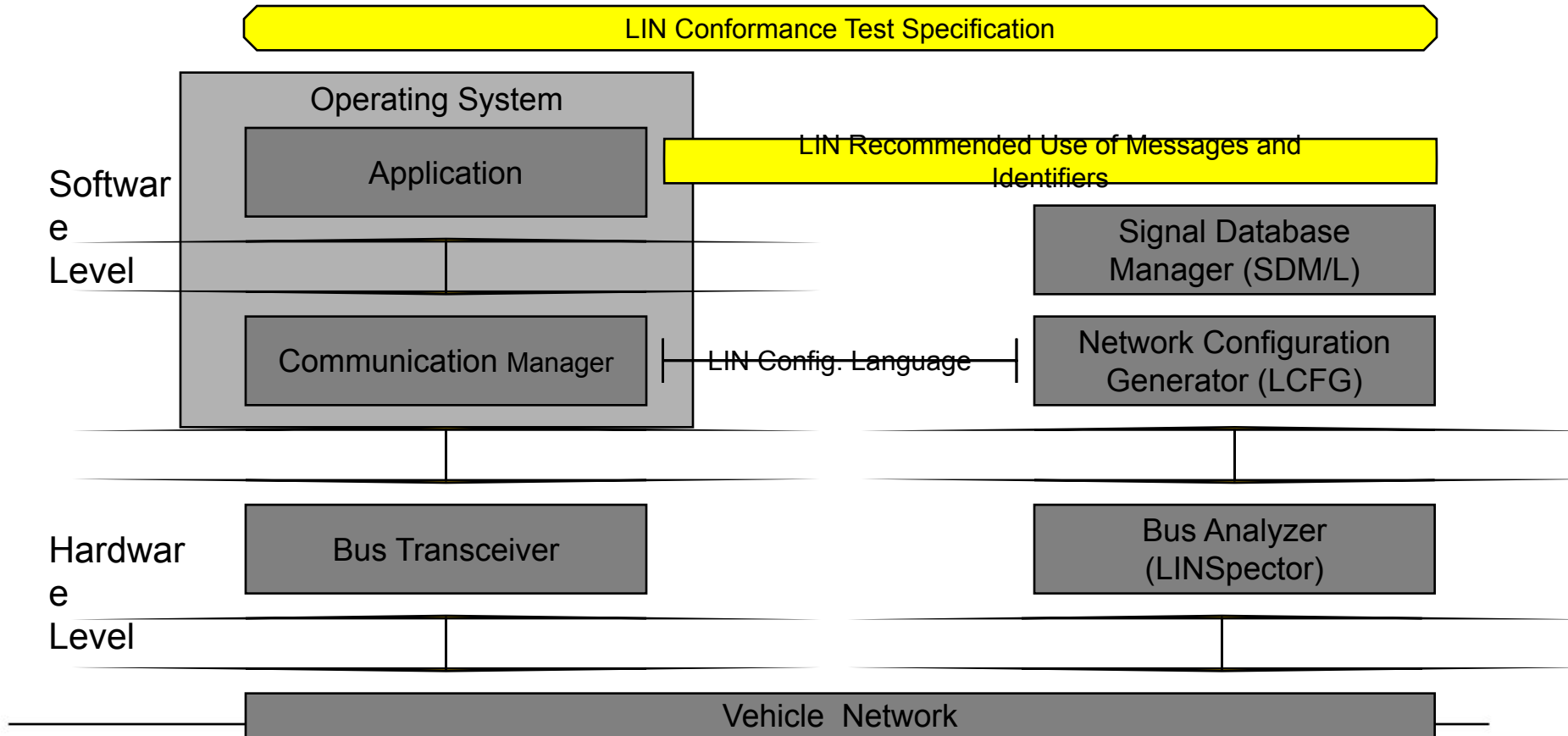First dedicated LIN part available Q3 '00

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Semiconductor Products Sector

BMW

Volvo

Daimler-Chrysler

LIN Spec

VW

VCT

AUDI

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LIN Standard - Overview

ECU
(LIN relevant
functions only)

Tools

Software Level

Hardware Level

LIN Conformance Test Specification

Operating System

Application

LIN Recommended Use of Messages and Identifiers

Signal Database Manager (SDM/L)

Communication Manager

LIN Config. Language

Network Configuration Generator (LCFG)

Bus Transceiver

Bus Analyzer (LINSpector)

Vehicle Network

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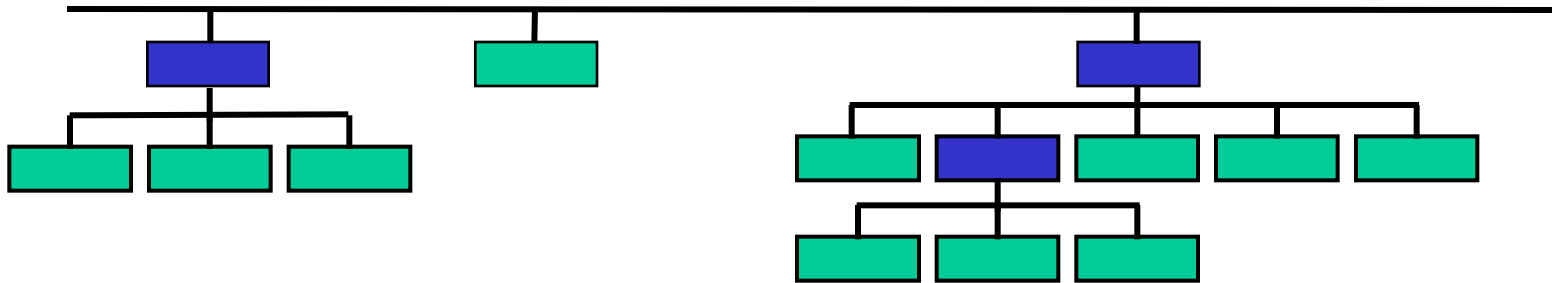intelligence everywhere

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Hierarchical Network Structure

Flat Network

Hierarchical Network

- Subnets are necessary to reduce Busload on main Bus

- Solution examples:

• **CAN**
+Automotive Standard Bus
+Compatible with Main Bus
-Expensive (Die Size/ Dual Wire)

- **Serial Sub Bus**

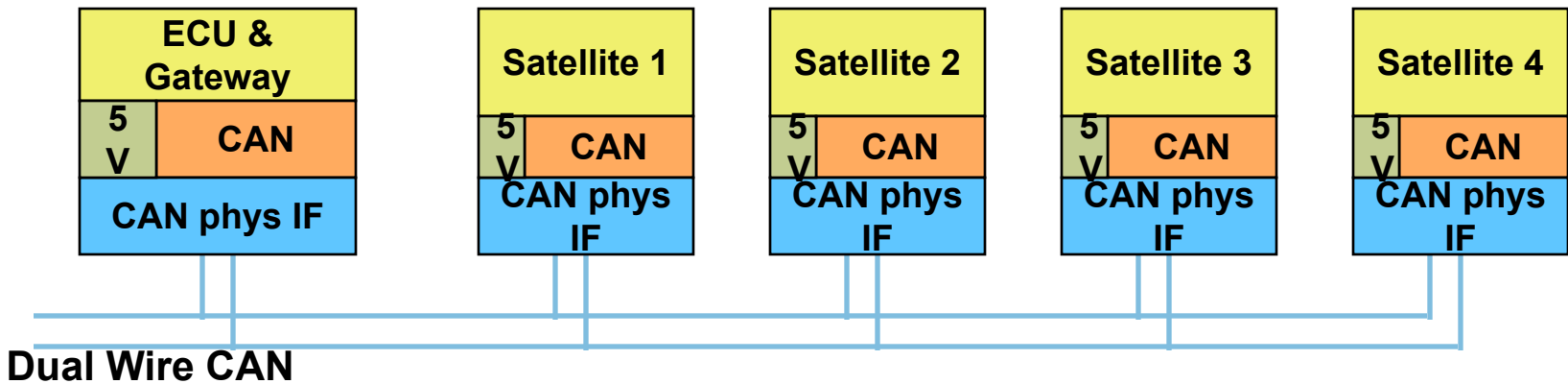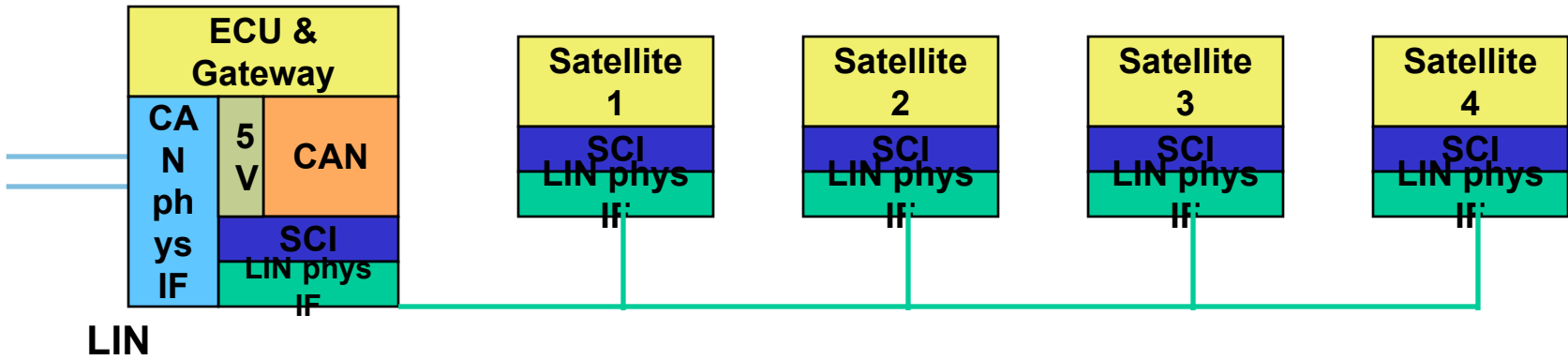| - no standard Bus System |
|---|
| - not compatible with Main Bus |
| + inexpensive |
| + SCI-Based: Interface exists even on cheap devices |
| + Interface can easily be reconstructed by ASIC or CPLD |

+ Protocol can be done in Software

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Sub-Network: LIN vs. CAN

LIN

ECU & Gateway				Satellite 1	Satellite 2	Satellite 3	Satellite 4

(LIN network: ECU & Gateway with CAN phys IF, 5V, CAN, SCI, LIN phys IF connected to Satellite 1–4 each with SCI and LIN phys IF)

Dual Wire CAN

(Dual Wire CAN network: ECU & Gateway with 5V, CAN, CAN phys IF connected to Satellite 1–4 each with 5V, CAN, CAN phys IF)

Cost Factors: CAN Module   Dual Wire Interface

Crystal   5V supply for bus

2nd Wire / Connector

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SubNets

- Necessary to reduce Busload on main Bus
- Solutions
  - **CAN**
    - + **Automotive Standard Bus**
    - + **Compatible with Main Bus**
    - - **Expensive (Die Size/ Dual Wire)**
  - **Serial Sub Bus**
    - - **no standard Bus System**
    - - **not compatible with Main Bus**
    - + **inexpensive**
    - + **SCI-Based: Interface exists even on cheap devices**
    - + **Interface can easily be reconstructed by ASIC or CPLD**

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Sub Bus Concept

- Basic Requirements:
  - **Satisfy Need for a Standard for Sub Busses**
  - **Cost driven: The solution must be cheaper than CAN**
  - **Reliability: Same Level as CAN expected**
  - **Long Term Solution**
  - **Logical Extension to CAN**
  - **Scalable: Capability to extend Systems with additional nodes**
  - **Lowering Cost of Satellite nodes:**
    - **No Crystal or Resonator**
    - **Easy implementation**
    - **Simple State Machines**
  - **Low Reaction Time (100 ms max)**
  - **Predictable Worst Case Timing**

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LIN Concept

- Technical Solution
  - Low cost single-wire implementation (enhanced ISO 9141)
  - Speed up to 20Kbit/s (limited for EMI-reasons)
  - Single Master / Multiple Slave Concept
    - → No arbitration necessary
  - Low cost silicon implementation based on common UART/SCI interface hardware
    - → Almost any Microcontroller has necessary hardware on chip
  - Self synchronization without crystal or ceramics resonator in the slave nodes
    - → Significant cost reduction of hardware platform
  - Guaranteed latency times for signal transmission (Predictability)

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Master / Slave Protocol

- ## Master Task
  - **Determines order and priority of messages.**
  - **Monitors Data and check byte and controls the error handler.**
  - **Serves as a reference with its clock base (stable clock necessary)**
  - **Receives Wake- Up Break from slave nodes**

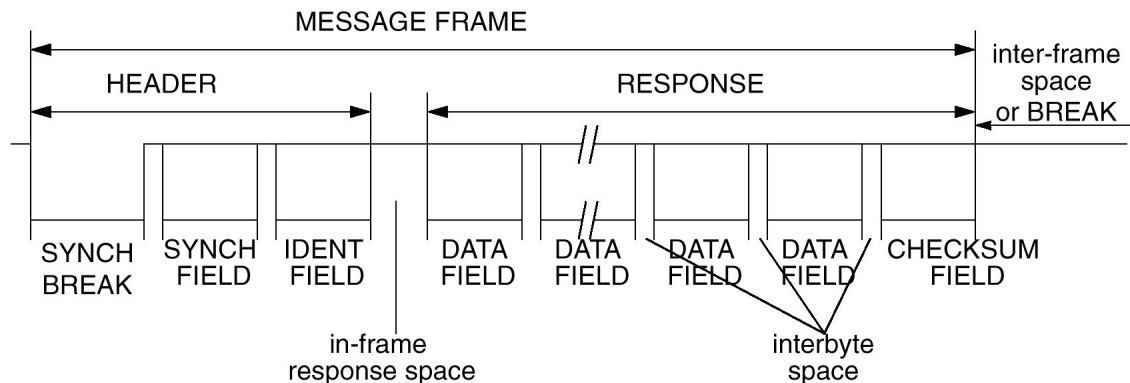- ## Slave Task
  - **Is one of 2-16 members on the bus**
  - **Receives or transmits data when an appropriate ID is sent by the master.**
  - **The node serving as a master can be slave, too!**

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Master / Slave Protocol

- Master
  - **has control over the whole Bus and Protocol
    The master controls which message at what time is to be
    transferred over the bus. It also does the error handling.
    To accomplish this the master**
    - **sends Sync Break**
    - **sends Sync Byte**
    - **sends ID-Field**
    - **monitors Data Bytes and Check Byte, and evaluates them on consistance**
    - **receives WakeUp Break from slave nodes when the bus is inactive and they request some action.**
    - **serves as a reference with it's clock base (stable clock necessary)**

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Master/Slave Protocol

- Slave
  - **Is one of 2-16 Members on the Bus and receives or transmits Data when an appropriate ID is sent by the master.**
    - **Slave snoops for ID.**
    - **According to ID, slave determines what to do.**
      - **either receive data**
      - **or transmit data**
      - **or do nothing.**
    - **When transmitting the slave**
      - **sends 1, 2, 4, or 8 Data Bytes**
      - **sends Check-Byte**
    - **The node serving as a master can be slave, too!**

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... protocol offers message timing predictability

Time Triggered Approach

- Message Length is known
    - **Number of transmitted data bytes is known**
        - → **minimum length can be calculated**
    - **Each Message has length budget of 140% of it's minimum length**
        - → **maximum allowed length is known**
        - → **distance between beginning of two messages**

Data Transmission

13 bit Break

synch field $55

identifier field

Next 13 bit break

Master Task

time

response spacing

2 byte data

1 byte block parity

Slave Task

time
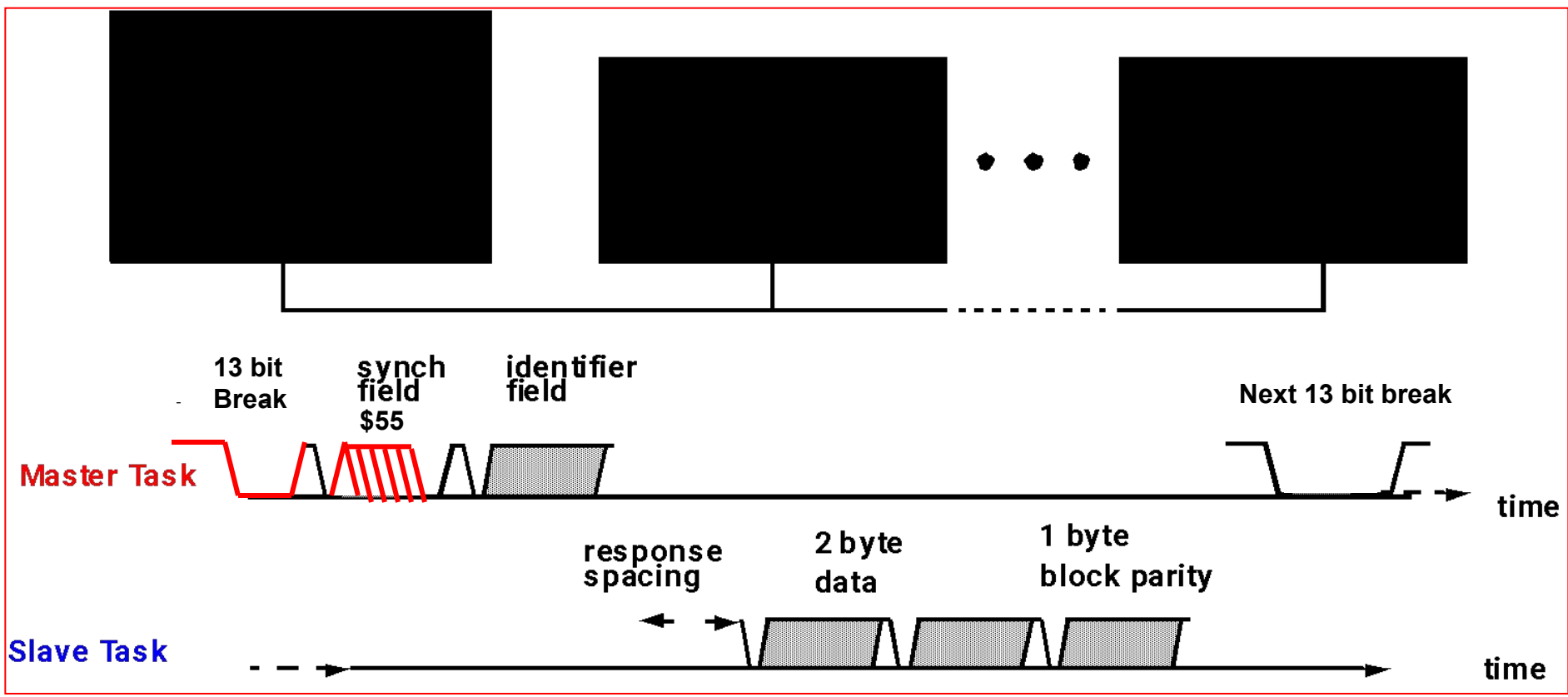
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Message Frame

- Synch Byte:
  - **Specific Pattern for Determination of Time Base (Determination of the time between two rising edges)**
  - **A Synch Byte precedes any Message Frame**

- ID-Field:
  - **Message Identifier: Incorporates Information about the sender, the receiver(s), the purpose, and the Data field length. Length 6 Bit. 4 classes of 1/2/4/8 Data Bytes. The length coding is in the 2 LSB of the ID-Field. Each class has 16 Identifiers. A total of 64 Message Identifiers are possible.**
  - **2 Parity Bits protect this highly sensitive ID-Field.**

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Identifier

- The identifier field is sent by the master node to all LIN nodes
- This identifier normally contains one of 64 different values and includes 2 parity bits in the 8 bit data
- The identifier is normally associated with a collection of signals that are subsequently transmitted on the LIN bus
- In a specific case this can initiate SLEEP mode in the LIN slave nodes – in this case no further data is transmitted on the LIN bus
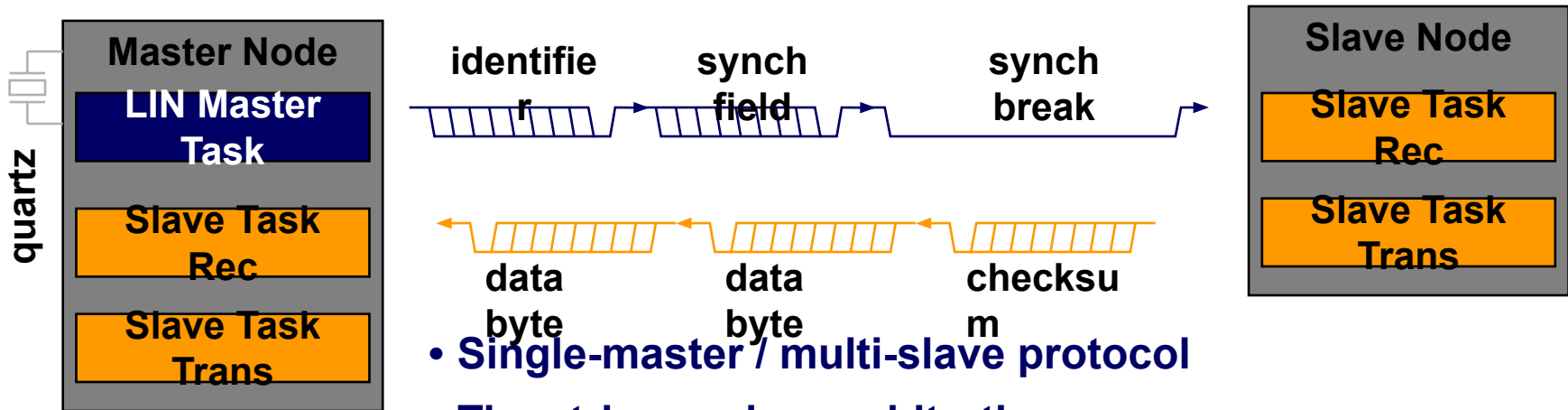
message header

synch break ≥ 13 bit   **synch field**   **identifier**

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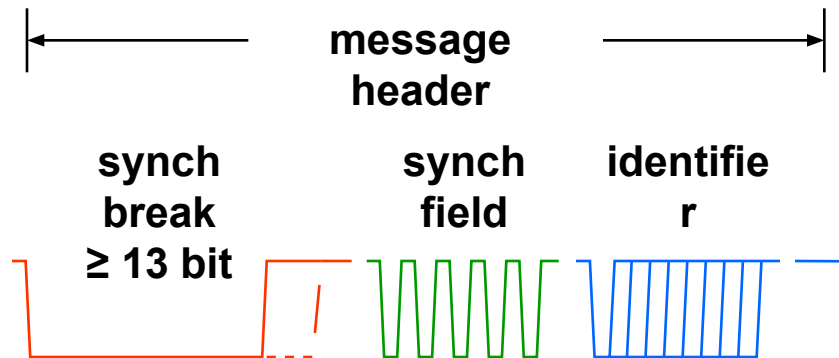
LIN Message Frame
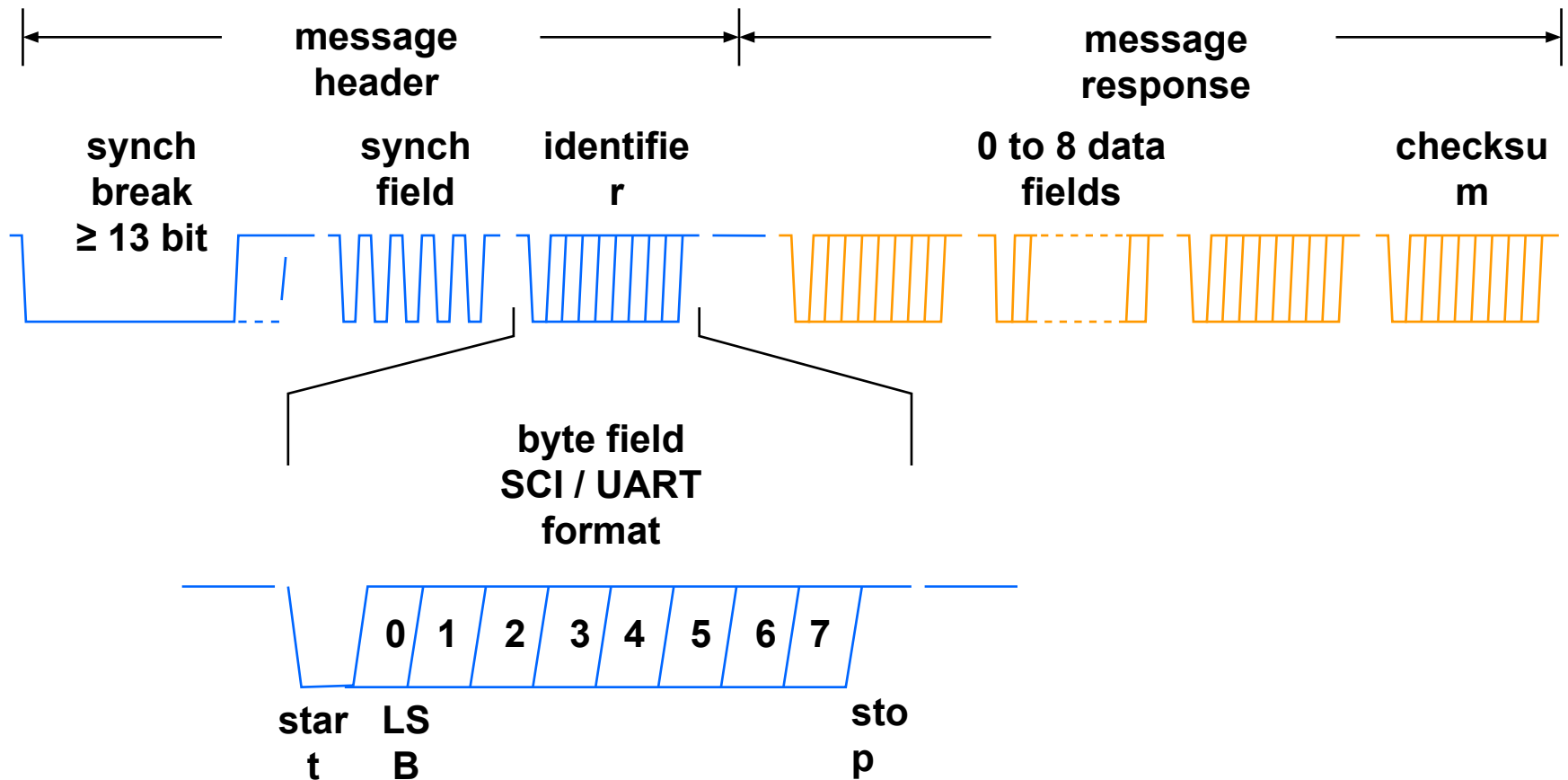
LIN Communication - Data from Slave to Master

Master Node
- LIN Master Task
- Slave Task Rec
- Slave Task Trans

quartz

identifier → synch field → synch break →

data byte ← data byte ← checksum

Slave Node
- Slave Task Rec
- Slave Task Trans

- **Single-master / multi-slave protocol**
- **Time triggered, no arbitration**
- **Identifier denotes message content, not physical address**
- **Multicast messages**
- **Baud rate synchronization through protocol**
- **Power saving sleep mode**

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LIN Communication - Data from Master to Slave(s)
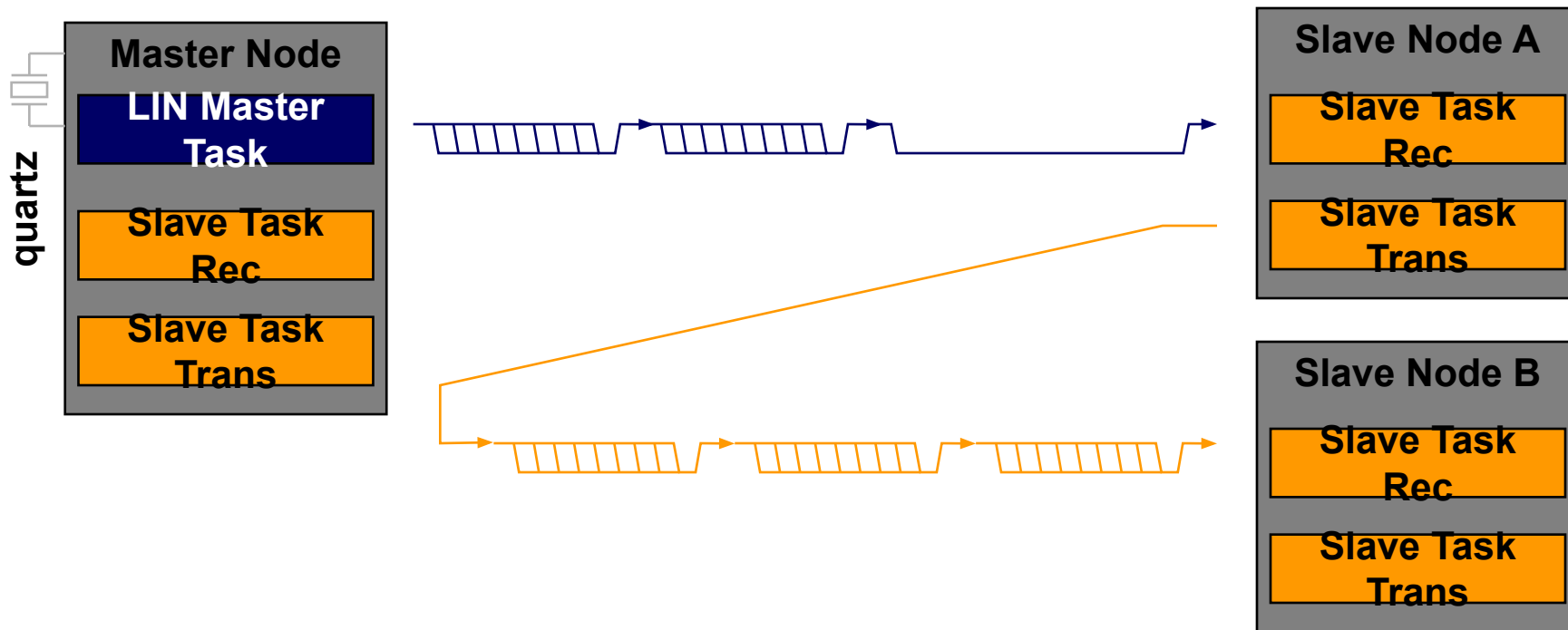
LIN Communication - Data from Slave to Slave

Master Node
- LIN Master Task
- Slave Task Rec
- Slave Task Trans

quartz

Slave Node A
- Slave Task Rec
- Slave Task Trans

Slave Node B
- Slave Task Rec
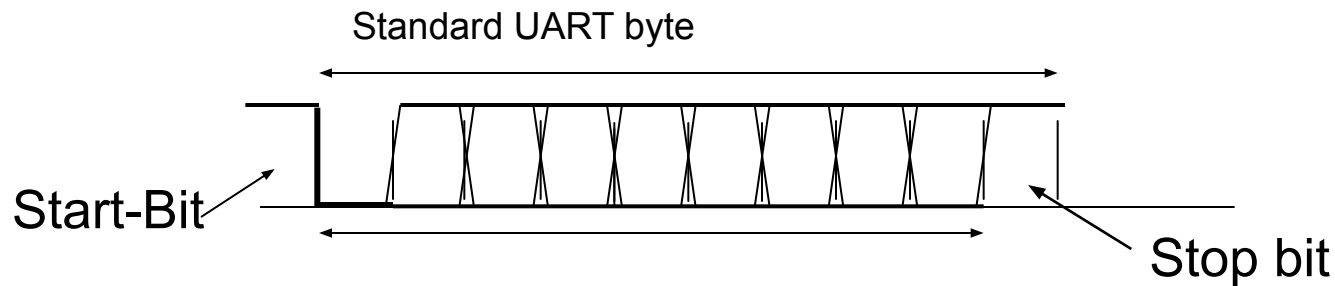- Slave Task Trans

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LIN Message Frame
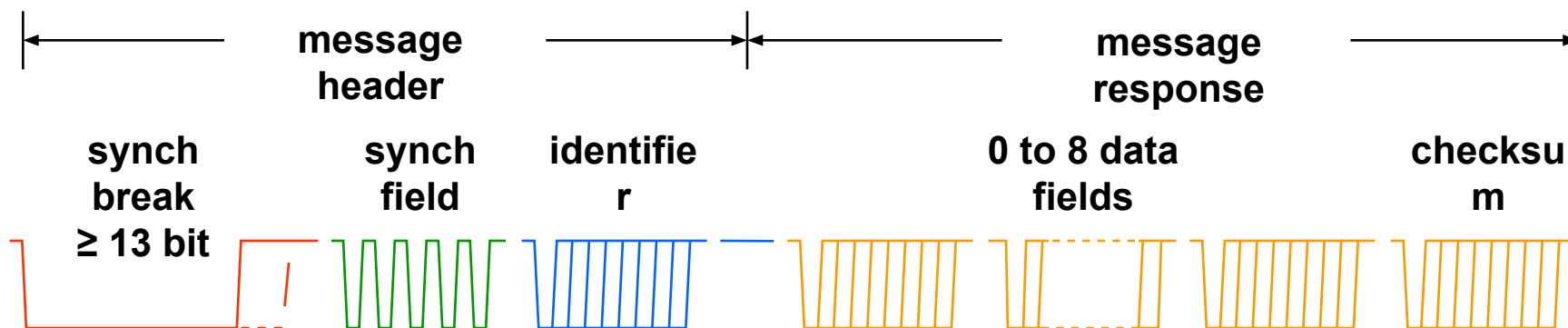
Frame Synchronisation (1)

Initial conditions: +/- 4% baud rate accuracy relative the transmitting source

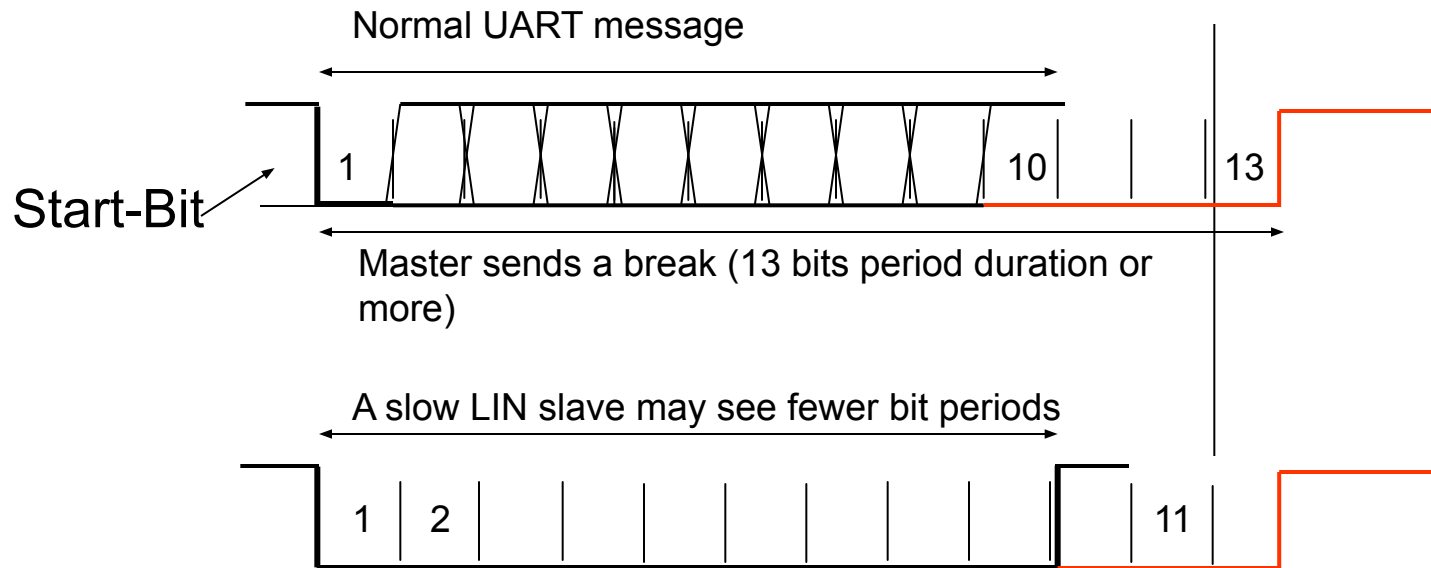A standard transmission of data will require matched send and receiver baud rates

Standard UART byte

Start-Bit

Stop bit

A normal UART with <4% baud rate error will read back the data correctly

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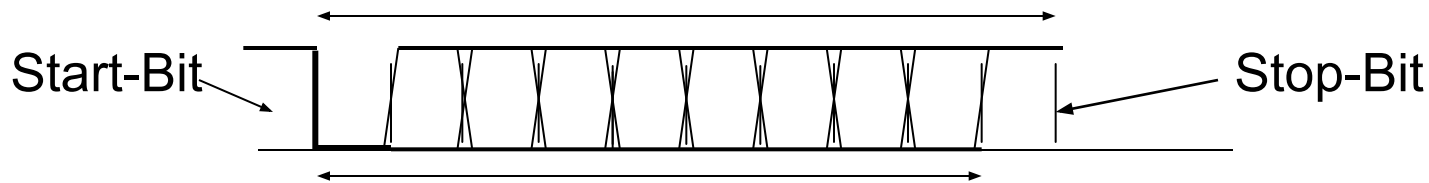*digital dna*
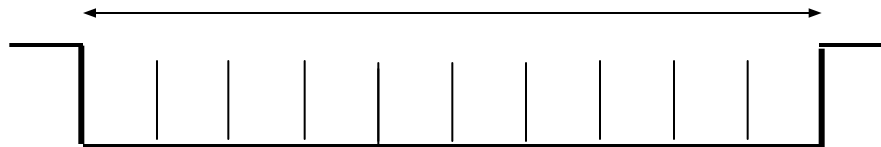
Frame Synchronisation (2)

Initial conditions: +/- 15% baud rate accuracy relative the the LIN master transmitting the synchronisation frame

A synch break must be at least 13 bit periods in duration to allow for this initial variation in oscillator accuracy within the LIN slave
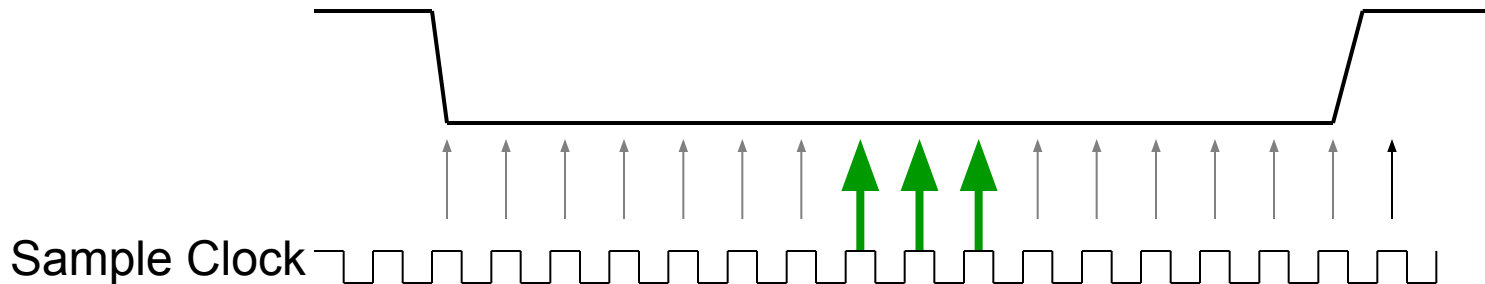

Normal UART message

Start-Bit

Master sends a break (13 bits period duration or more)

A slow LIN slave may see fewer bit periods

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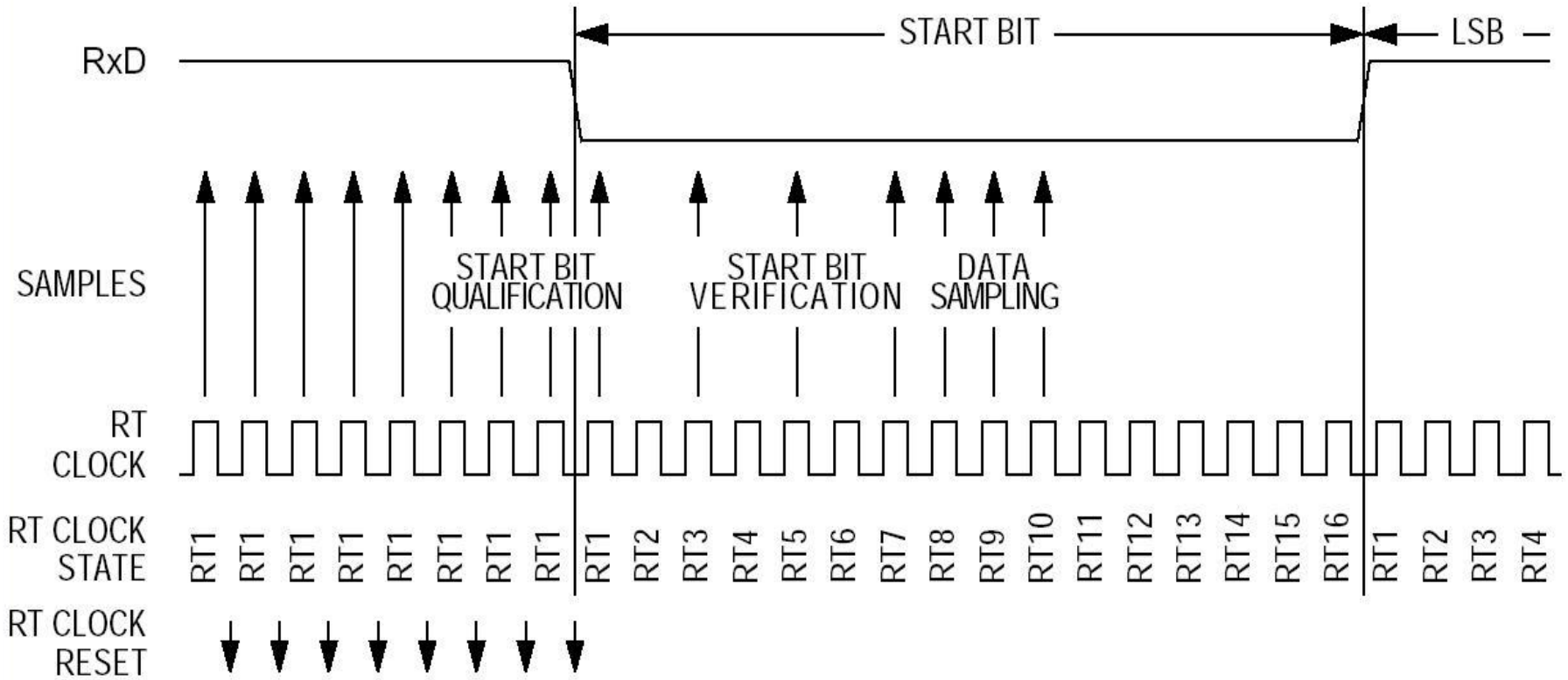
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Bit-Synchronisation

- A start bit transition to a low logic level (dominant) indicates a start of a byte, least significiant first and completing with a logic high level (resessive) bit to indicate the STOP bit

Start-Bit   Stop-Bit
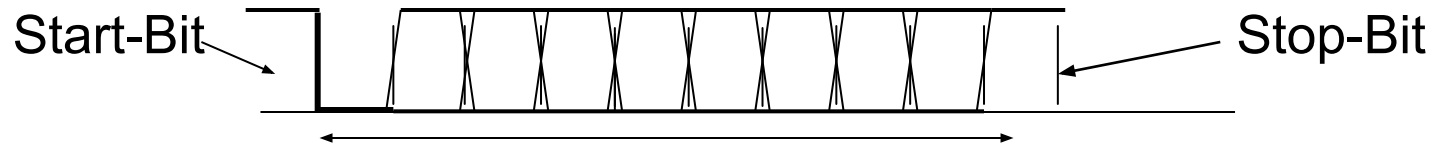
Data is sampled in the middle of the bit field:

Sample Clock

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Bit Sampling

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Bit-Synchronisation

Start-Bit ← → Stop-Bit

After recognition of a Low level in the start bit, the data is sampled at a rate 16 times the bit rate expected. The middle 3 samples must all agree for an error free reception of the data.

A stop bit is expected after 1 start bit and 8 data bits in a typical message

Sample Clock

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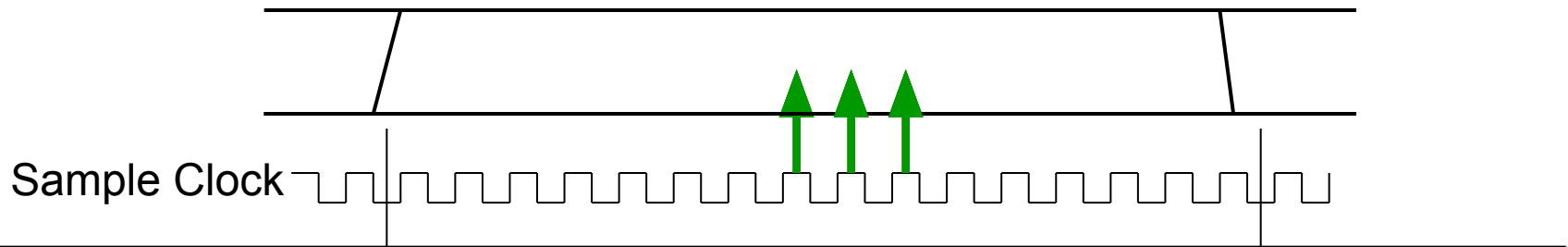
Taking account of Ground-Shift

The detection point for data transitions can be affected by voltage references. Ground shift can change this reference by a significant amount, affecting the bit timing of the data
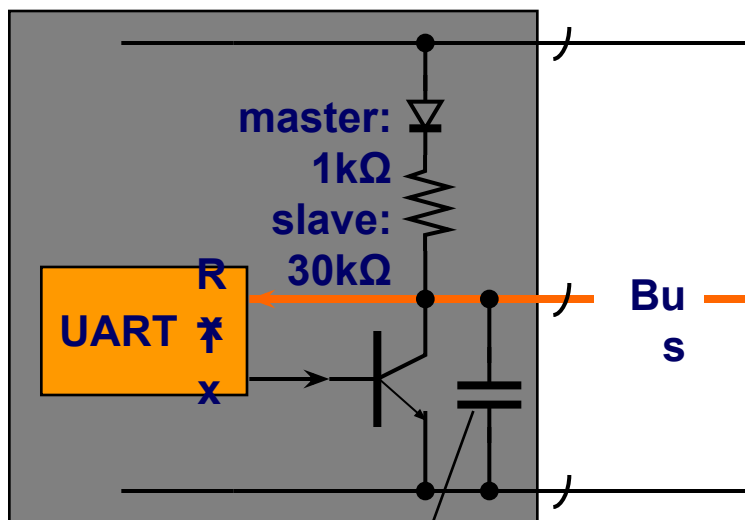

Sense voltage

Data timing
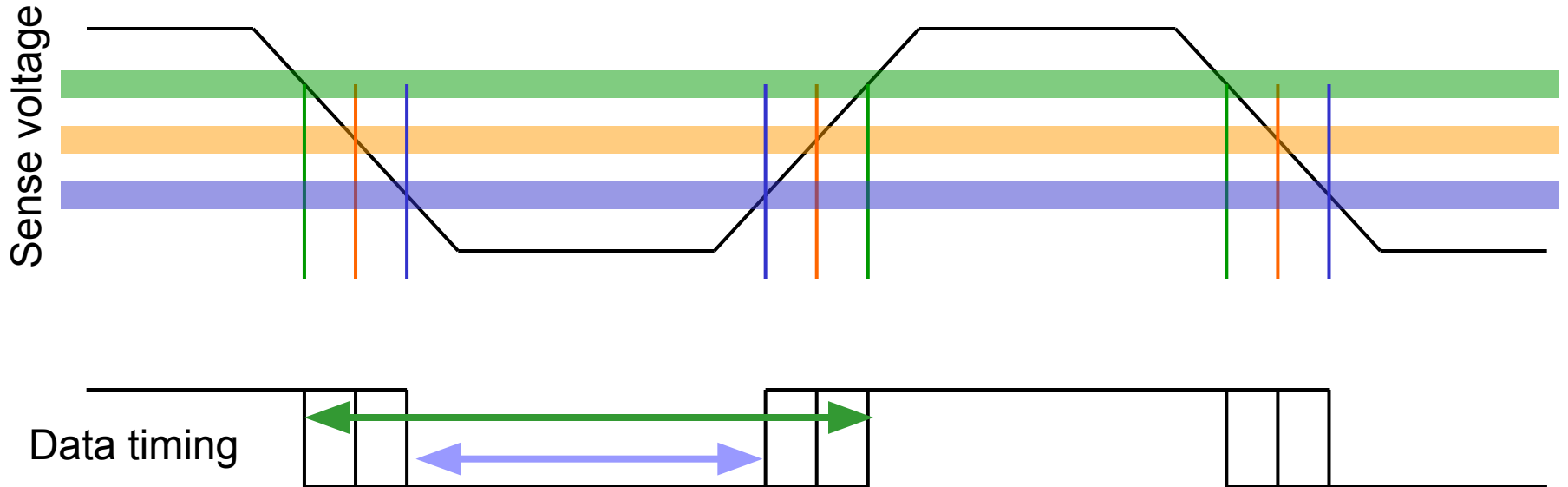
Available bit sampling zone can reduce worst case bit width to around 40us at 20k baud
This affects the overall baud rate tolerance required for safe LIN communications

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LIN Physical Interface

Electronic Control Unit

Bus Voltage

master: 1kΩ
slave: 30kΩ

UART R X

Bus

VBAT 8...18 V

60 %

40 %

GND

recessive logic '1'

controlled slope ~2V/μs

dominant logic '0'

Time

Example capacitances
master: 2.2nF
slave: 220pF

Note:
The LIN specification refers to the ECU connector voltages !

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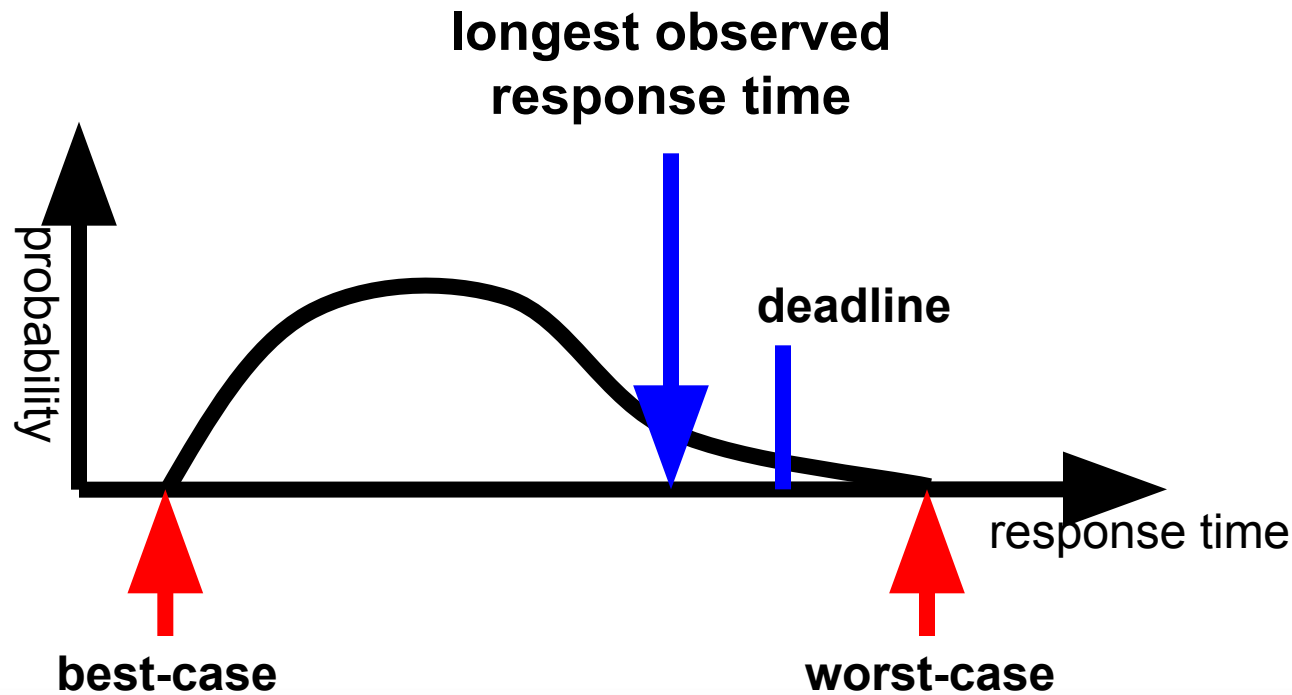digital dna™
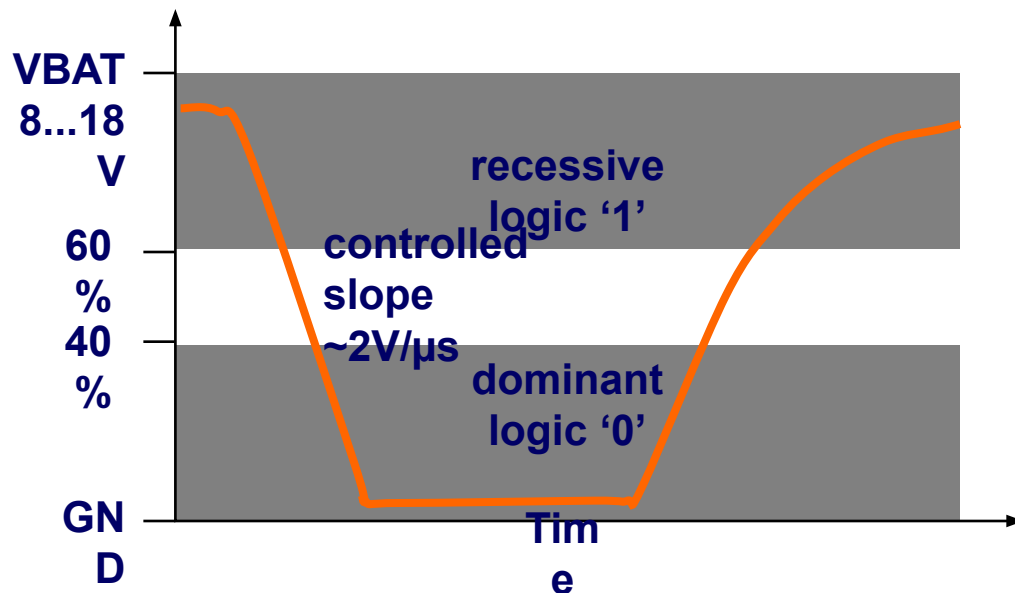
Examination of whether the Deadline is met

- Signal based messaging with static latency analysis ensures that all signals meet defined minimum latency times

- Drives need for complete configuration tool support to ensure guaranteed timing of all signals in a LIN network

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Message latency

notional generation

new value available for trans-mission

start of frame trans-miss ion

completio n of frame trans-miss ion

new value available for read call

notional consump-t ion

generation latency (signal)

scheduling latency (frame)

message length (frame)

notification latency (frame)

consumption latency (signal)

time

LIN availability time (signal)

maximum age (signal)

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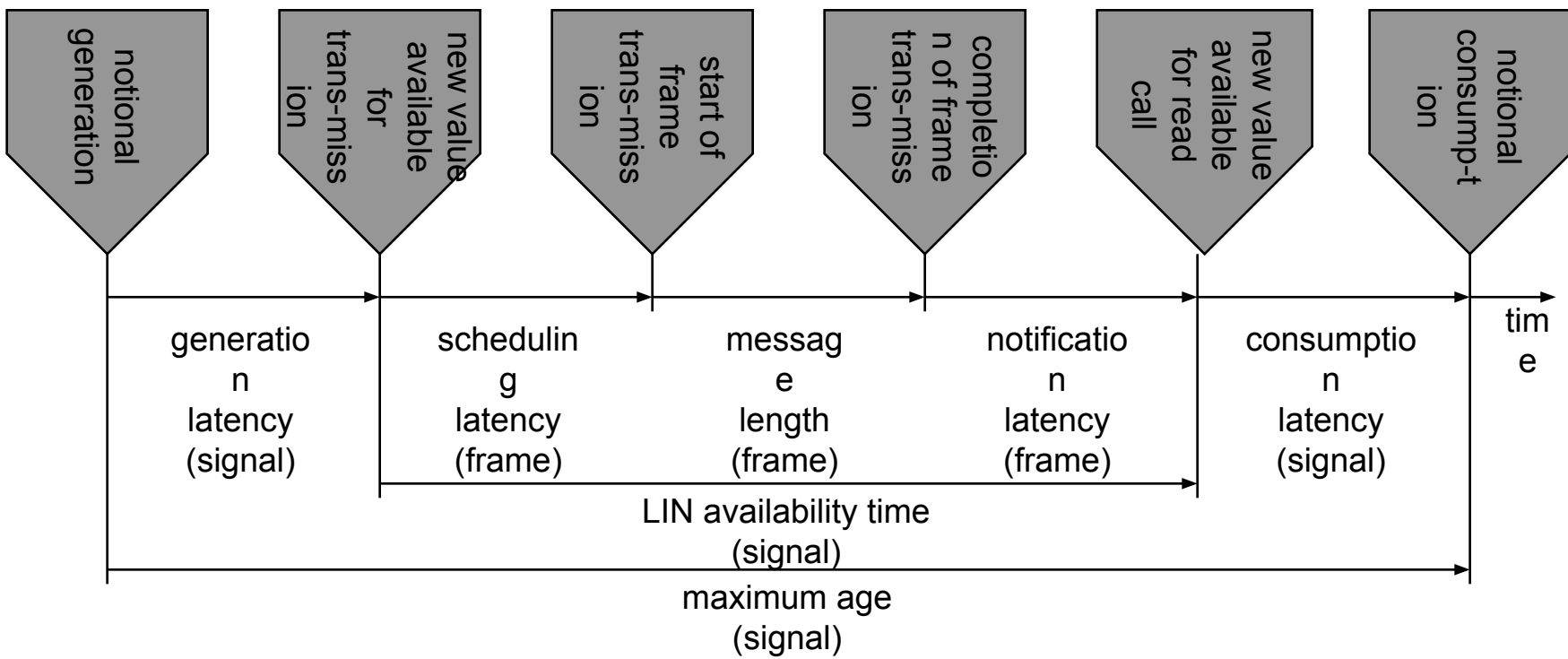
Message latency across a network
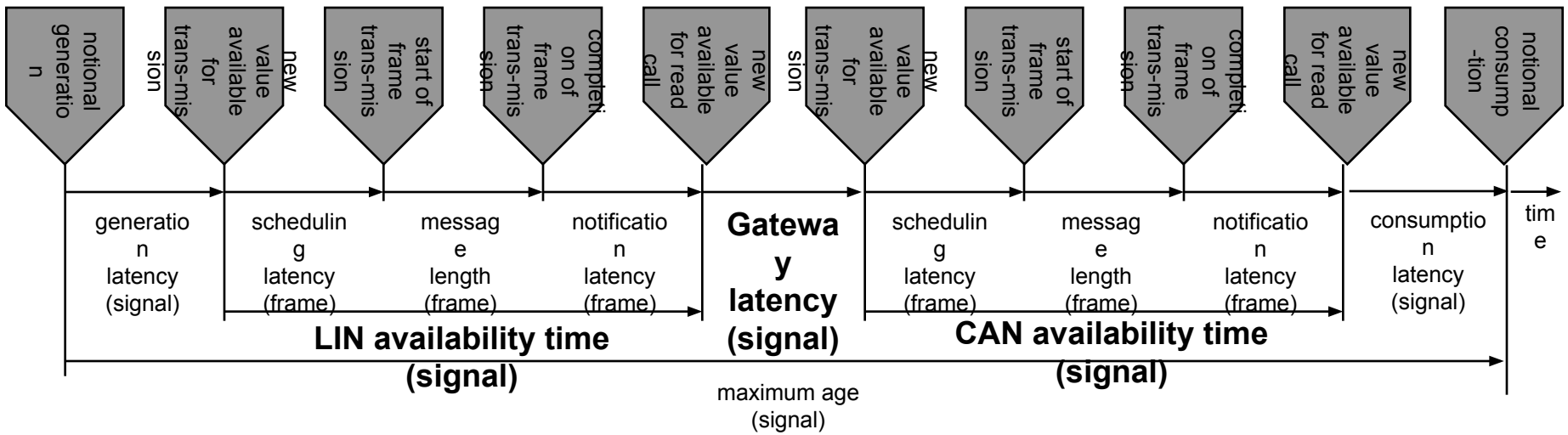
notional generation	trans-mission for	new value available	start of frame trans-mission	completion of frame trans-mission	new value available for read call	trans-mission for	new value available	start of frame trans-mission	completion of frame trans-mission	new value available for read call	notional consump-tion

generation latency (signal)	scheduling latency (frame)	message length (frame)	notification latency (frame)	**Gateway latency (signal)**	scheduling latency (frame)	message length (frame)	notification latency (frame)	consumption latency (signal)	time

LIN availability time (signal)

CAN availability time (signal)

maximum age (signal)

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Latency optimisation with LIN

Basic schedule

Window Status	Lock Status	Mirror Status	Master Command	Keyboard Status
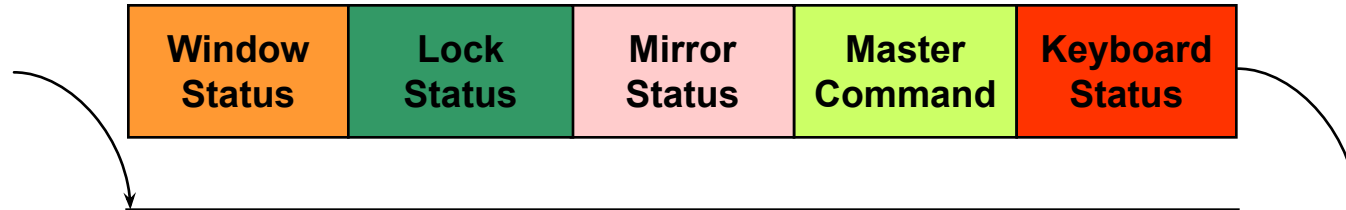
Alternate schedule for low latency signals from a keyboard
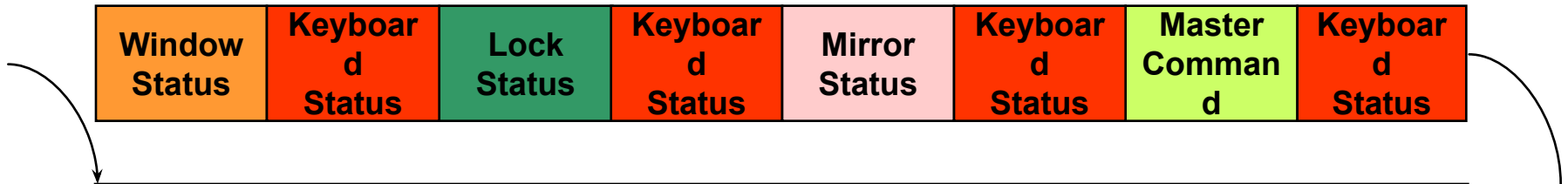
Window Status	Keyboard Status	Lock Status	Keyboard Status	Mirror Status	Keyboard Status	Master Command	Keyboard Status

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Variables Scheduling

Alternate Schedule Table

Main Schedule Table

Sub Schedule Table

Sub Schedule Table

Sub Schedule Table

Decision

| Msg A | Msg B | Msg C | Msg A | Msg D |

| Msg B | Msg A | Msg E | Msg F |

| Msg G | Msg A | Msg E | Msg F |

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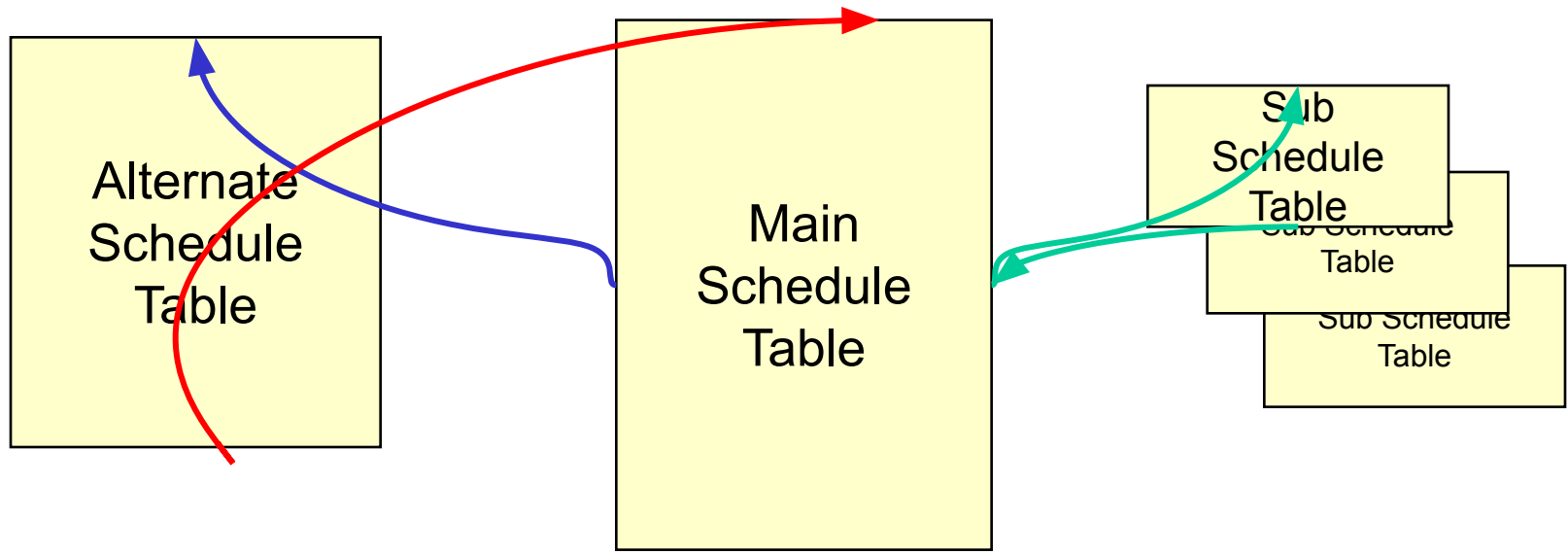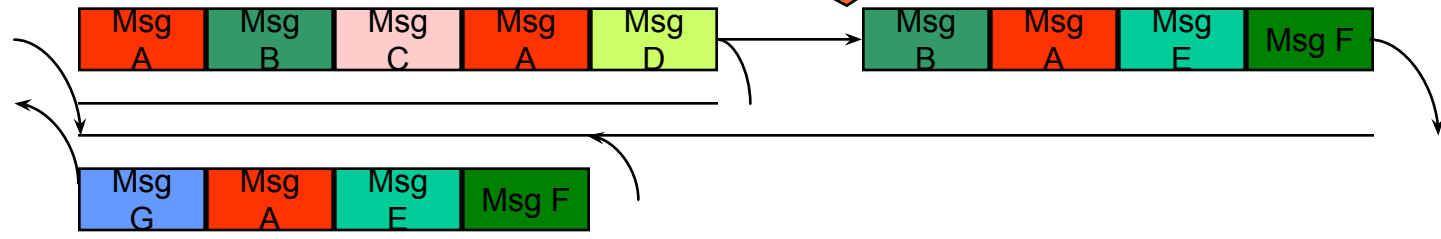
Event Triggered Message

- Problem
  - **Specific node communication required but this takes up too much time for all network messages**
- Solution : Event Triggered frame:
  - **Header is sent out**
    1. **normal case: no answer**
    2. **Rare response: only one node responds**
    3. **Very rare response : several nodes respond simultaneously**
- Cases 1 and 3 are exceptions that should be addressed at the application design.
- Event triggered messaging is complementary to the regular signal based messaging scheme

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Further information

 - Consortium

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http://www.lin-subbus.org

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LIN Development Flow
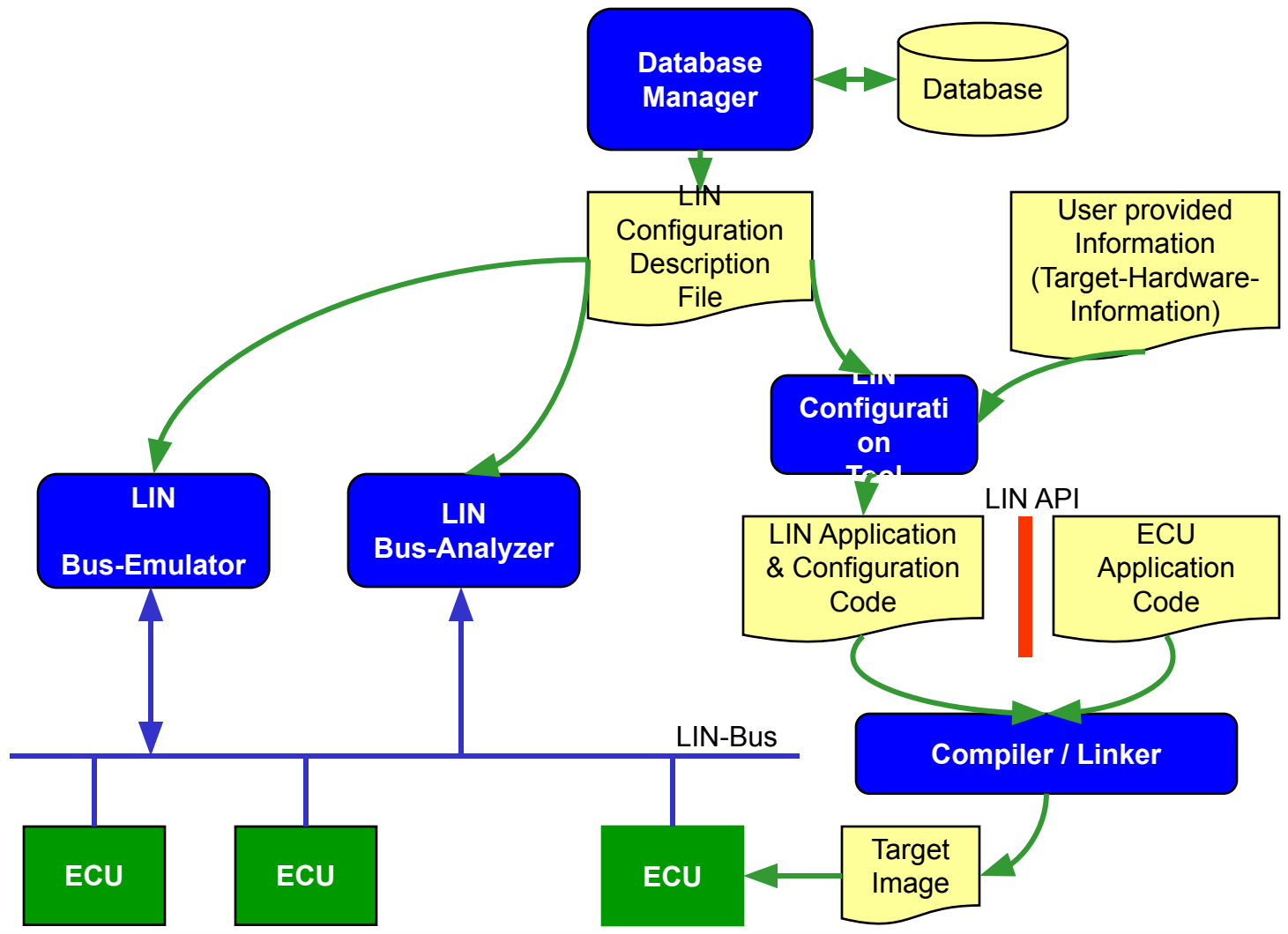
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LIN Configuration Description File

- Includes all essential information of network signals, latency periods, cycle times, nodes affected

- Input file serves as a development interface for a node

- LIN Application Generator
  - **LIN-Emulator**
  - **LIN Analyser**

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The Workflow

- **Data Input**
    - **Definition of objects**
    - **Definition of relations between the objects**

- **Data Processing**
    - **Signal Packing (Frame Editor/Frame Compiler)**
    - **Timing Analysis**

- **Data Output**
    - **Configuration file generation**
    - **Various optional customer-defined post-operations**

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