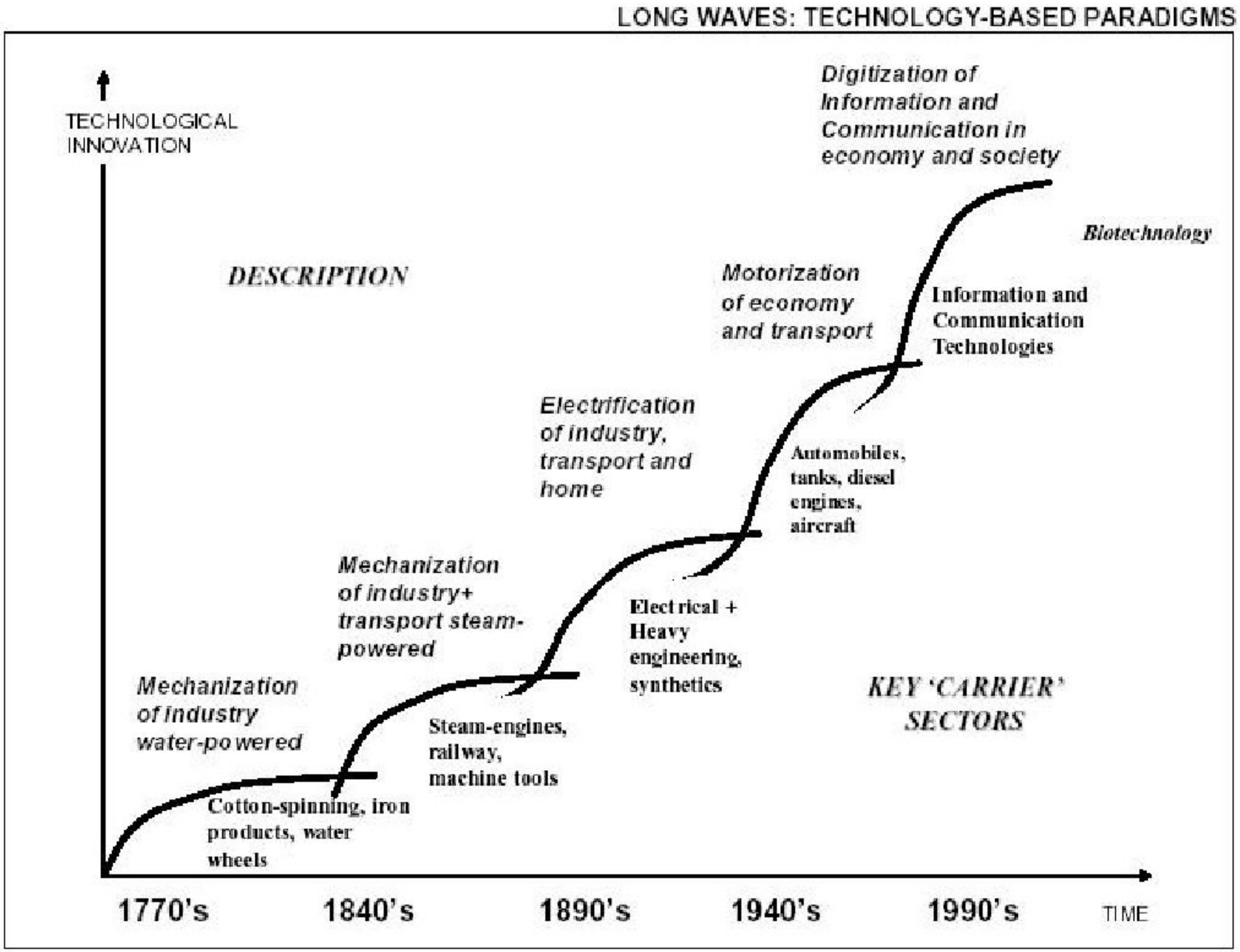
Наноэлектроника: устройства, цепи, архитектура

OUTLINE

1. Microelectronics: Present status and challenges
   - CMOS: the technology which has changed the world
   - scaling and Moore's Law
   - the Red Brick Wall: "challenges" and challenges
2. Nanoelectronics: Physics and technology
   - carbon nanotubes, graphene, spintronics, and other fashions
   - physics options: ballistics, tunneling, quantum-mechanical interference
   - the patterning challenge, the bottom-up approach
3. Hybrid CMOS/nanoelectronic circuits
   - memory effects
   - the hybrid circuits: history and evolution
   - CMOL, FPNI, 3D CMOL and all that alphabet soup
4. Possible applications
   - terabit-scale memories
   - reconfigurable logic circuits
   - the CMOL roadmap
   - mixed-signal neuromorphic networks
5. Challenges
   - molecular options: single-electronics vs. atomic reconfiguration
   - advanced patterning methods
   - summary and conclusions

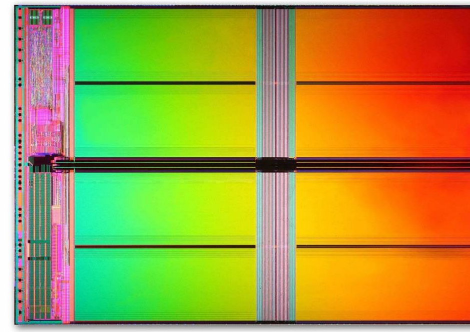
Из пещер к цифровому обществу



Source: Martin R. Hilbert; based on Freeman and Louça (2001)

CMOS MEMORY AND PROCESSORS
КМОП память и процессоры

Samsung SD card with NAND flash memory chip (Feb. 2009: 64 Gb on a die at 43 nm fab)



Intel Core 2 Extreme microprocessors (2008): 45 nm fab, ~3×10^{8} transistors, 4MB L2 cache, power consumption ~75 W)

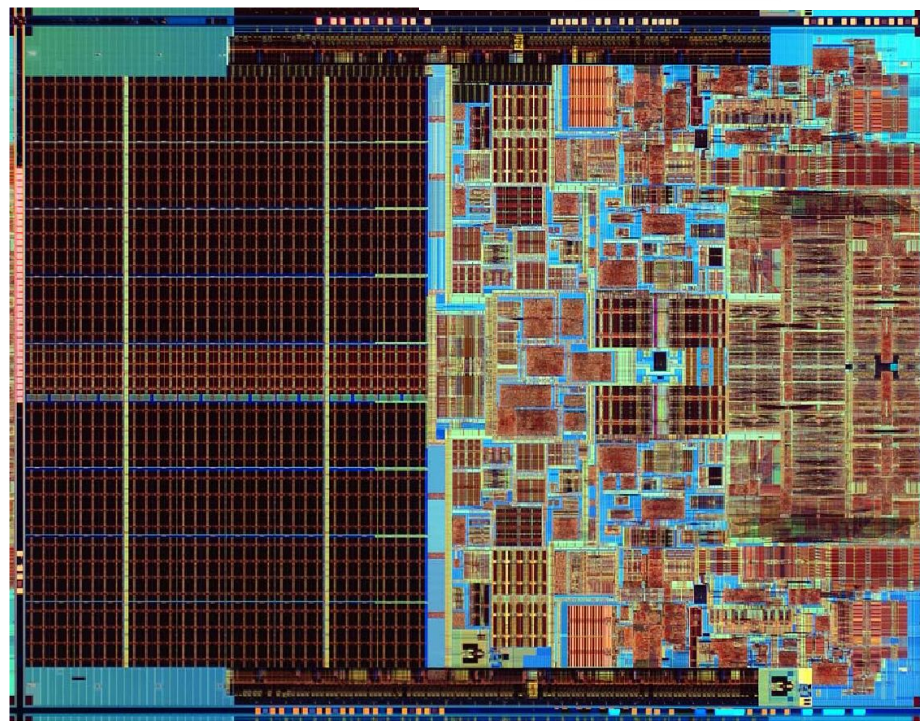


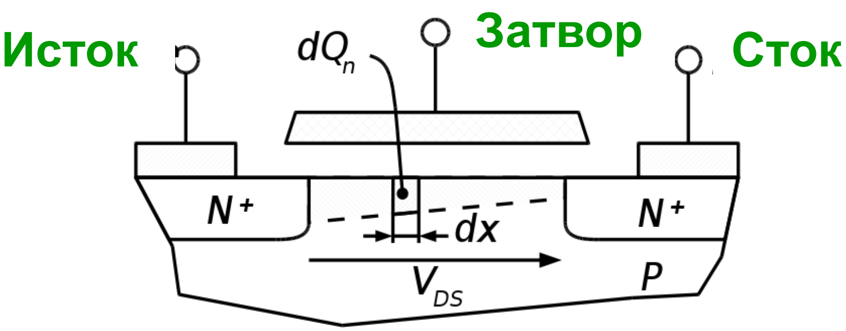
Figure: Intel

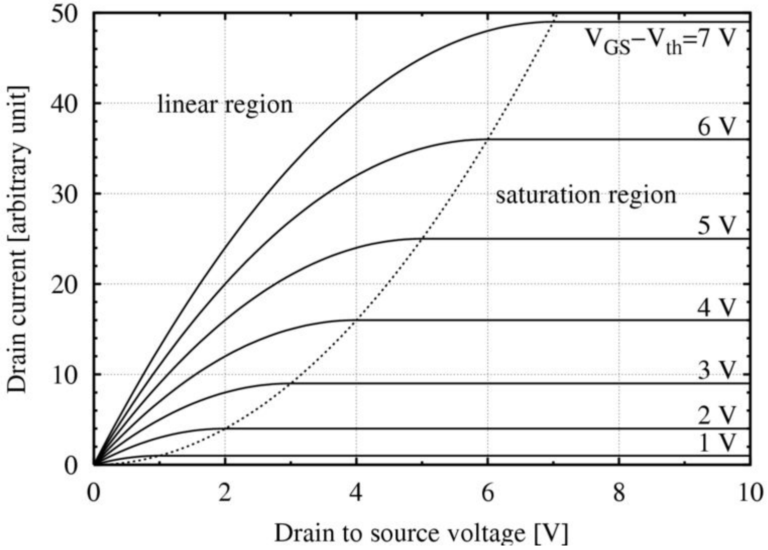
Флэш-память NAND отличается малыми размерами запоминающей ячейки и, соответственно, минимальной ценой единицы информации; широко используется в запоминающих устройствах таких потребительских товарах, как цифровые камеры и плееры MP3. Эта архитектура также широко применяется для хранения данных в камерах и сотовых телефонах.

SILICON MOSFET: THE CONCEPT

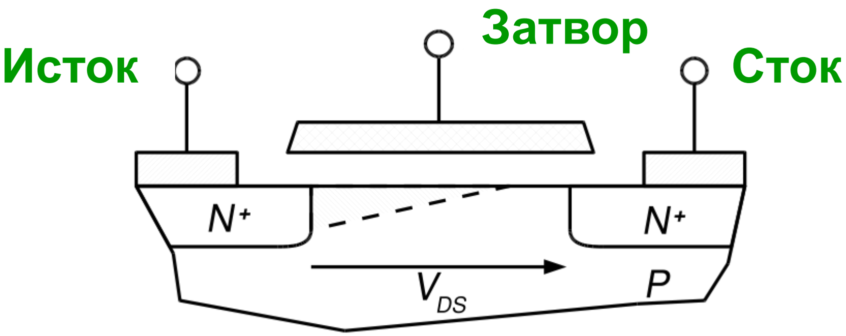
Концепция полевого МОП транзистора

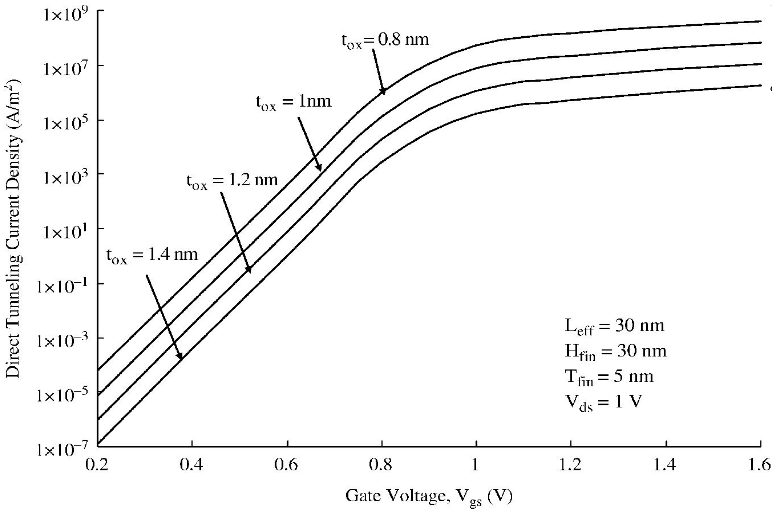
Линейный режим:



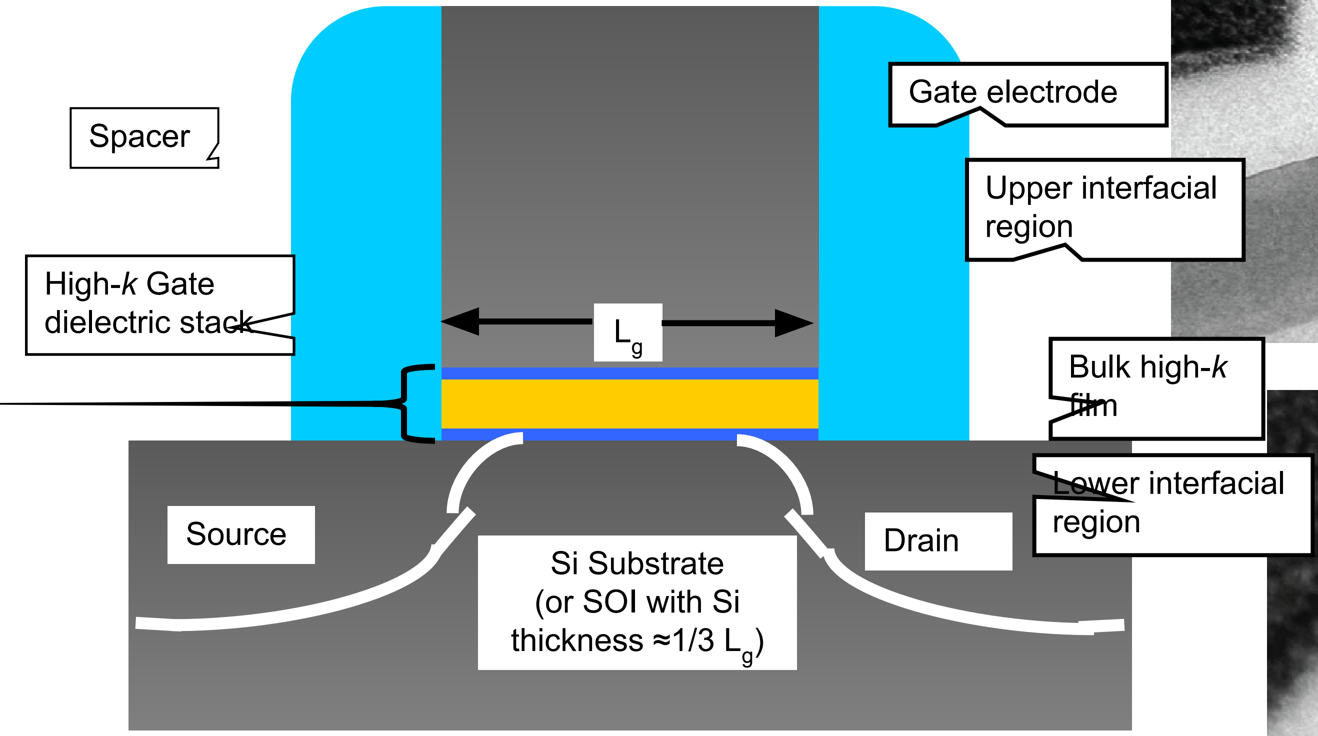


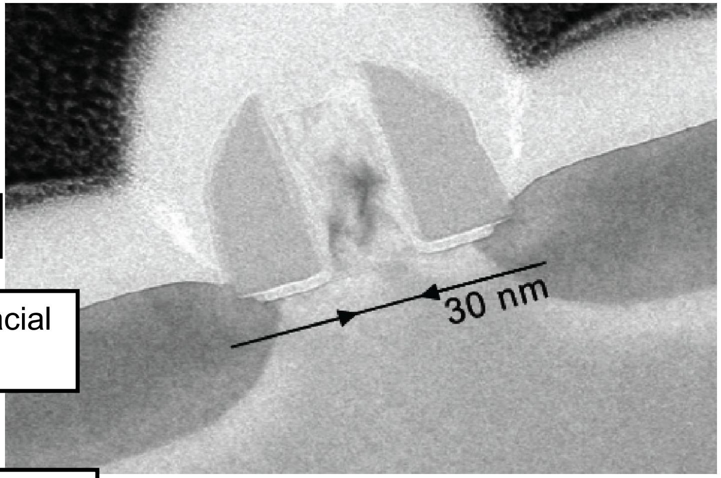
Насыщение:

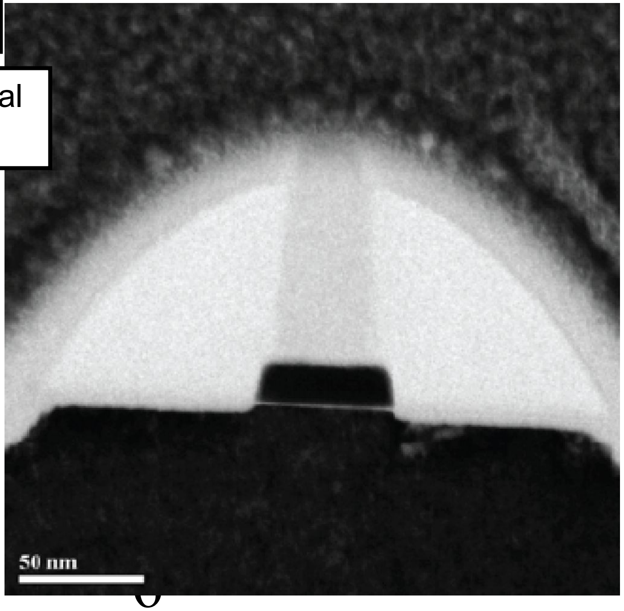




Современные полевые МОП транзисторы



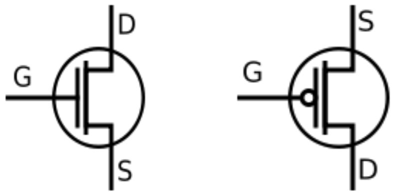


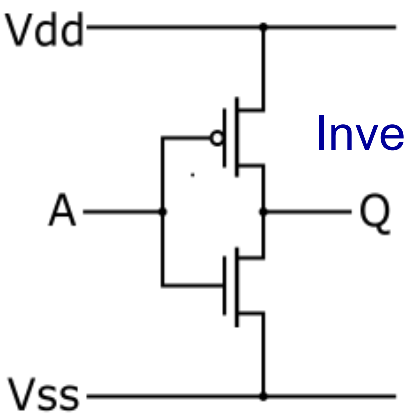


CMOS LOGIC

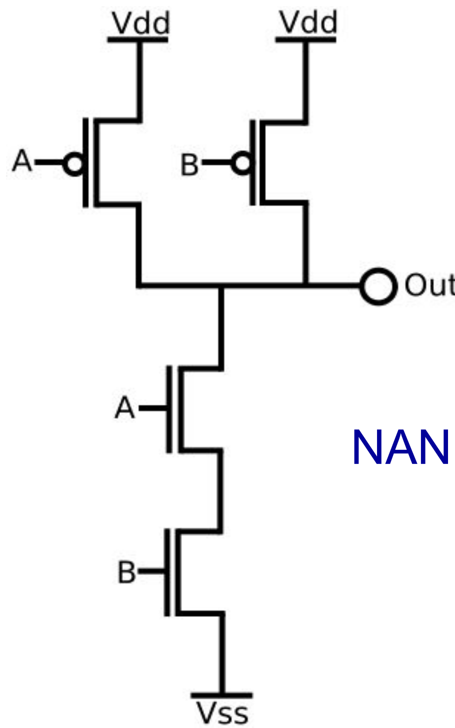
FET notation:

n-channel *p*-channel

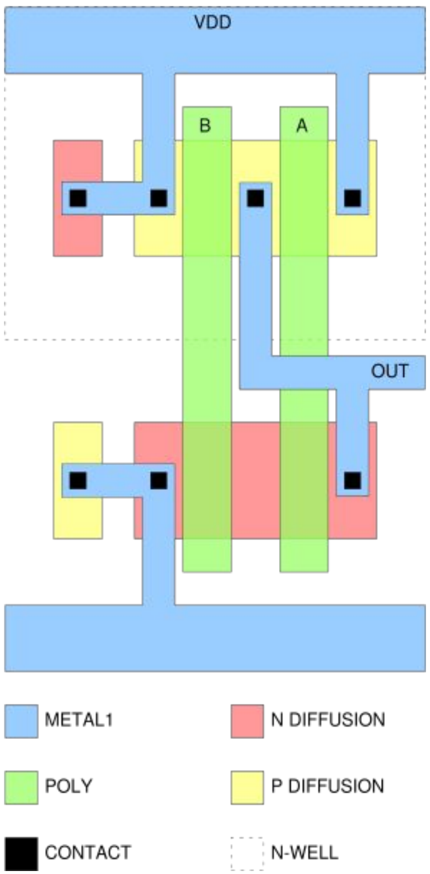




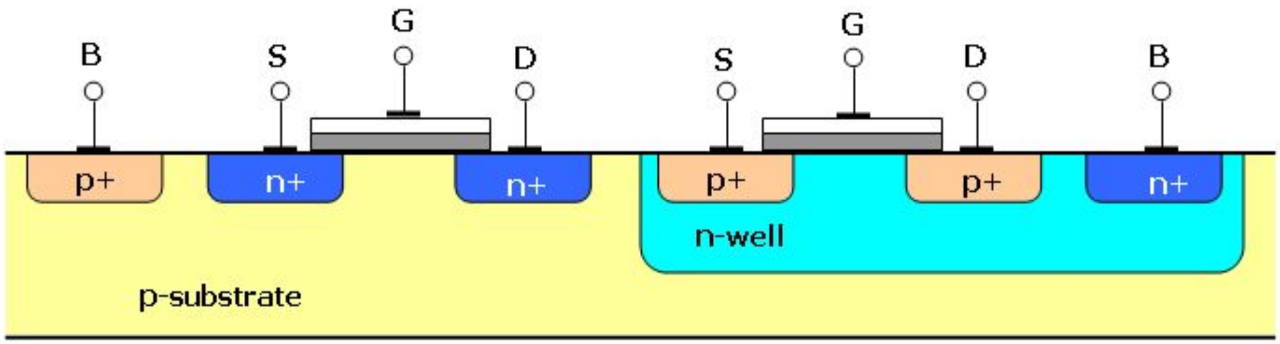
Inverter



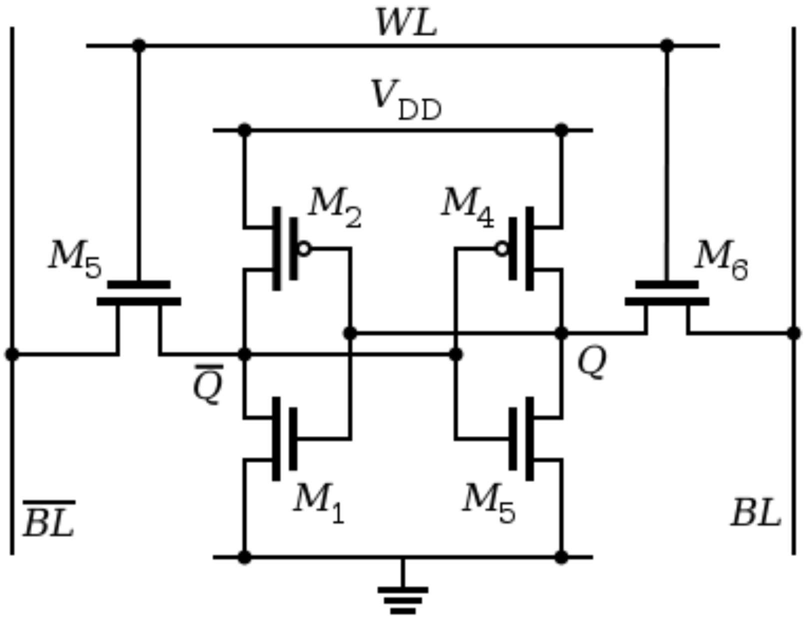
NAND gate



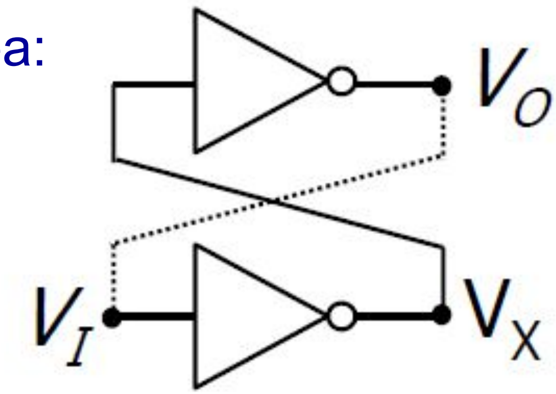
CMOS cross-section

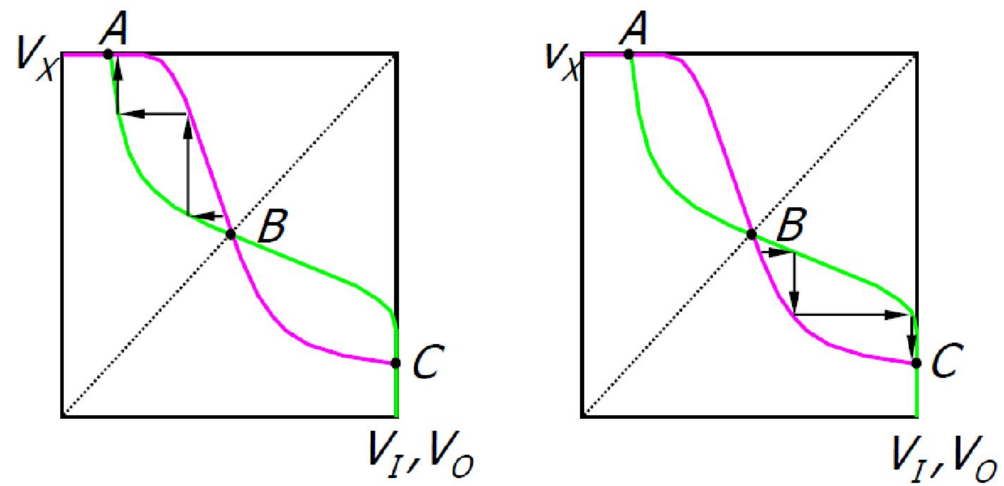


СОЗУ SRAM



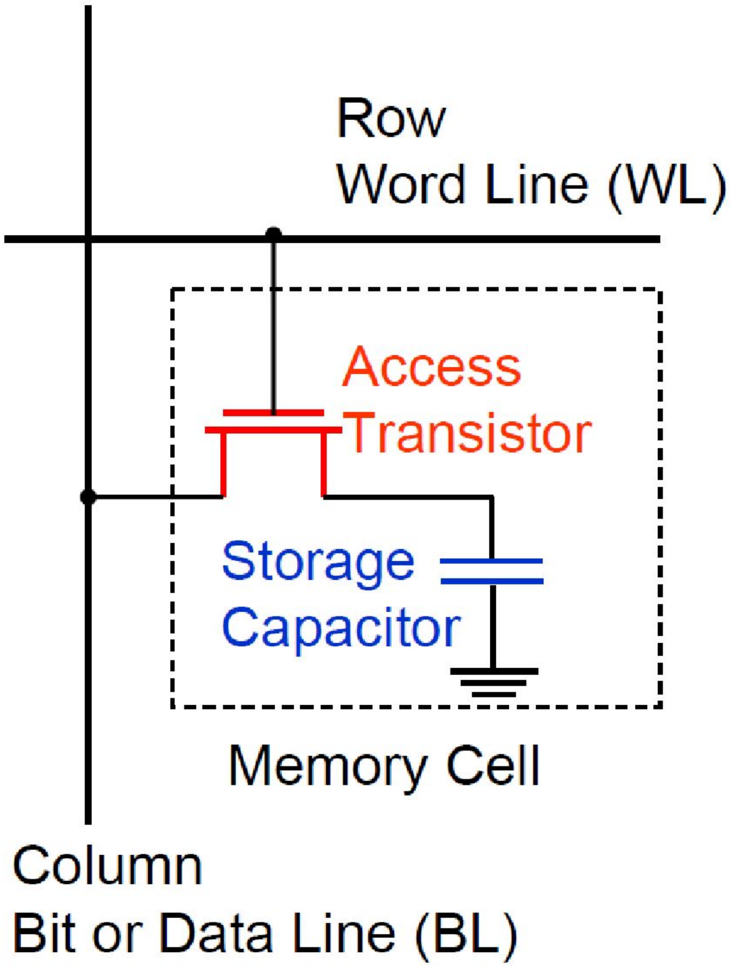
Operation idea:

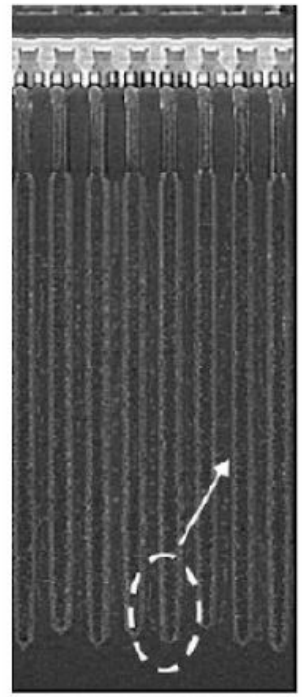


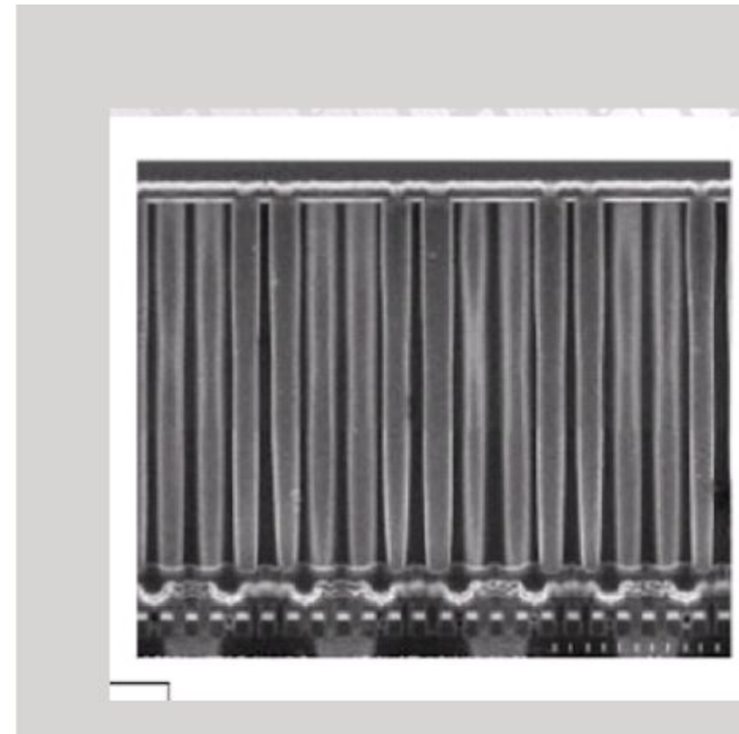


5-6 transistors, access time below 1 ns, CMOS-scalable, $A \sim 100\ F^2$

ДОЗУ DRAM



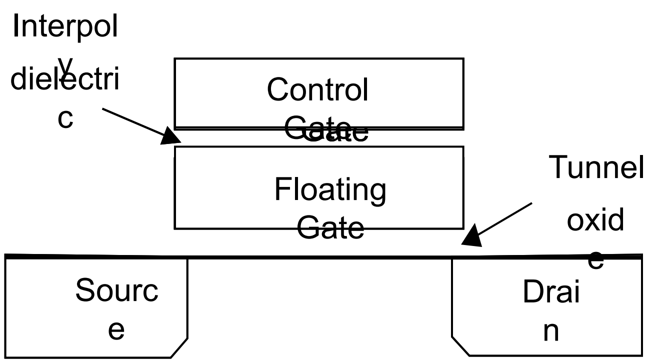




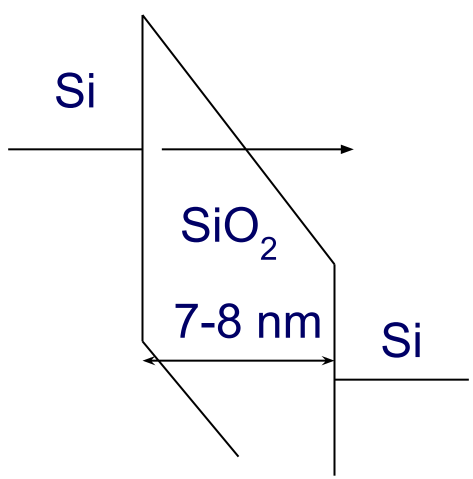
From 16 Mb up, non-planar; stuck at 512 Mb; stopped to be the IC technology driver, but still no good replacement

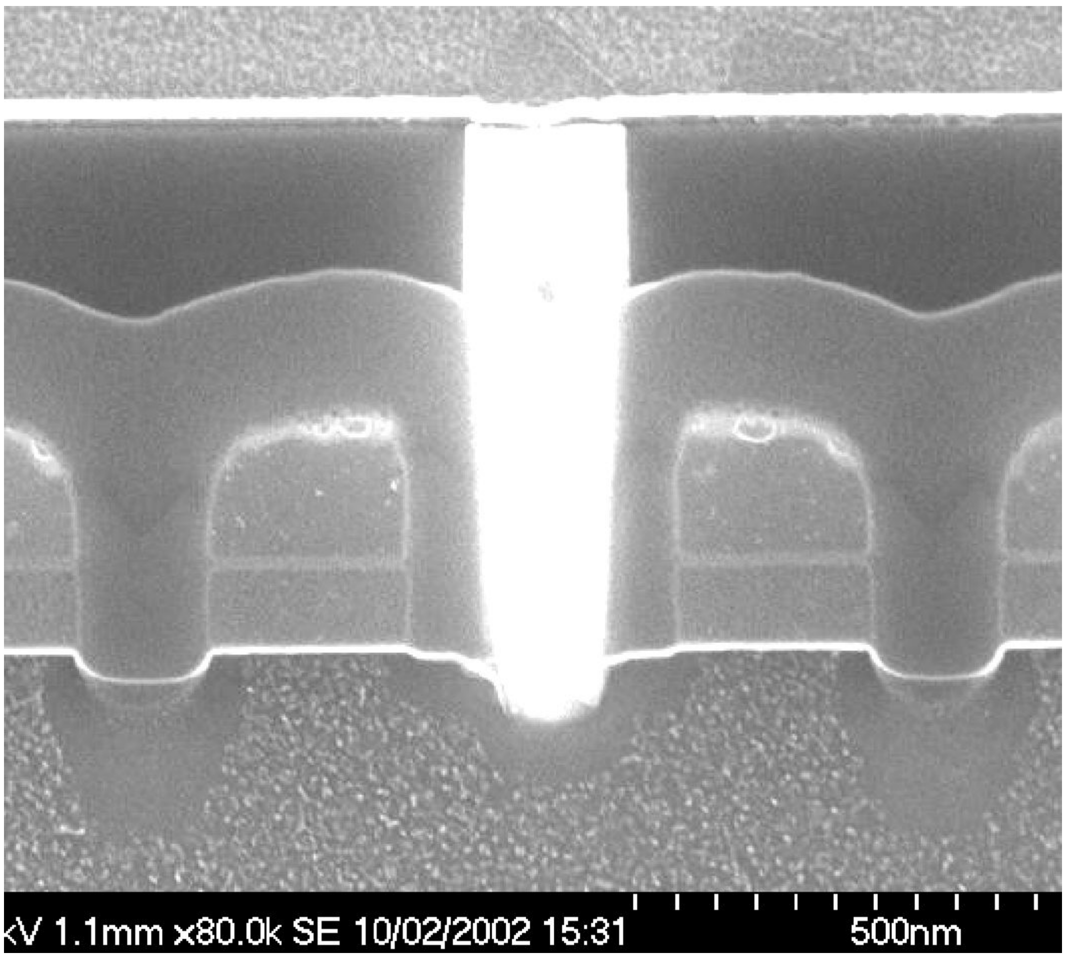
1 transistor, access in 10s ns, needs refresh, NOT scalable (C ~ 25 fF)

NAND FLASH MEMORY: CELL

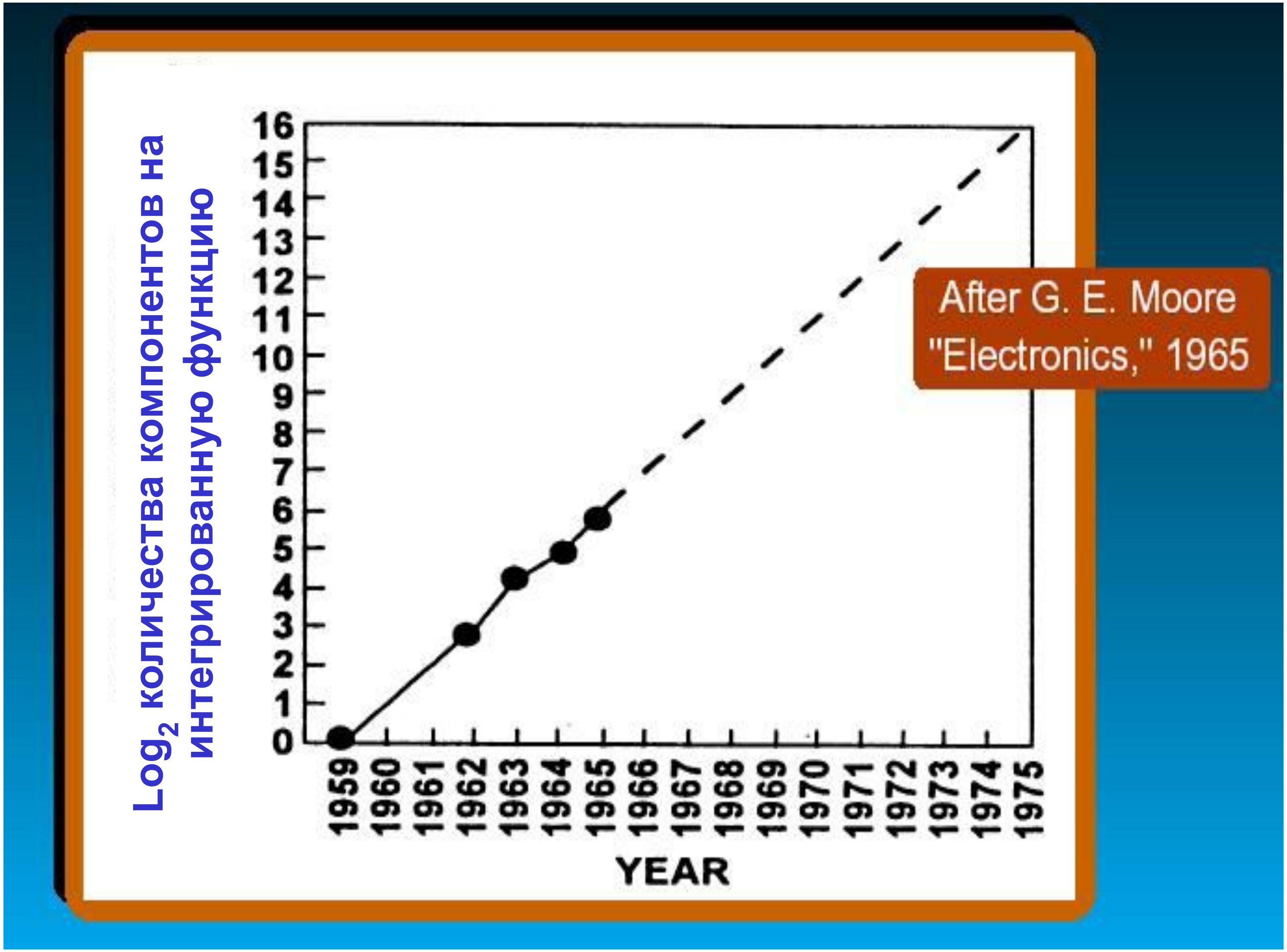


Fowler-Nordheim tunneling





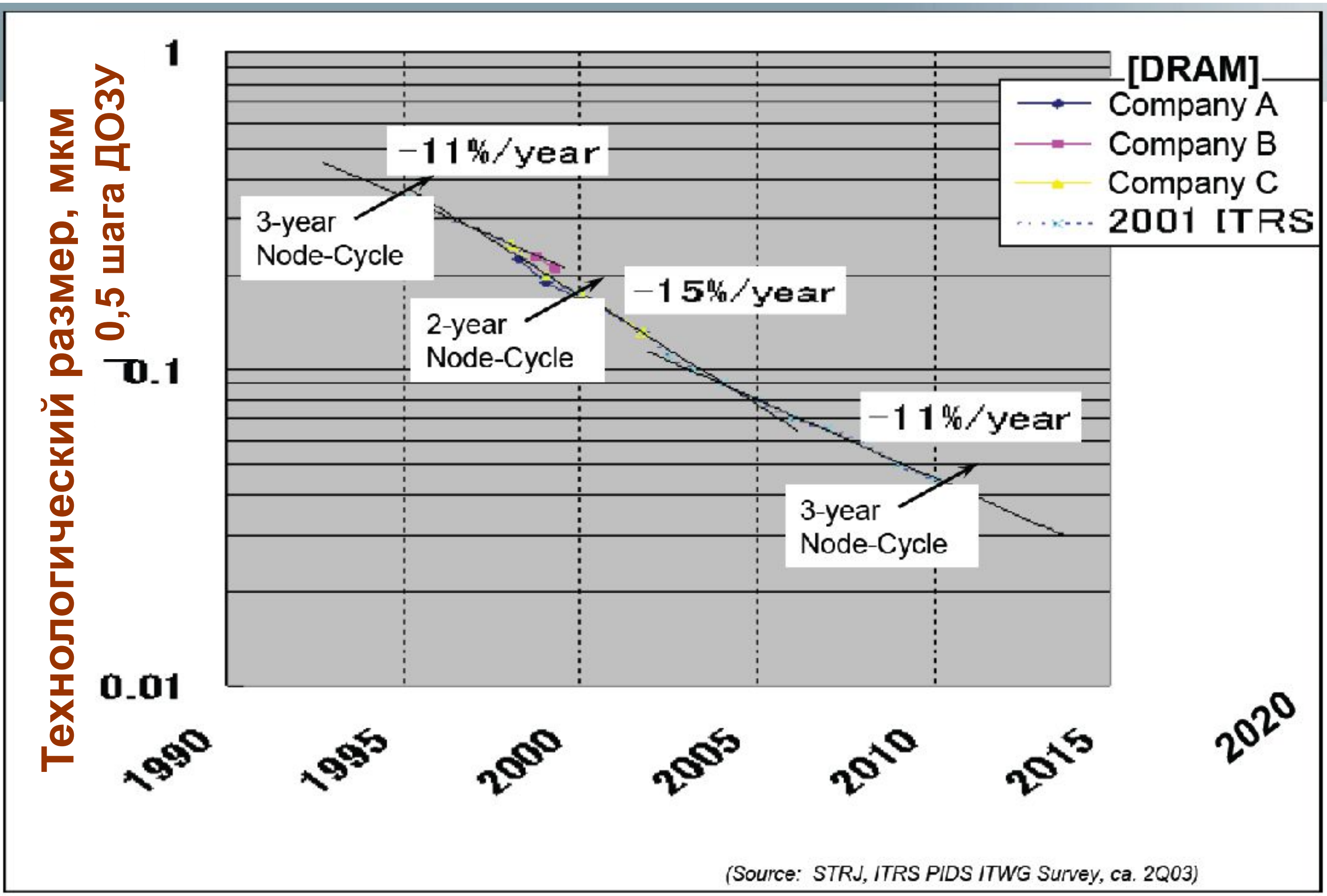
Закон Мура (MOORE'S LAW)



Закон Мура для интегрированных схем

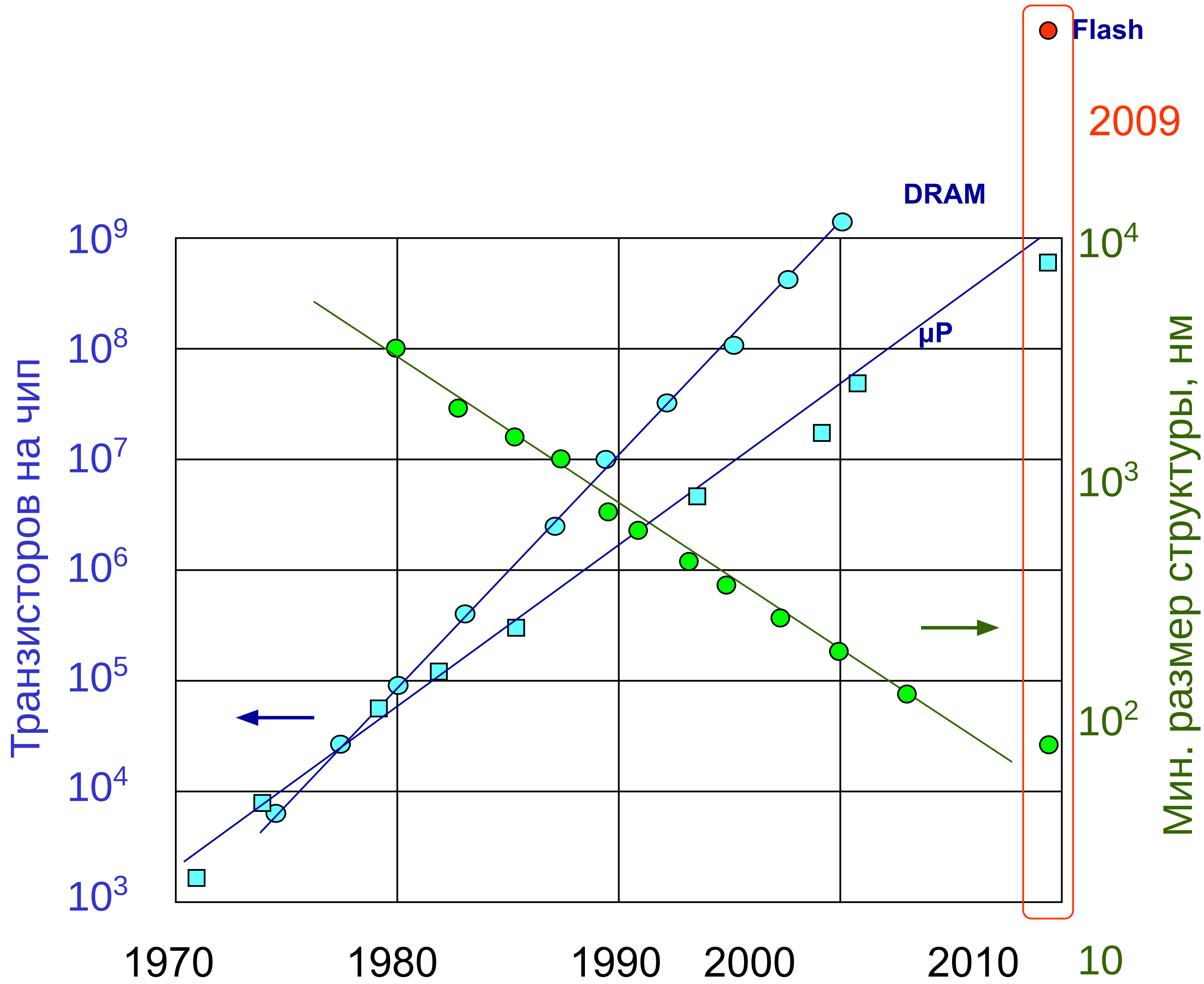
Figure: Intel

Закон Мура для минимального размера



ITRS International Technology Roadmap for Semiconductor

Закон Мура для плотности элементов



Физические основы закона Мура на примере MOSFET

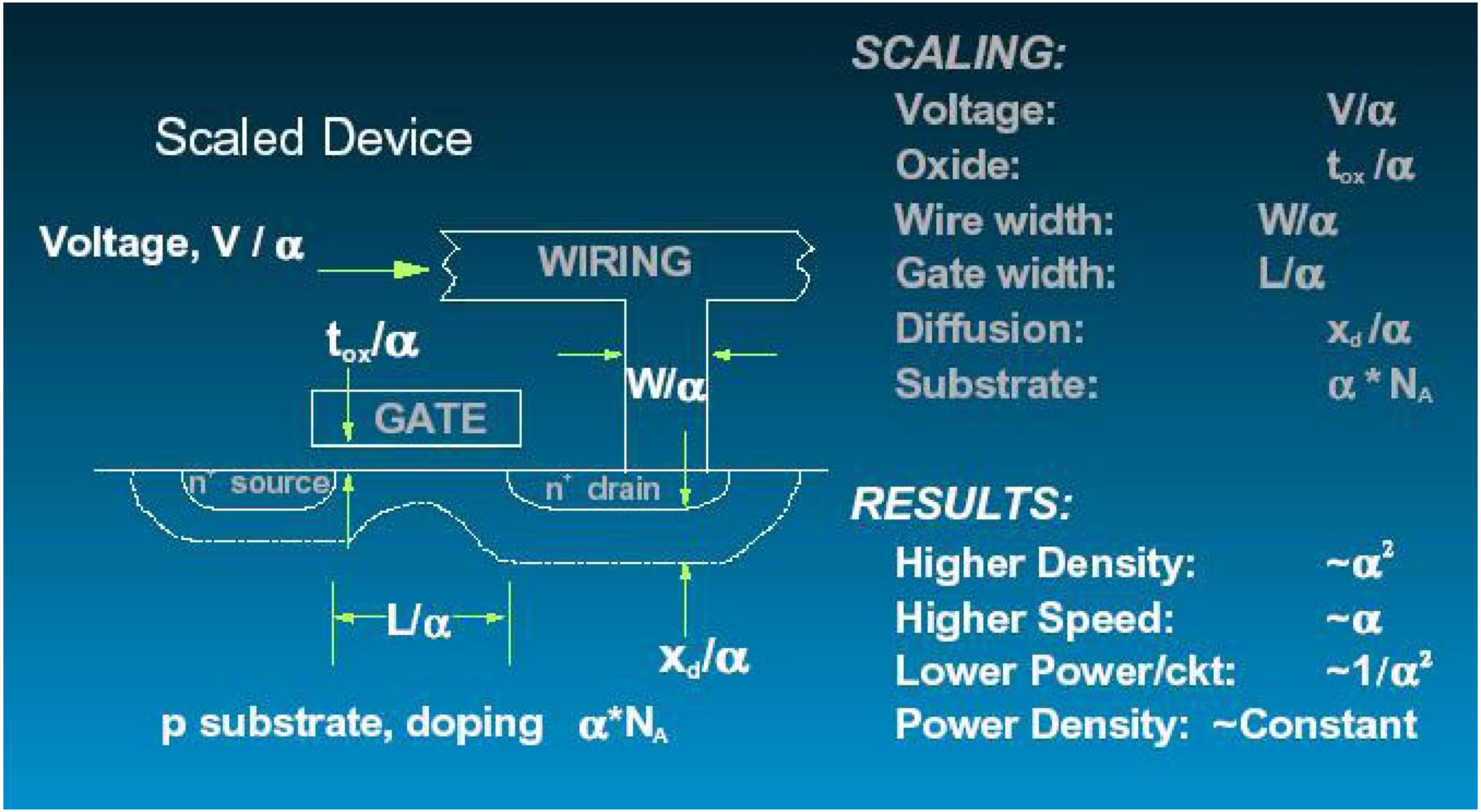
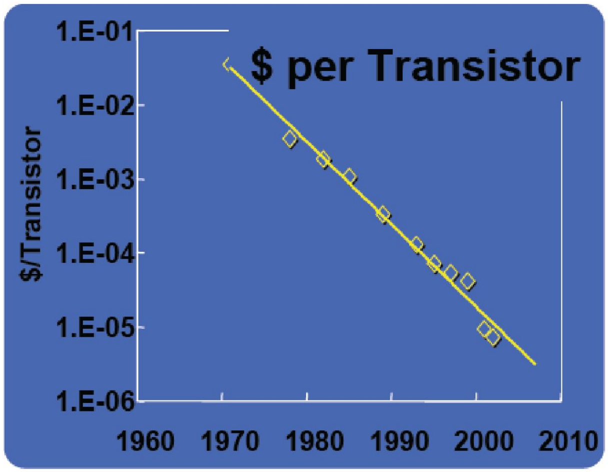


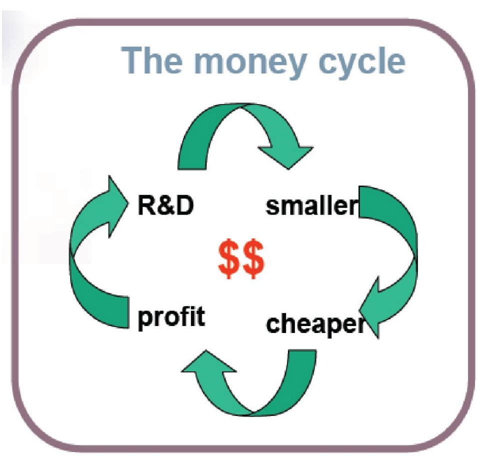
Figure: R. Isaac (2001)

Экономические основы закона Мура



Стоимость микропроцессоров

NAND Flash 2009:
~10^{-11} $/transistor (!!)



New fab: ~ a few $B, currently ~30 are being built.

The semiconductor industry can progress only by rolling over a large fraction of its revenue into the development of the next generation of chips.

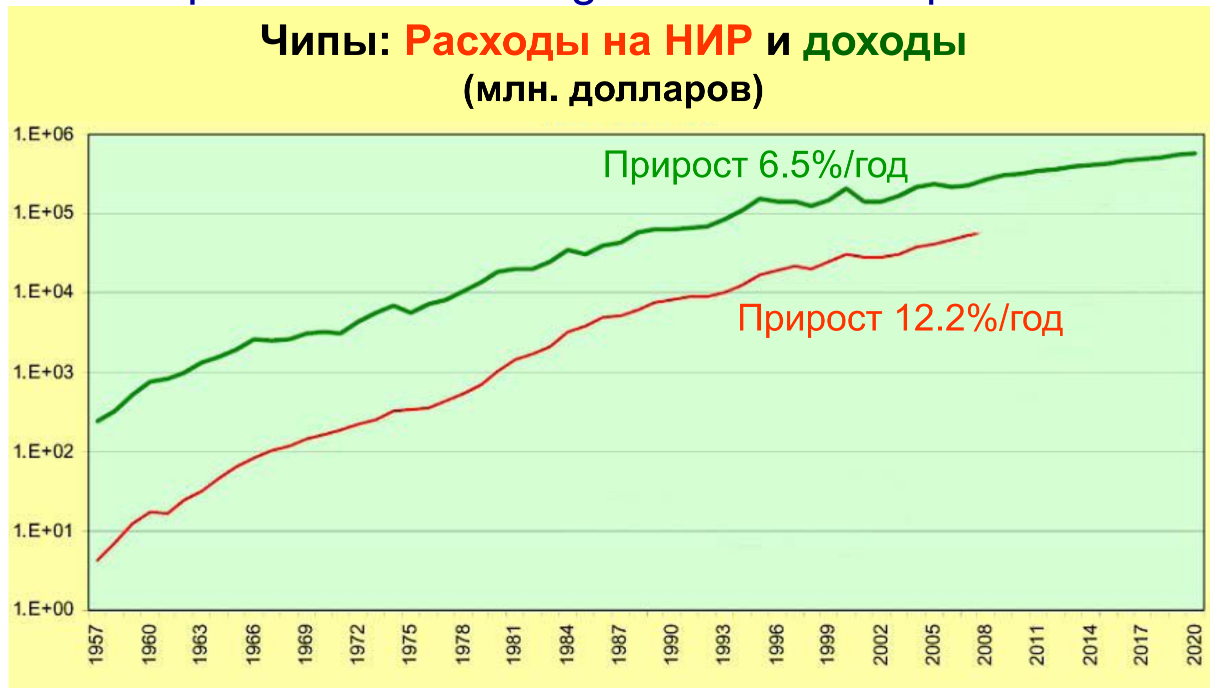
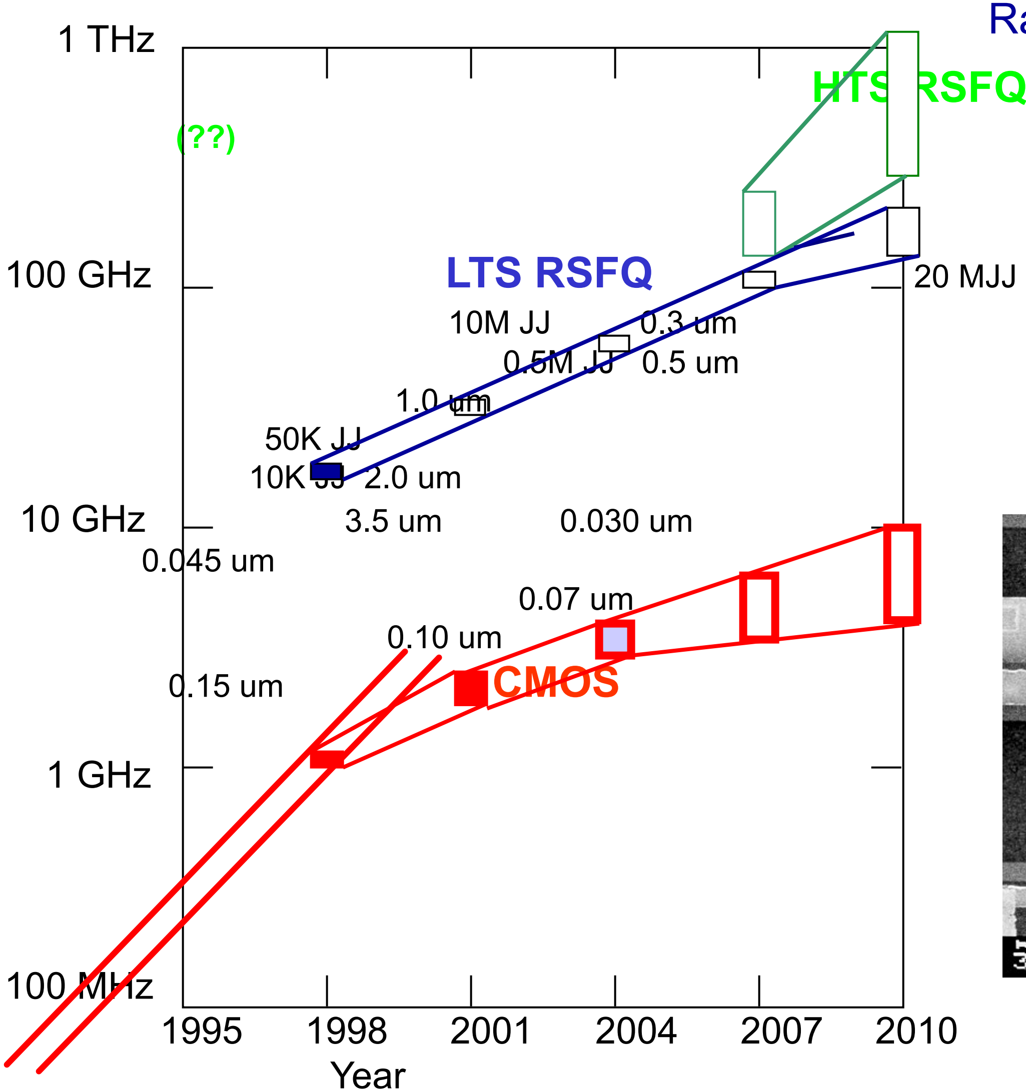
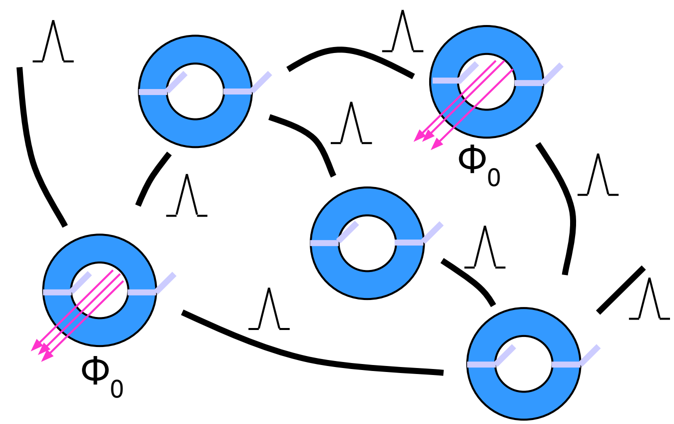


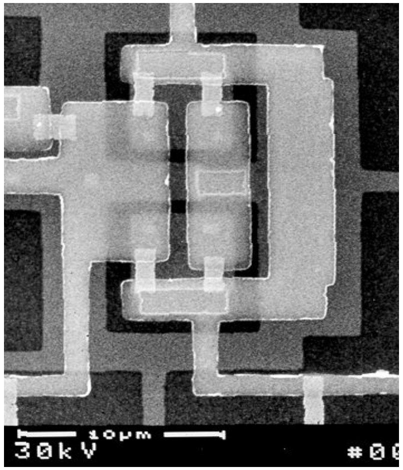
Figure: D. Hutcheson, VLSI Research

DETOUR A: NOT EVERYTHING IS MOORE'S LAW

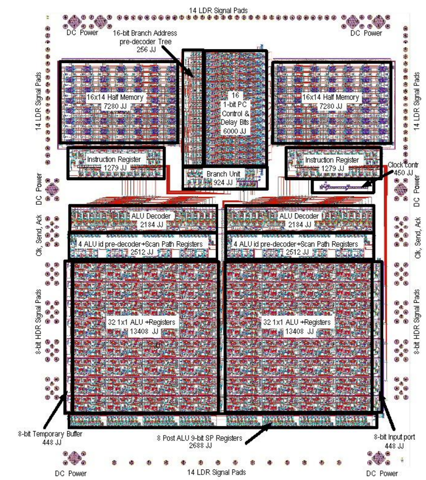


Rapid Single-Flux-Quantum (RSFQ) logic



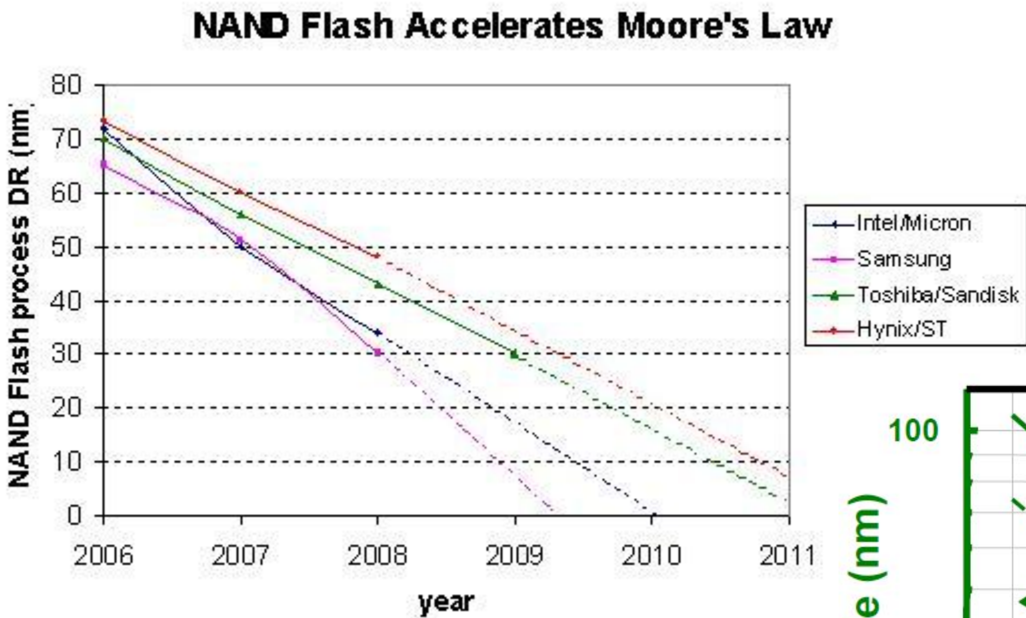


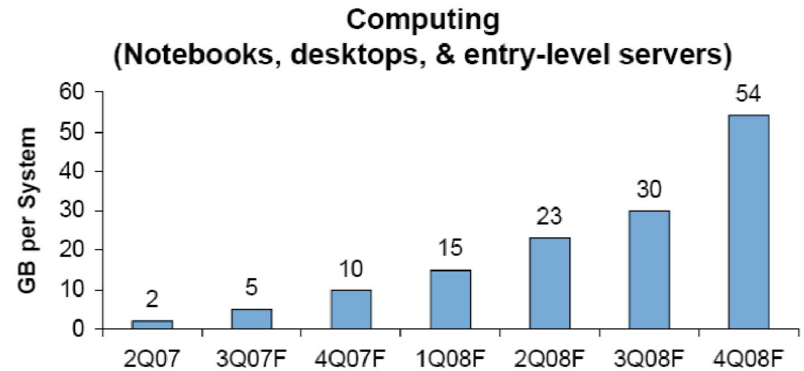
770 GHz, 1.5 µW frequency divider

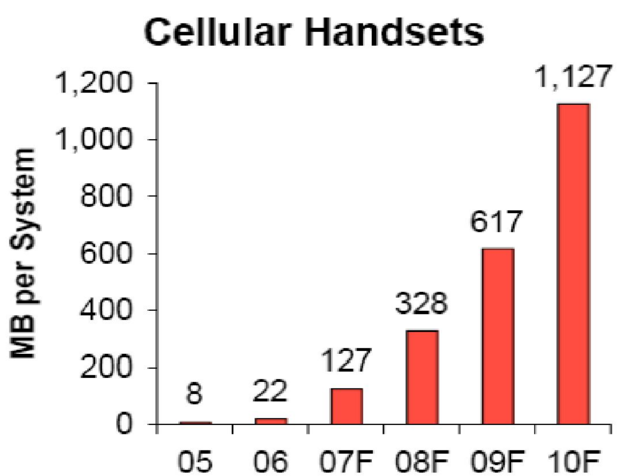


Flux 1 µp (~80,000 JJ)

Флеш-память: взрывное развитие







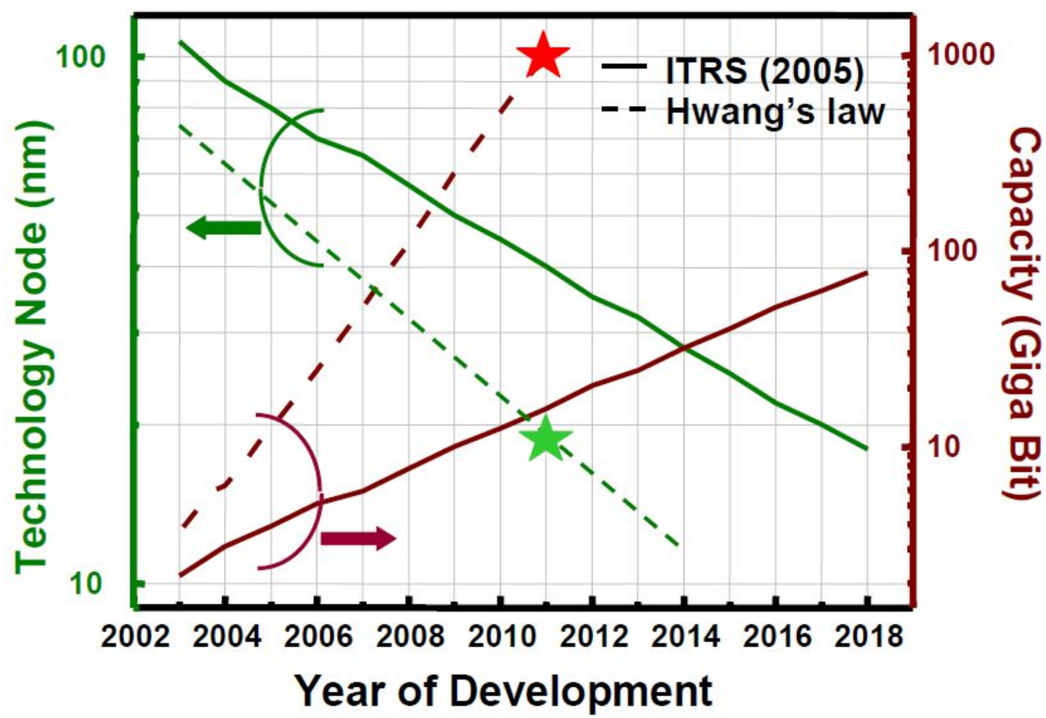
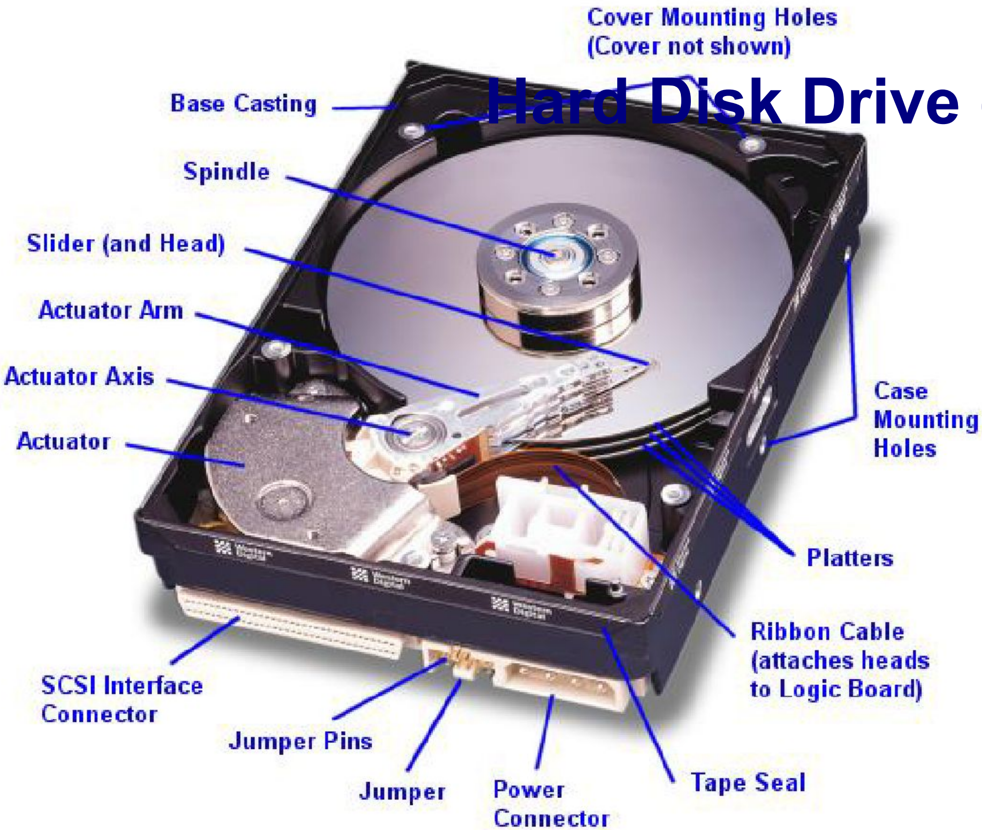


Figure courtesy: B. G. Park

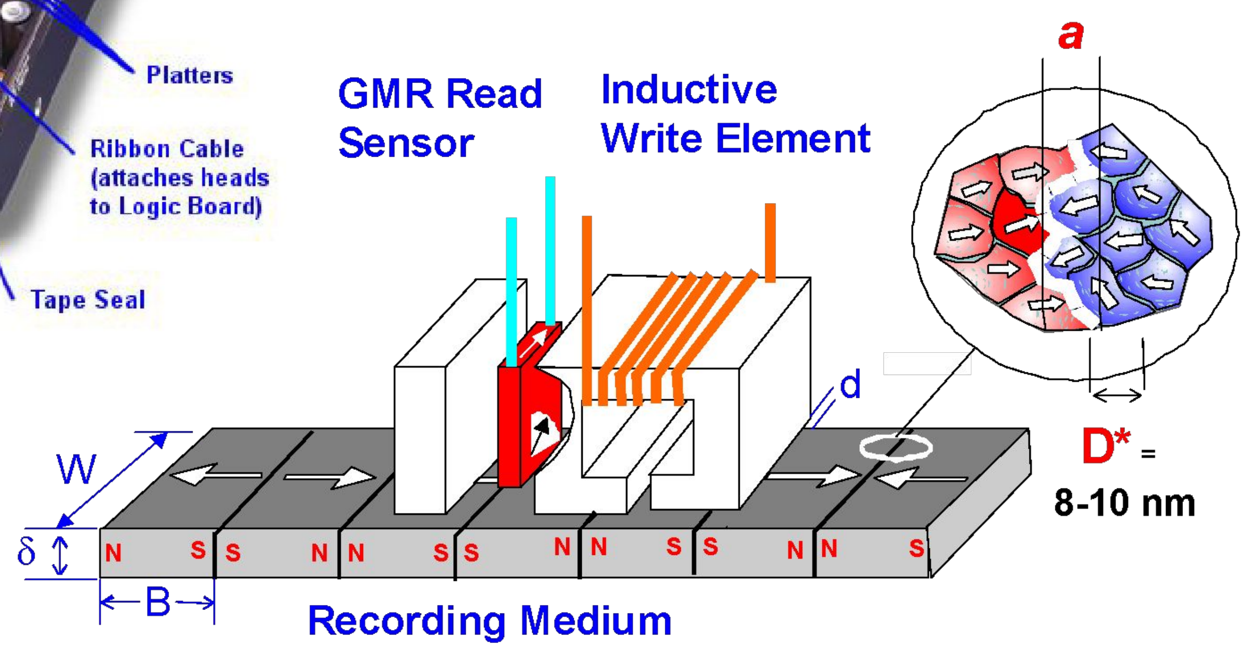
MAGNETIC RECORDING

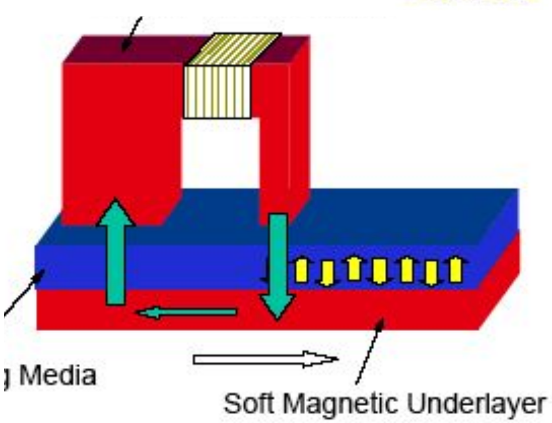
Hard Disk Drive (HDD)



7,200 rpm: ~10 m/s @ *h* ~10 nm

(for jet plane at *h* ~ 300 nm)





Courtesy: **U. Mastromatteo, STMicroelectronics**

MAGNETIC RECORDING: AREAL DENSITY AS OF 2001

Far insufficient! - KKL

Magnetic Stability

- **Magnetic Energy ~ Thermal Energy**

Superparamagnetic limit

Criterion:100 s at room temperature

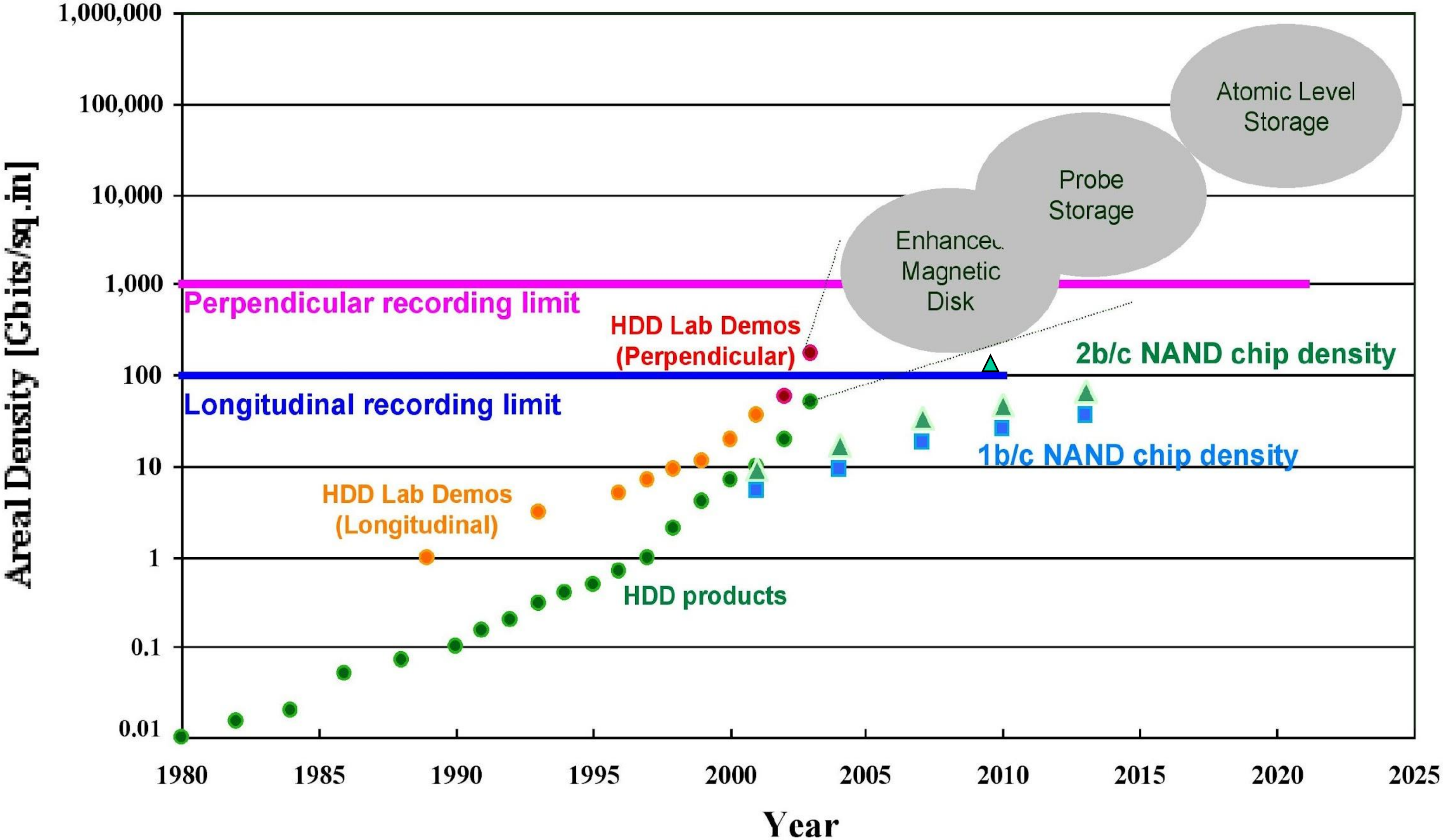
$$1/\tau = f_o e^{-KV/k_B T}$$

Material	Co	Fe			
Anisotropy	Crystalline	Crystalline	Shape Anisotropy		
Shape	Sphere (diameter *d*)	Sphere (diameter *d*)	Disc (diameter *d*, thickness *t*)		
			d/t=4	*d/t*=10	*d/t*=100
Anisotropy constant K (10^5erg/cm^3)	45	4.8	100	140	180
Volume V (10^{-19} cm^3)	2.3	21	1.0	0.74	0.55
Size *d* (Å)	76	160	80	100	191

- **Domain Size ~ Physical Size**
- **Proximity Effect**

Courtesy: I. Schuller, UCSD

NONVOLATILE MEMORY/STORAGE BATTLE



Courtesy: **U. Mastromatteo, STMicroelectronics**