

Lecture # 10

The Field-Effect Transistor (FETs). Junction Field-effect transistor fundamentals

Course: El 2207: Electronics

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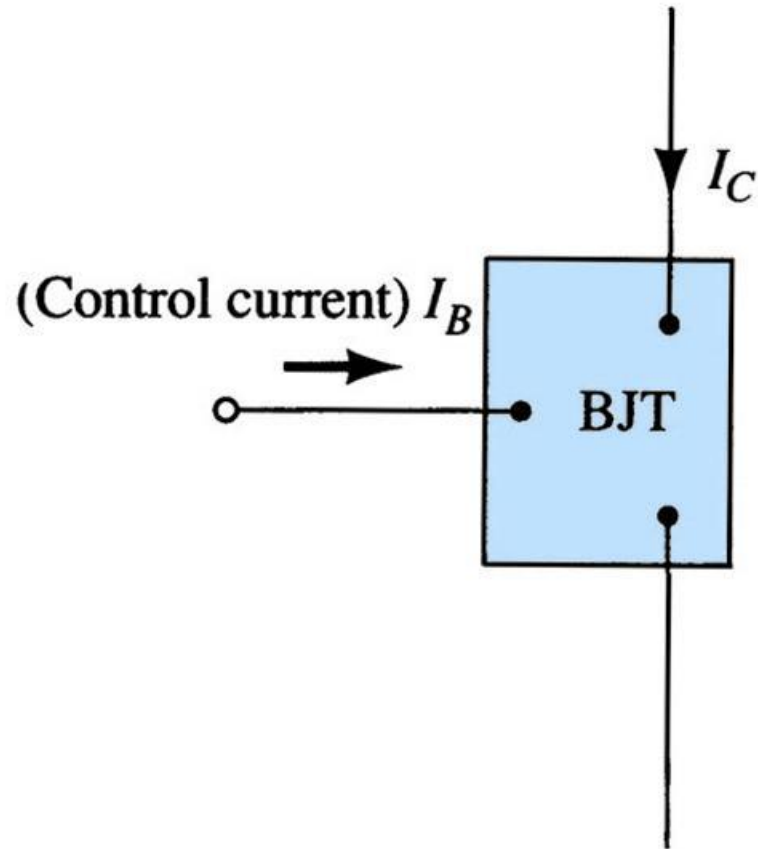
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Introduction (FET)

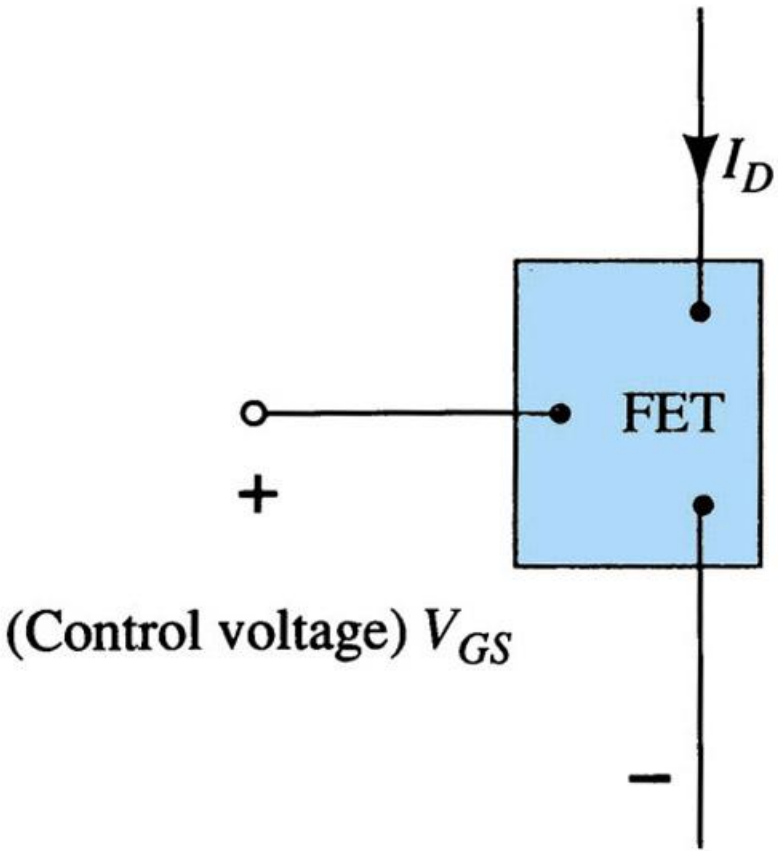
- Field-effect transistor (FET) are important devices such as BJTs
 - Also used as amplifier and logic switches
 - Types of FET:
 - JFET (junction field-effect transistor)
 - MOSFET (metal-oxide-semiconductor field-effect transistor)
 - What is the difference between JFET and MOSFET?
-

Current-controlled amplifiers



(a)

Voltage-controlled amplifiers



(b)

Introduction.. (Advantages of FET)

- High input impedance ($M\Omega$)
(Linear AC amplifier system)
- Temperature stable than BJT
- Smaller than BJT
- Can be fabricated with fewer processing
- BJT is bipolar – conduction both hole and electron
- FET is unipolar – uses only one type of current carrier
- Less noise compare to BJT
- Usually use as logic switch

Disadvantages of FET

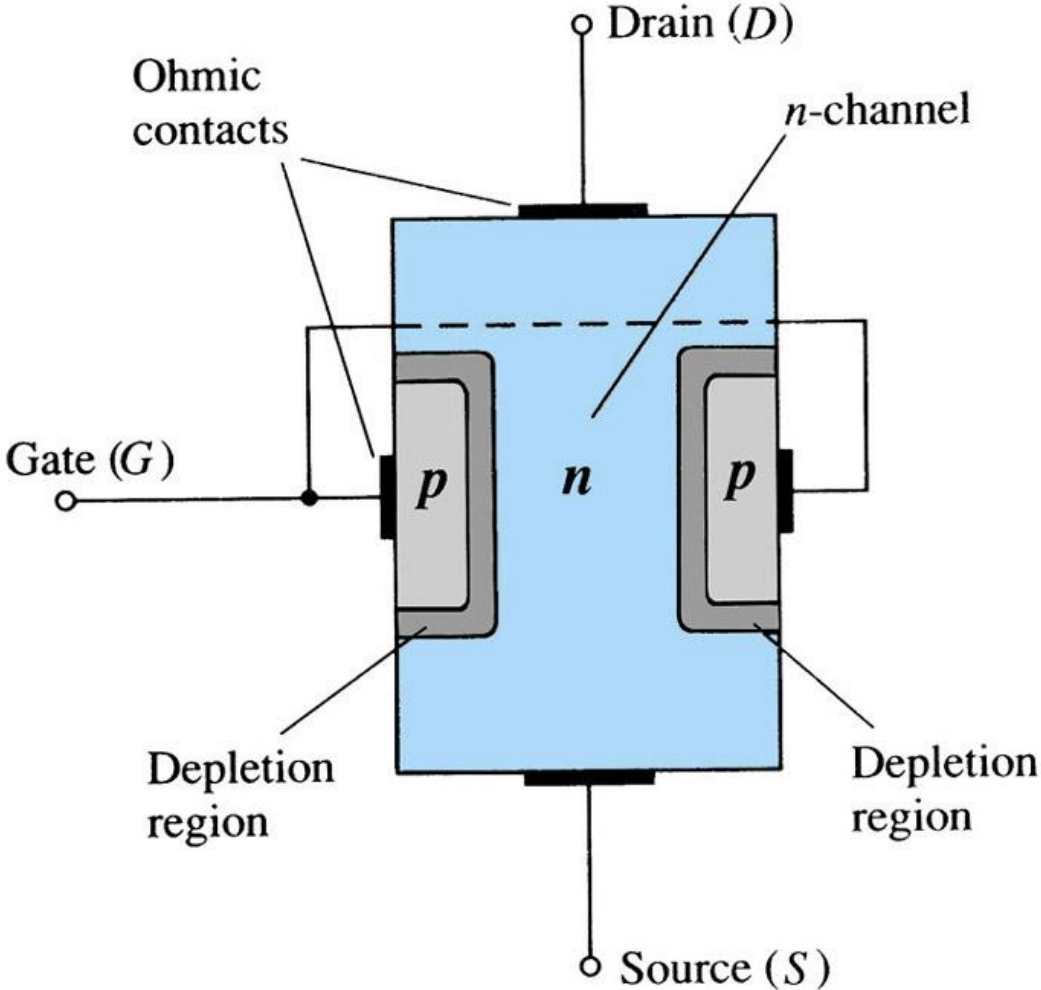
- Easy to damage compare to BJT
 - ???
-

Junction field-effect transistor..

- There are 2 types of JFET
 - n-channel JFET
 - p-channel JFET

 - Three Terminal
 - **gate:** as in the “gate” keeper of the current
 - **source:** the source of the current
 - **drain:** the destination of the current
-

Junction field-effect transistor (JFET)

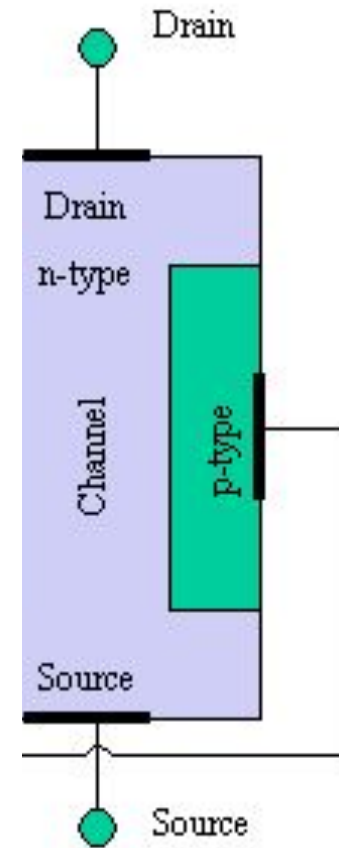
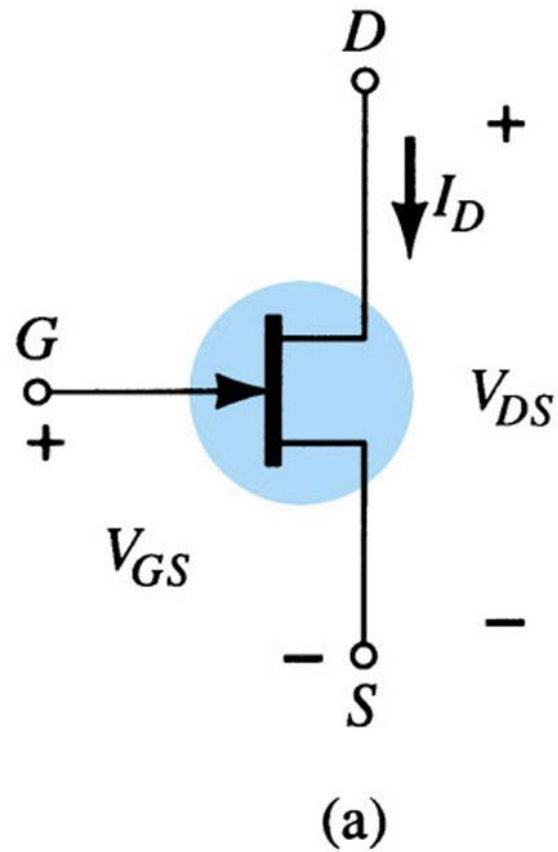


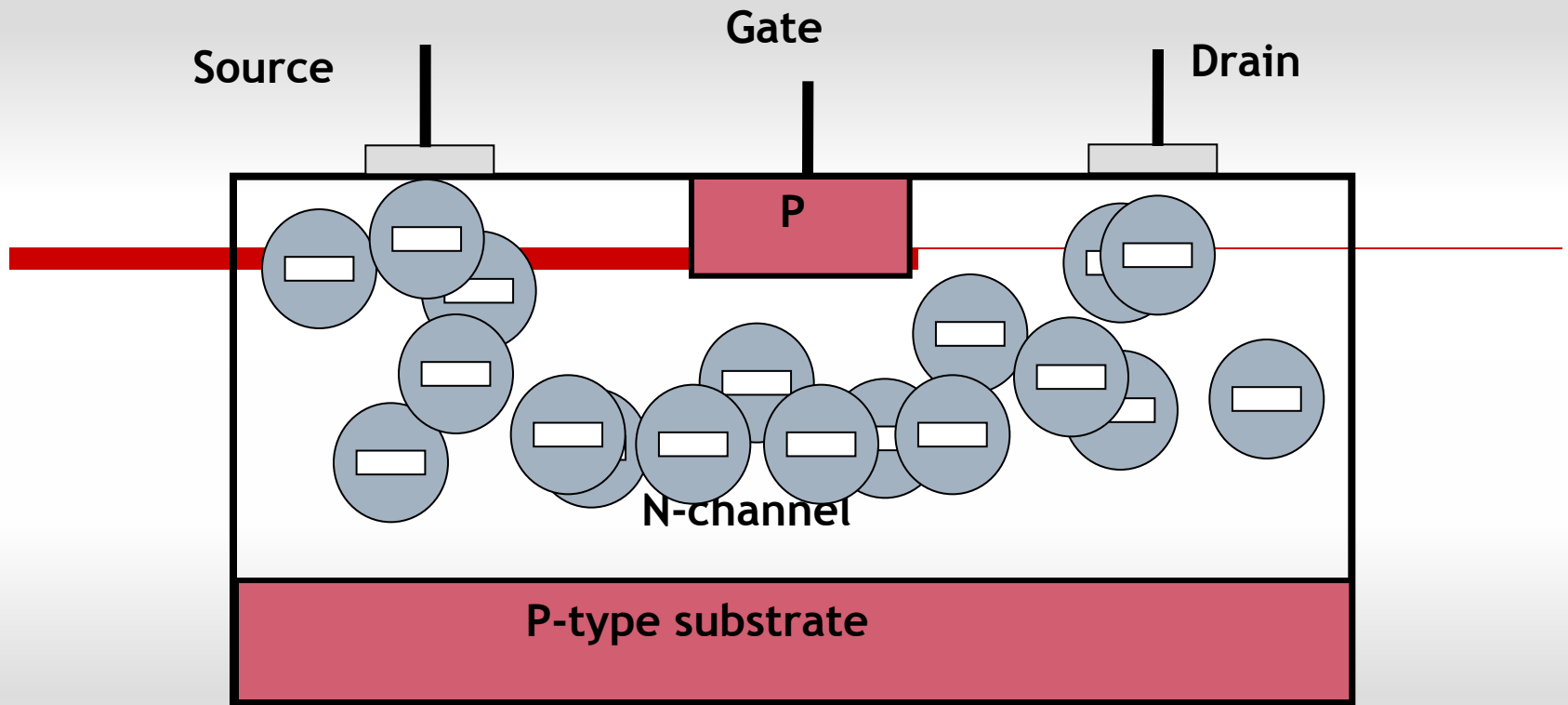
N-channel JFET

□ N channel JFET:

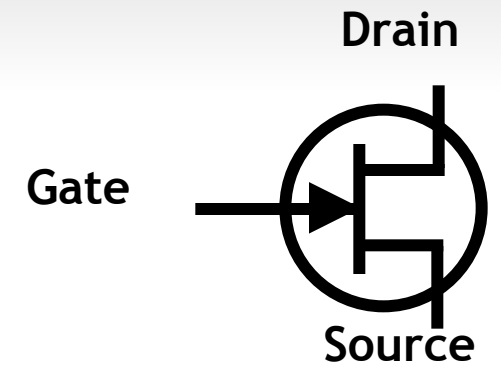
- Major structure is **n-type material (channel)** between embedded **p-type material** to form 2 p-n junction.
 - In the normal operation of an n-channel device, the **Drain (D)** is positive with respect to the **Source (S)**. Current flows into the Drain (D), through the channel, and out of the Source (S)
 - Because the resistance of the channel depends on the **gate-to-source voltage (V_{GS})**, the **drain current (I_D)** is controlled by that voltage
-

N-channel JFET..

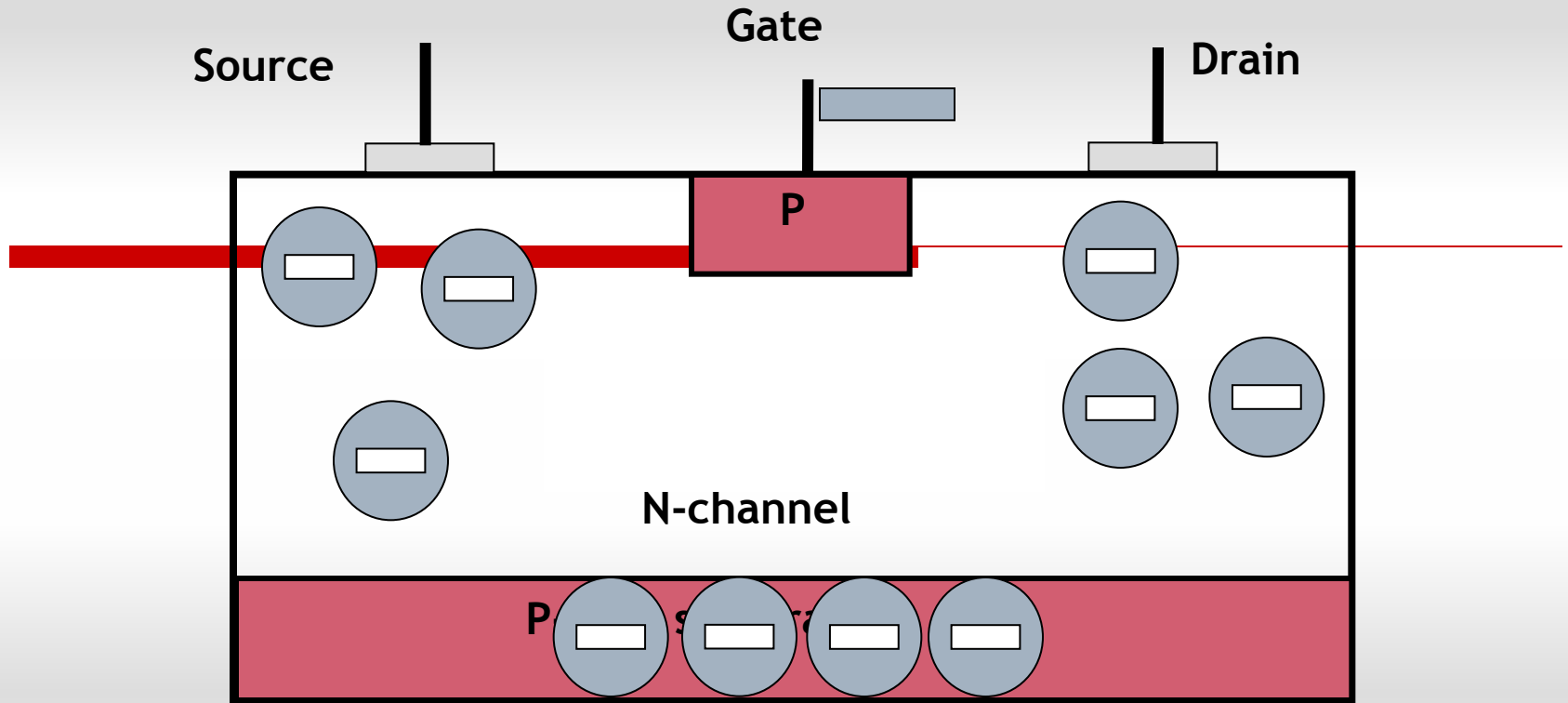




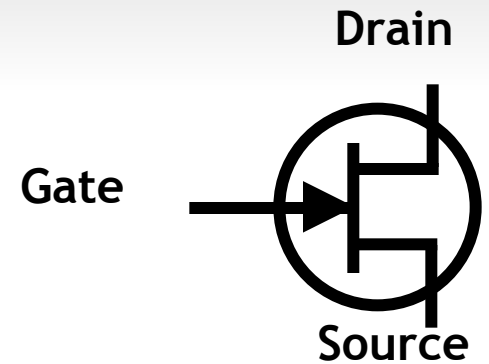
Structure of an N-channel JFET



The channel has carriers so
it
conducts from source to



A negative gate voltage
 can push the carriers
 from
 the channel and turn
 the JFET off

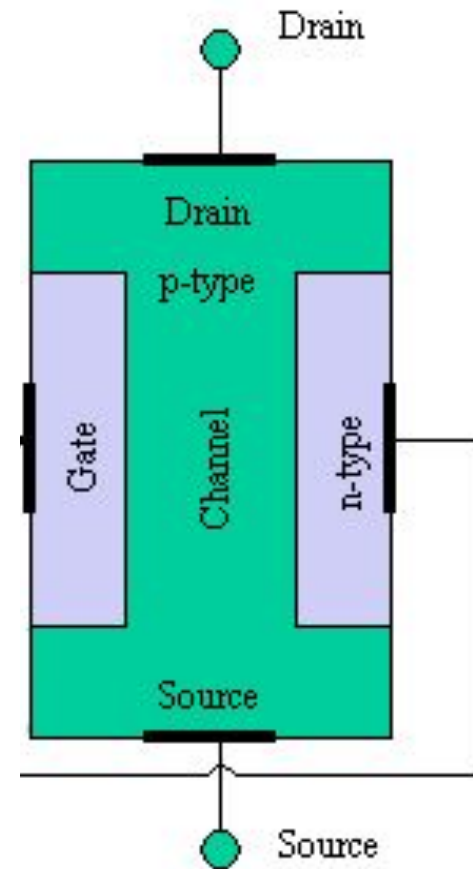
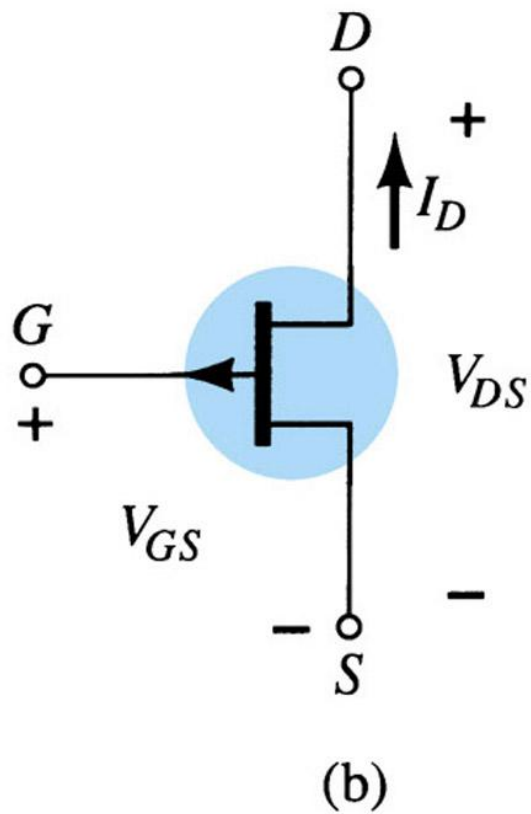


P-channel JFET

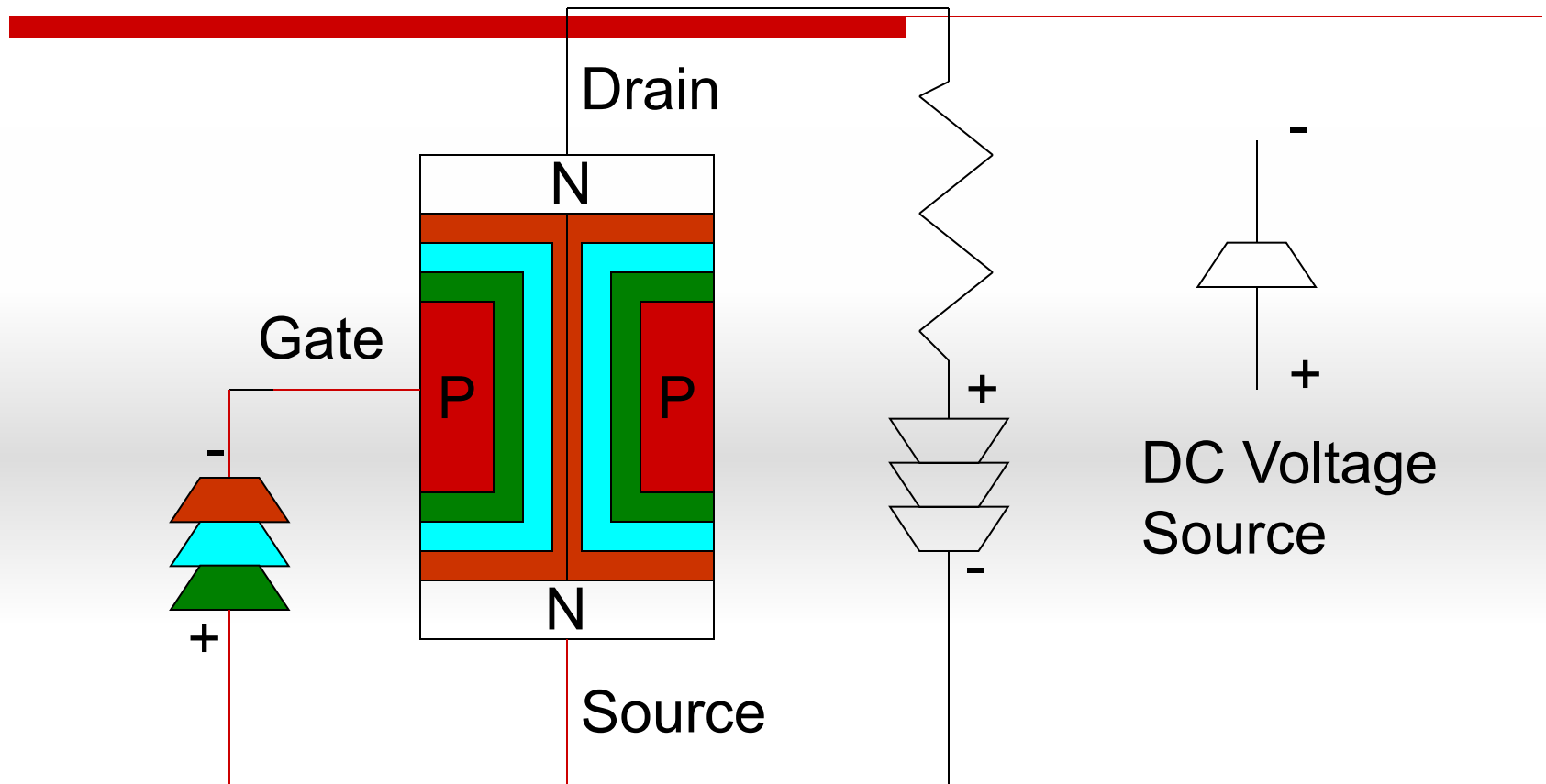
□ P channel JFET:

- Major structure is p-type material (channel) between embedded n-type material to form 2 p-n junction.
 - Current flow : from Source (S) to Drain (D)
 - Holes injected to Source (S) through p-type channel and flowed to Drain (D)
-

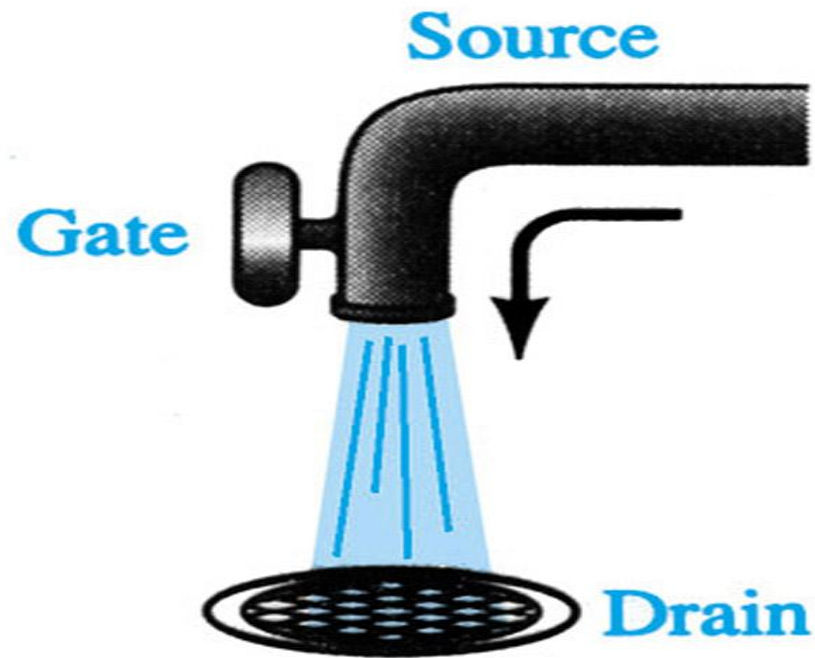
P-channel JFET..



Operation of a JFET



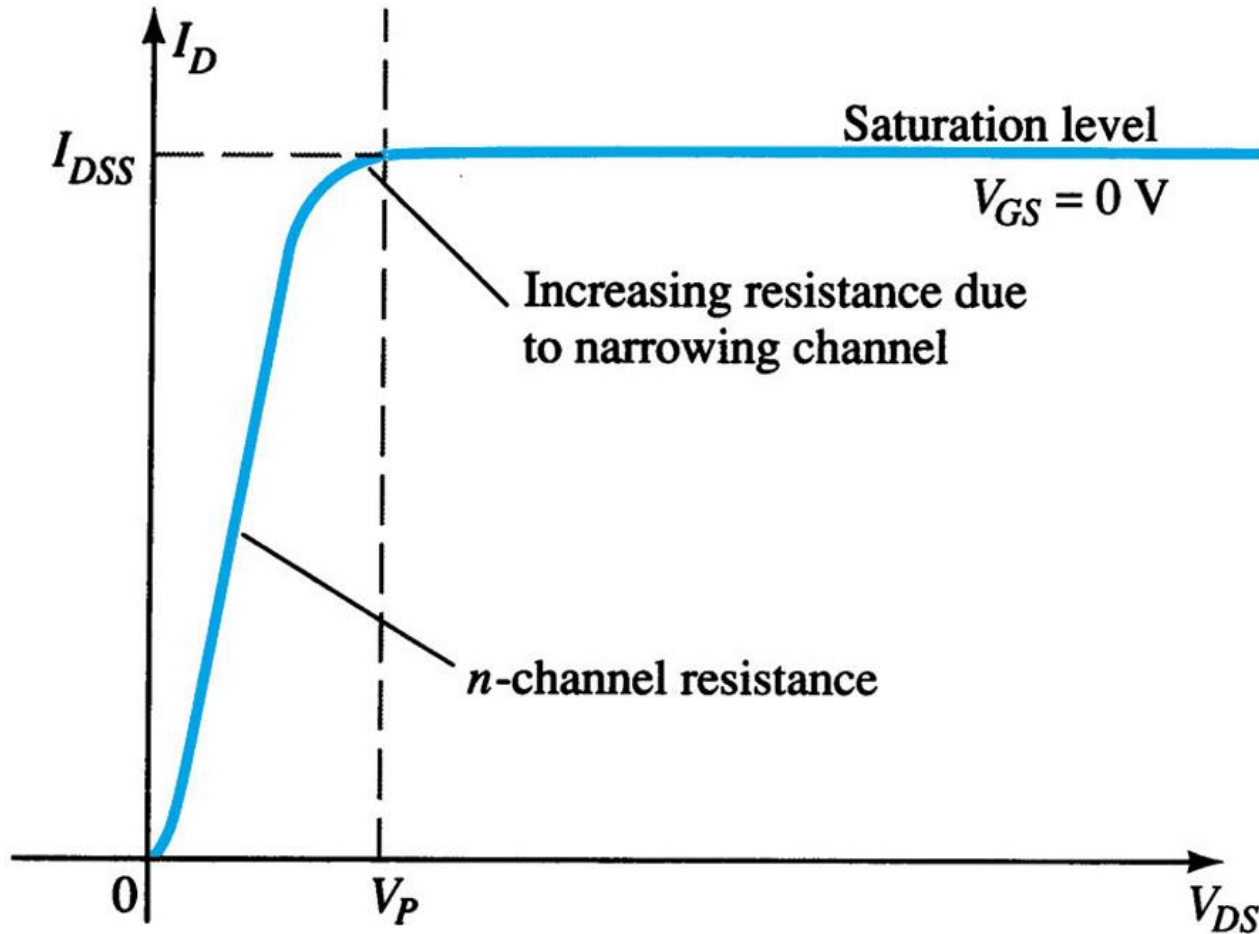
Water analogy for the JFET control mechanism



JFET Characteristic Curve

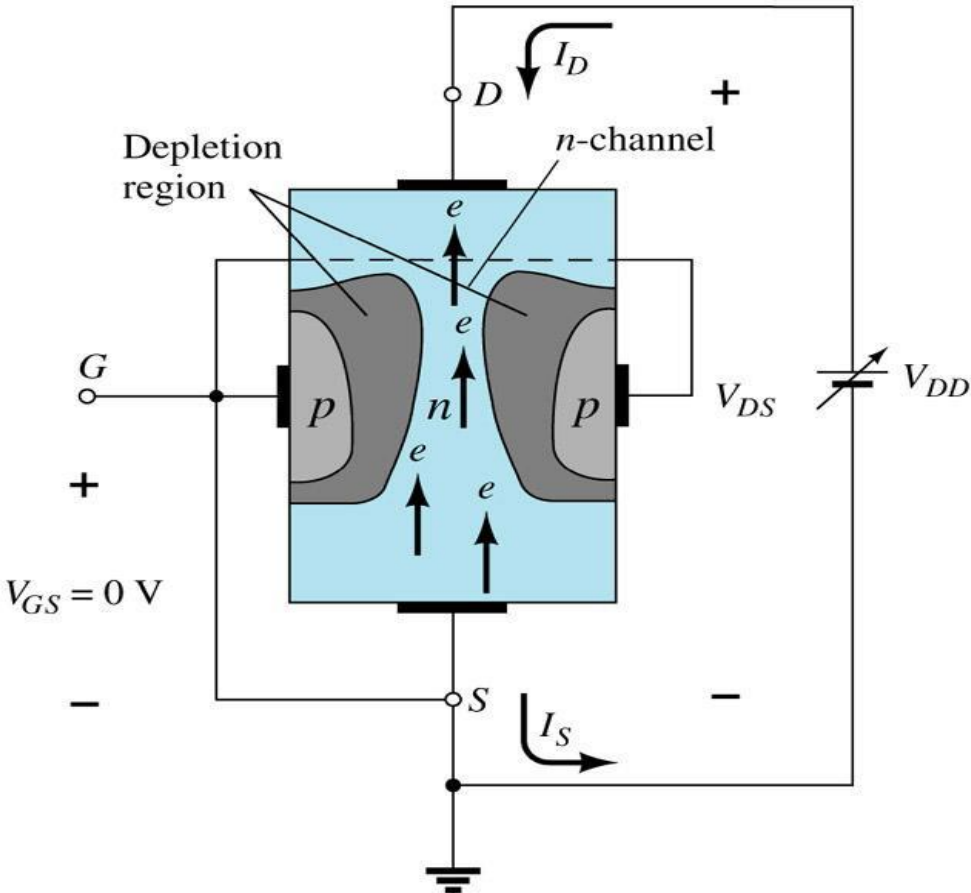
- To start, suppose $V_{GS} = 0$
 - Then, when V_{DS} is increased, I_D increases. Therefore, I_D is proportional to V_{DS} for small values of V_{DS}
 - For larger value of V_{DS} , as V_{DS} increases, the depletion layer become wider, causing the resistance of channel increases.
 - After the pinch-off voltage (V_p) is reached, the I_D becomes nearly constant (called as I_D maximum, I_{DSS} -Drain to Source current with Gate Shorted)
-

I_D versus V_{DS} for $V_{GS} = 0$ V.



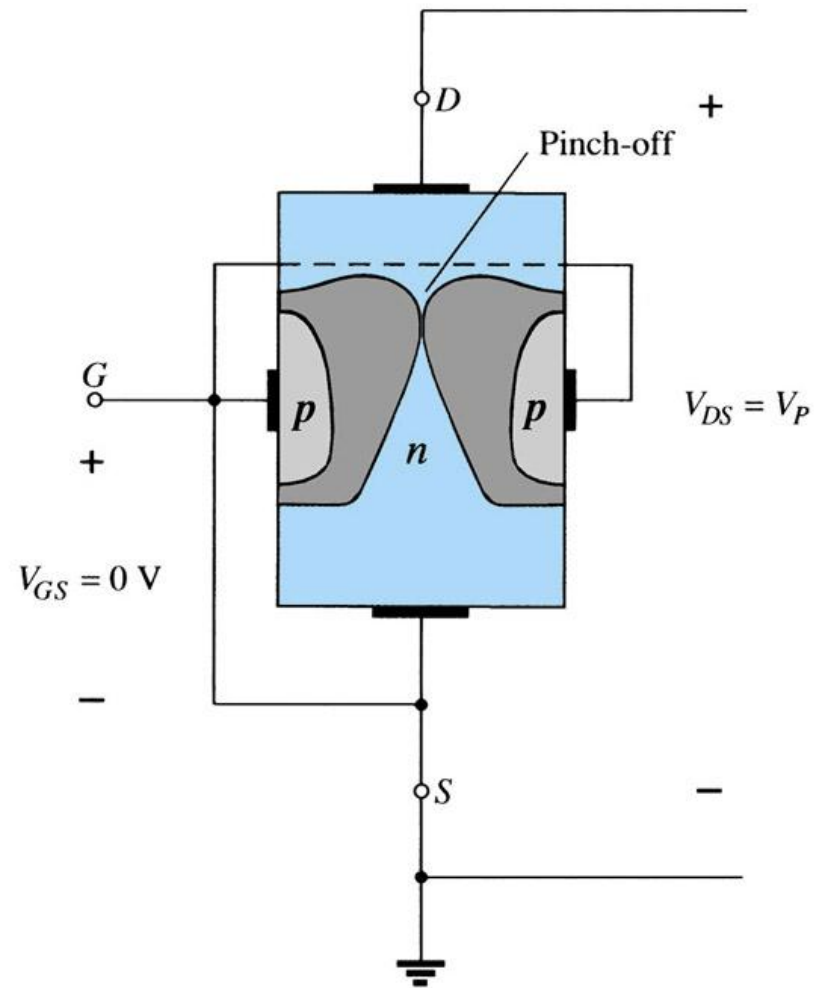
JFET Characteristic Curve

JFET for $V_{GS} = 0 \text{ V}$ and $0 < V_{DS} < |V_p|$

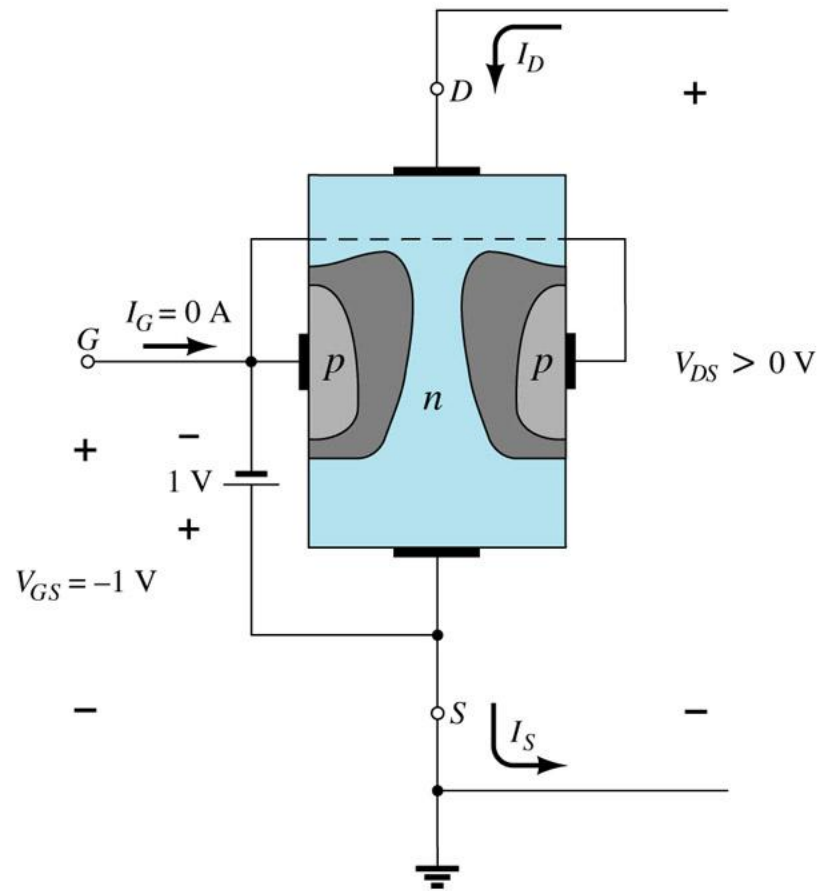


Channel becomes narrower as V_{DS} is increased

Pinch-off ($V_{GS} = 0 \text{ V}$, $V_{DS} = V_P$).

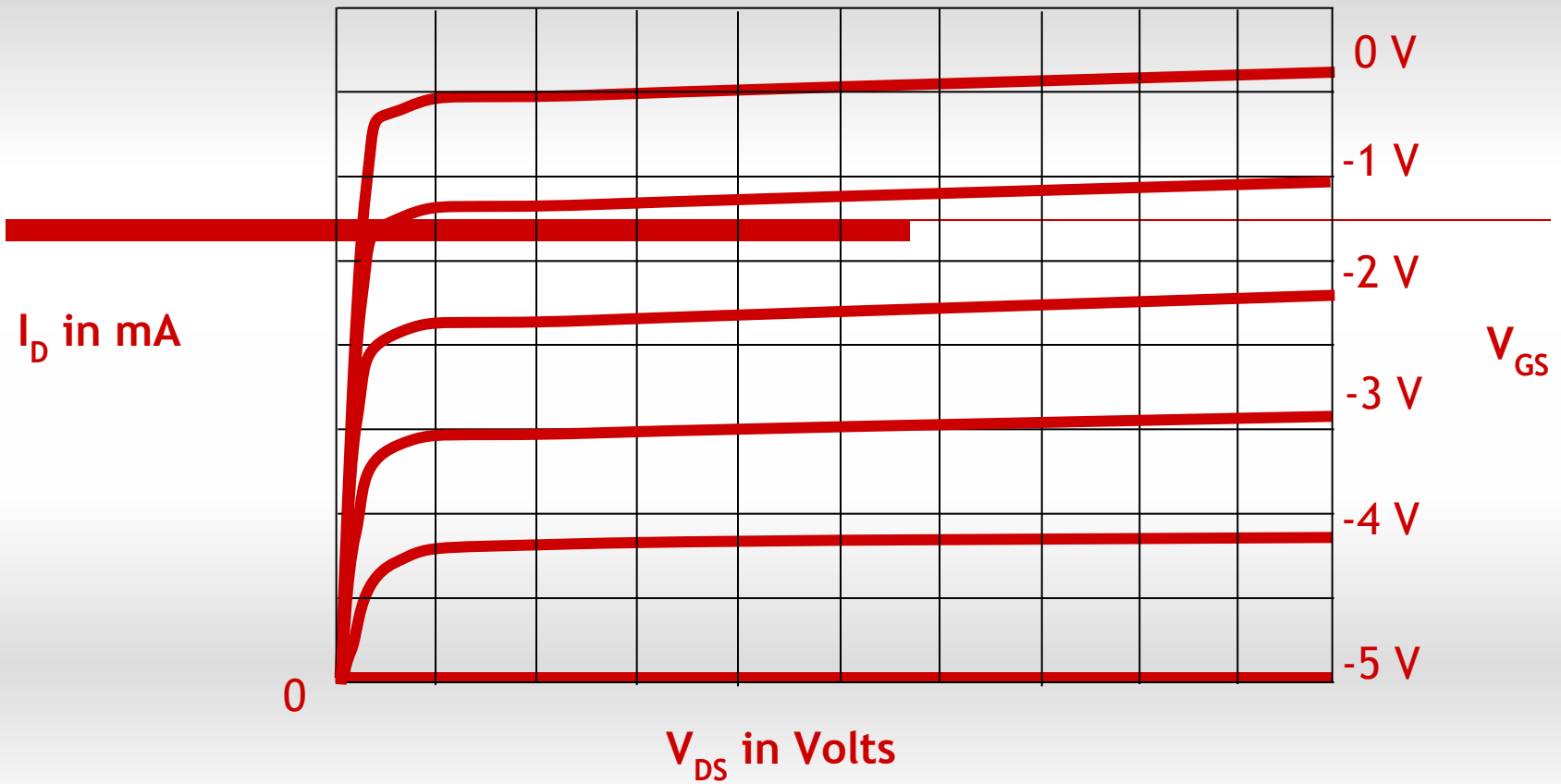


Application of a negative voltage to the gate of a JFET.



JFET Characteristic Curve..

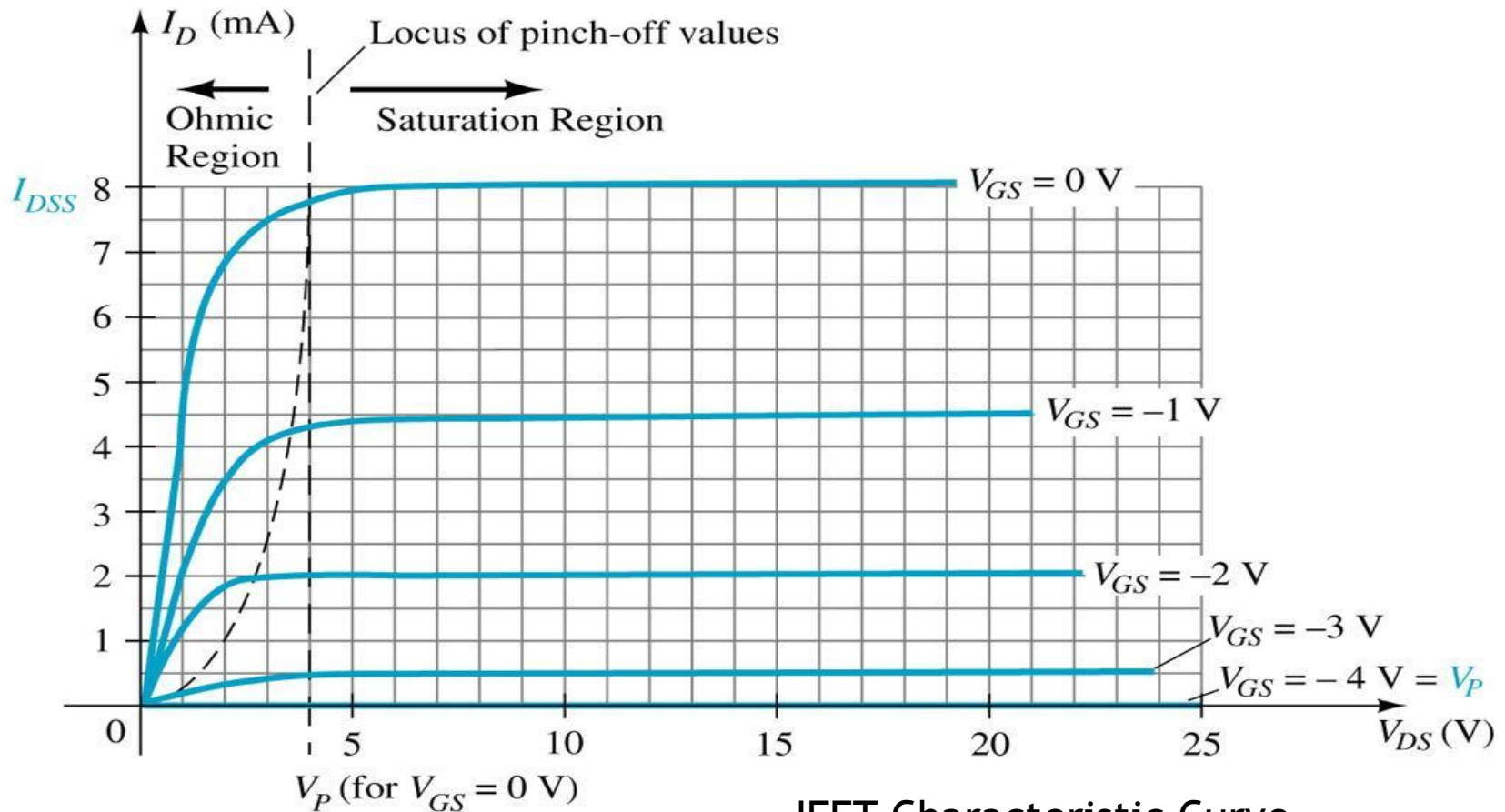
- For negative values of V_{GS} , the gate-to-channel junction is reverse biased even with $V_{DS}=0$
- Thus, the initial channel resistance is higher (in which the initial slope of the curves is smaller for values of V_{GS} closer to the pinch-off voltage (V_p))
- The resistance value is under the control of V_{GS}
- If V_{GS} is less than pinch-off voltage, the resistance becomes an open-circuit ;therefore the device is in **cutoff ($V_{GS}=V_{GS(off)}$)**
- The region where I_D constant – The **saturation/pinch-off region**
- The region where I_D depends on V_{DS} is called the **linear/triode/ohmic region**



This is known as a depletion-mode device.

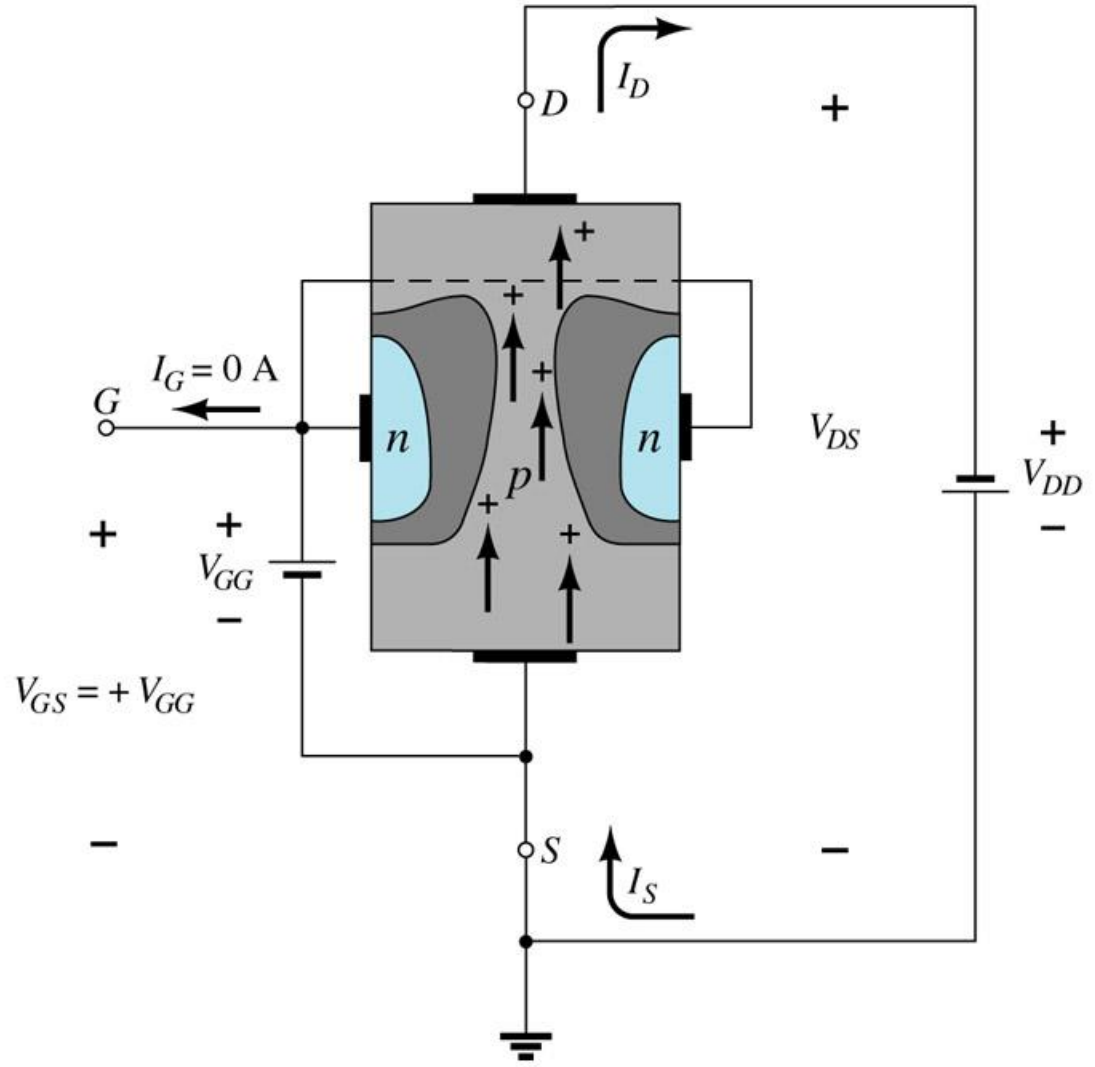
N-channel JFET drain family of characteristic curves

n -Channel JFET characteristics curve with $I_{DSS} = 8 \text{ mA}$ and $V_P = -4 \text{ V}$.

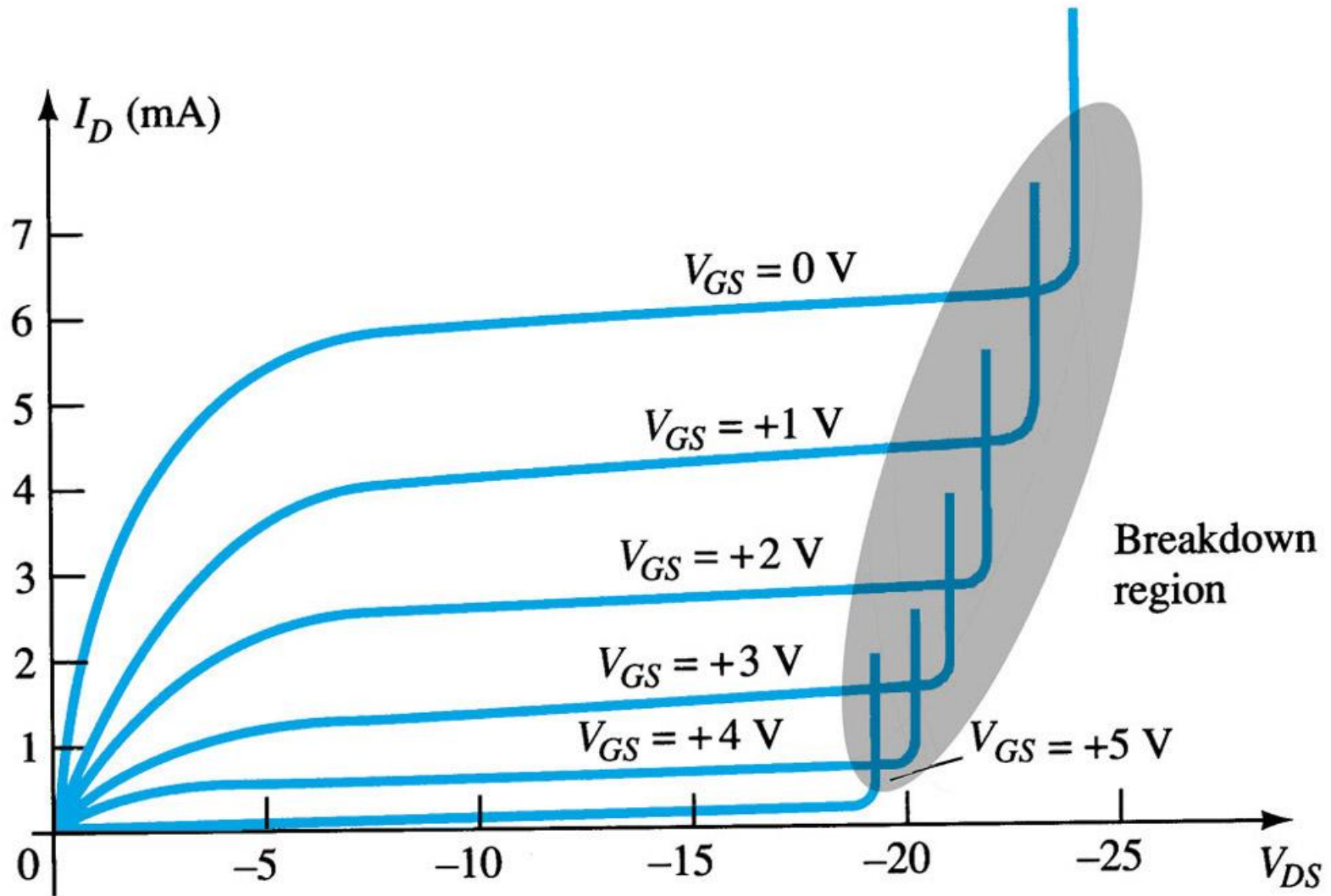


JFET Characteristic Curve

p-Channel JFET

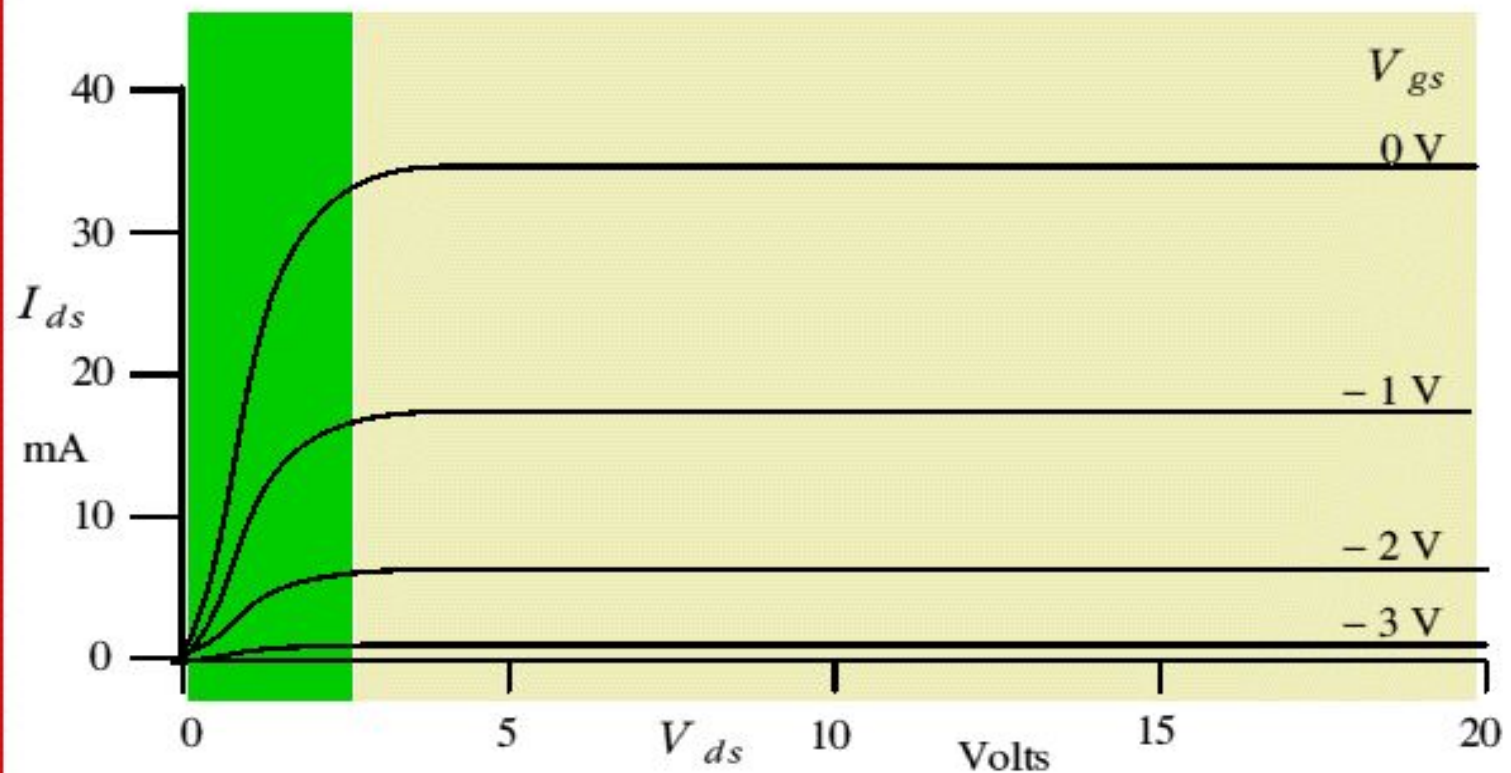


p -Channel JFET characteristics with $I_{DSS} = 6$ mA



Characteristics for n-channel JFET

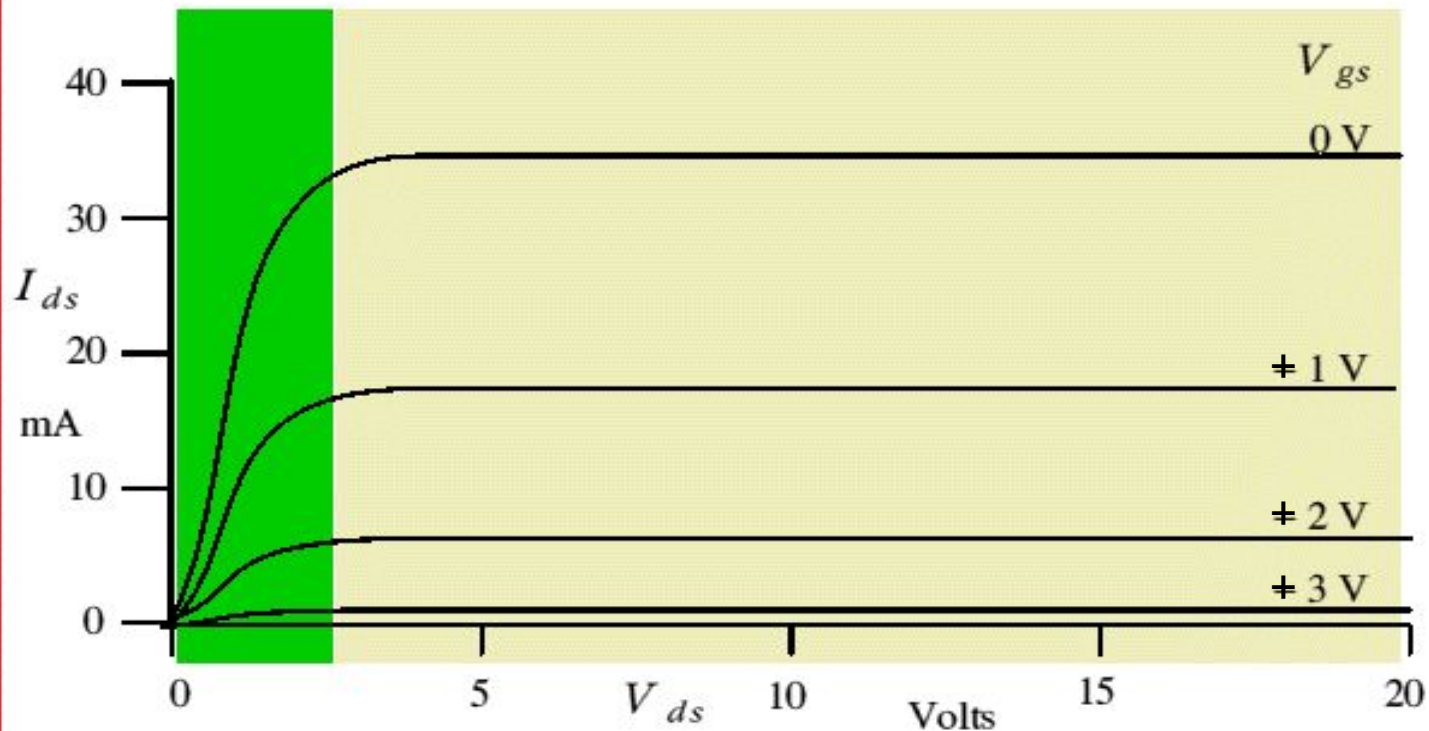
I_{ds} = drain-source current V_{ds} = drain-source voltage V_{gs} = gate-source voltage



'Characteristic curves for a typical N-channel JFET.

Characteristics for p-channel JFET

I_{ds} = drain-source current V_{ds} = drain-source voltage V_{gs} = gate-source voltage



'Characteristic curves for a typical P -channel JFET.

Operation of n-channel JFET

- JFET is biased with two voltage sources:
 - V_{DD}
 - V_{GG}
- V_{DD} generate voltage bias between Drain (D) and Source (S) – V_{DS}
- V_{DD} causes **drain current**, I_D flows from Drain (D) to Source (S)
- V_{GG} generate voltage bias between Gate (G) and Source (S) with negative polarity source is connected to the Gate Junction (G) – reverse-biases the gate; therefore **gate current**, $I_G = 0$.
- V_{GG} is to produce depletion region in N channel so that it can control the amount of drain current, I_D that flows through the channel

Transfer Characteristics

The input-output transfer characteristic of the JFET is not as straight forward as it is for the BJT. In BJT:

$$I_C = \beta I_B$$

which β is defined as the relationship between I_B (input current) and I_C (output current).

Transfer Characteristics..

In JFET, the relationship between V_{GS} (input voltage) and I_D (output current) is used to define the transfer characteristics. It is called as Shockley's Equation:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2 \quad V_P = V_{GS(OFF)}$$

The relationship is more complicated (and not linear)

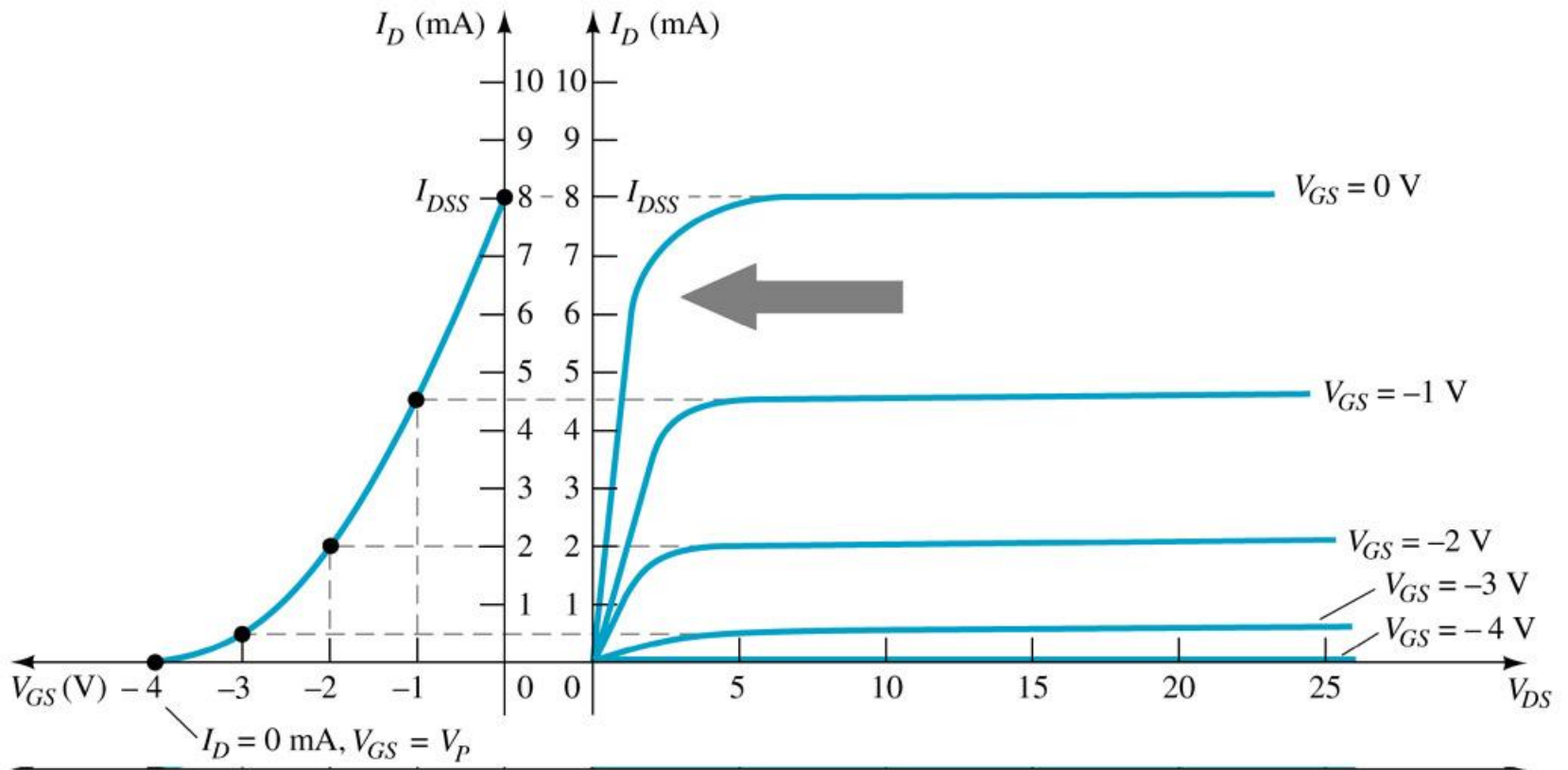
As a result, FET's are often referred to a square law devices

Transfer Characteristics...

- Defined by Shockley's equation:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(off)}} \right)^2 \qquad V_P = V_{GS(off)}$$

- Relationship between I_D and V_{GS} .
 - Obtaining transfer characteristic curve axis point from Shockley:
 - When $V_{GS} = 0 \text{ V}$, $I_D = I_{DSS}$
 - When $V_{GS} = V_{GS(off)}$ or V_P , $I_D = 0 \text{ mA}$
-



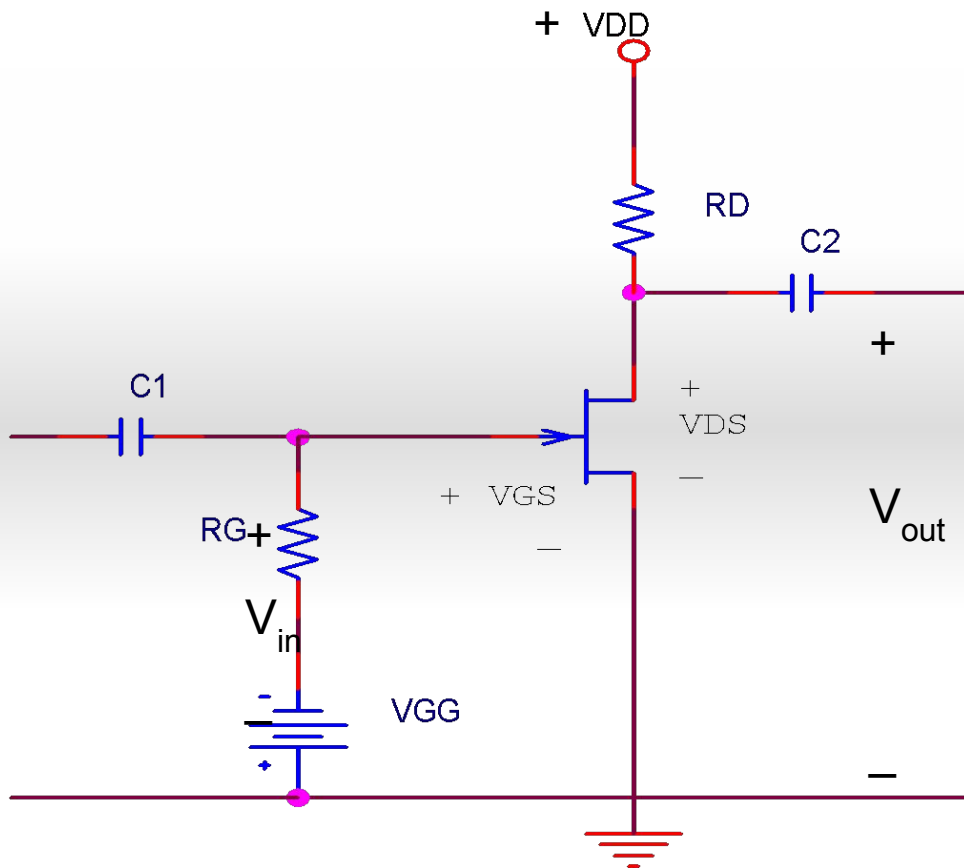
JFET Transfer Characteristic Curve

JFET Characteristic Curve

DC JFET Biasing

- Just as we learned that the BJT must be biased for proper operation, the JFET also must be biased for operation point (I_D , V_{GS} , V_{DS})
 - In most cases the ideal Q-point will be at the **middle** of the transfer characteristic curve, which is **about half of the I_{DSS}** .
 - 3 types of DC JFET biasing configurations :
 - Fixed-bias
 - Self-bias
 - Voltage-Divider Bias
-

Fixed-bias

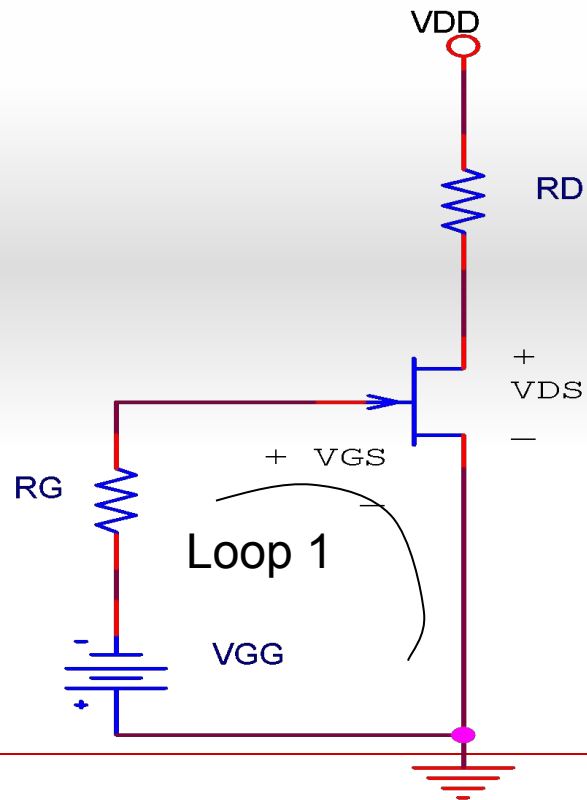


Fixed-bias

- Use two voltage sources: V_{GG} , V_{DD}
- V_{GG} is reverse-biased at the Gate - Source (G-S) terminal, thus no current flows through R_G ($I_G = 0$).

Fixed-bias..

- DC analysis
 - All capacitors replaced with open-circuit



Fixed-bias...

1. Input Loop

- By using KVL at loop 1:

$$\begin{aligned} V_{GG} + V_{GS} &= 0 \\ V_{GS} &= -V_{GG} \end{aligned}$$

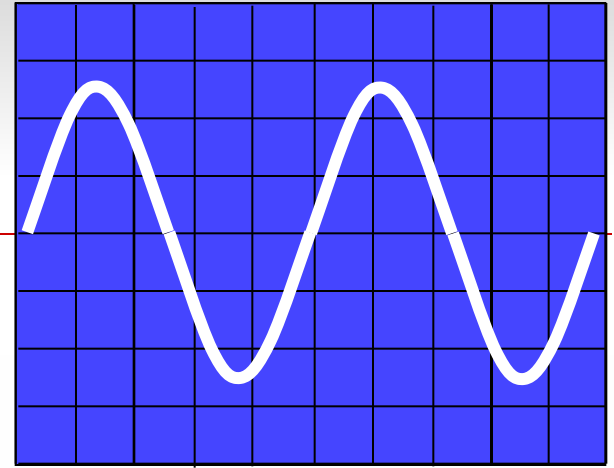
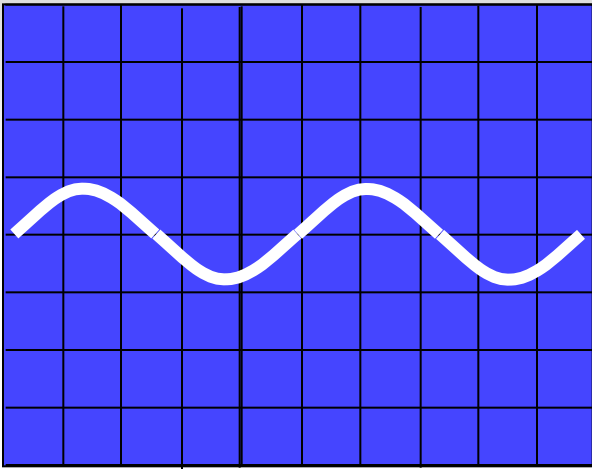
- For graphical solution, use $V_{GS} = -V_{GG}$ to draw the load line
- For mathematical solution, replace $V_{GS} = -V_{GG}$ in Shockley's Eq. ,therefore:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GS(off)}} \right)^2 = I_{DSS} \left(1 + \frac{V_{GG}}{V_{GS(off)}} \right)^2$$

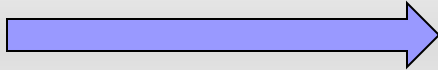
2. Output loop

$$\begin{aligned} -V_{DD} + I_D R_D + V_{DS} &= 0 \\ V_{DS} &= V_{DD} - I_D R_D \end{aligned}$$

- 3. Then, plot transfer characteristic curve by using Shockley's Equation

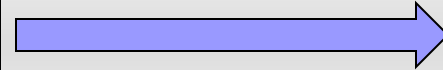


Voltage In



**Voltage
Amplifie**

Current Out



The JFET is
a voltage
controlled
amplifier.

