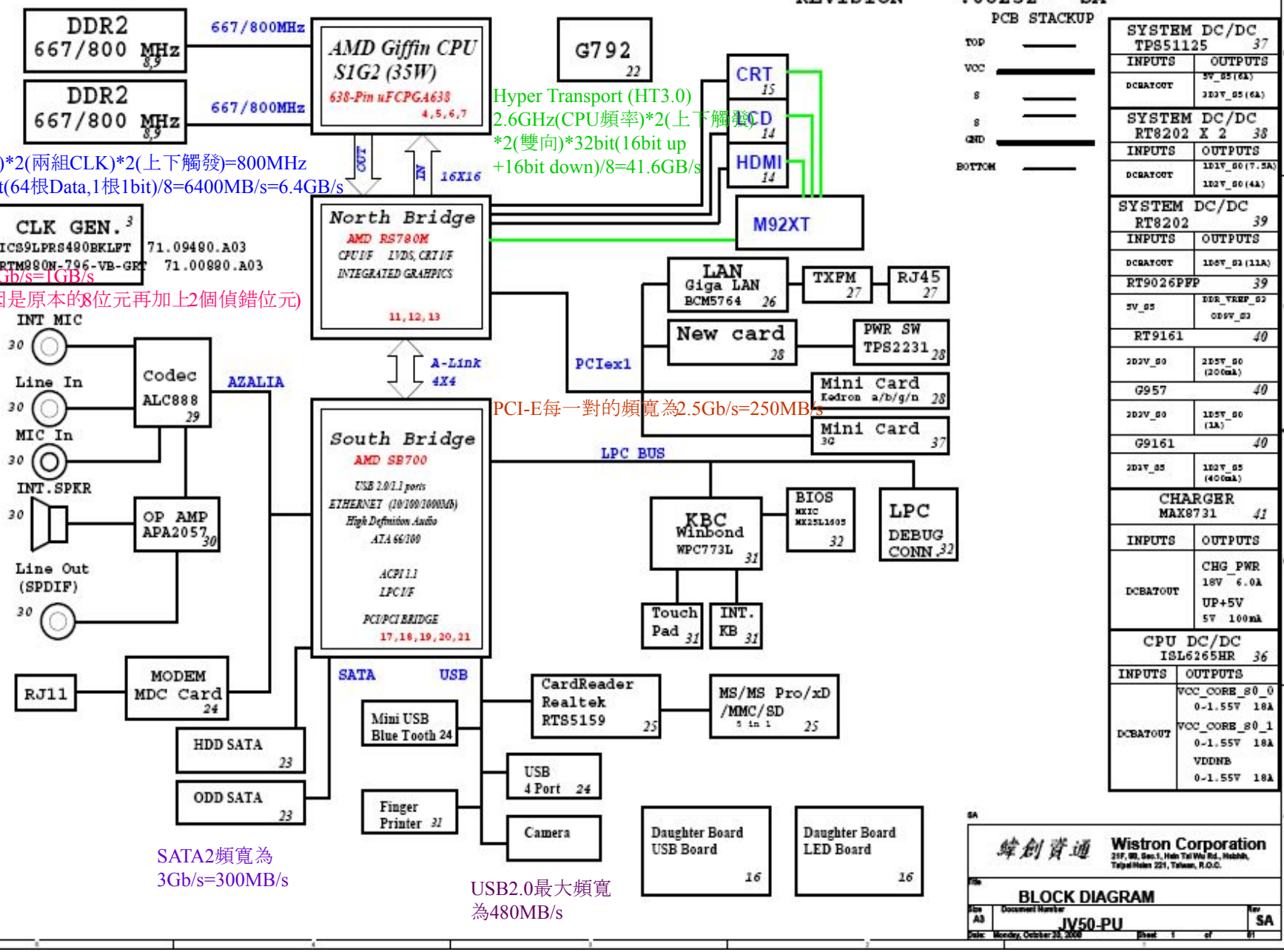
JV50-PU Block Diagram

Project code: 91.4CH01.001
PCB P/N : 48.4C901.001
REVISION :08252- -SA



PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC TPS51125 37	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 (6A) 3D3V_S5 (6A)

SYSTEM DC/DC RT8202 X 2 38	
INPUTS	OUTPUTS
DCBATOUT	1D1V_S0 (7.5A) 1D2V_S0 (4A)

SYSTEM DC/DC RT8202 39	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 (11A)

RT9026PFP 39	
5V_S5	DDR_VREF_S3 OD5V_S3

RT9161 40	
2D2V_S0	2D5V_S0 (200mA)

G957 40	
2D2V_S0	1D5V_S0 (1A)

G9161 40	
2D1V_S5	1D2V_S5 (400mA)

CHARGER MAX8731 41	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265HR 36	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A VCC_CORE_S0_1 0~1.55V 18A VDDNB 0~1.55V 18A

Wistron Corporation

BLOCK DIAGRAM

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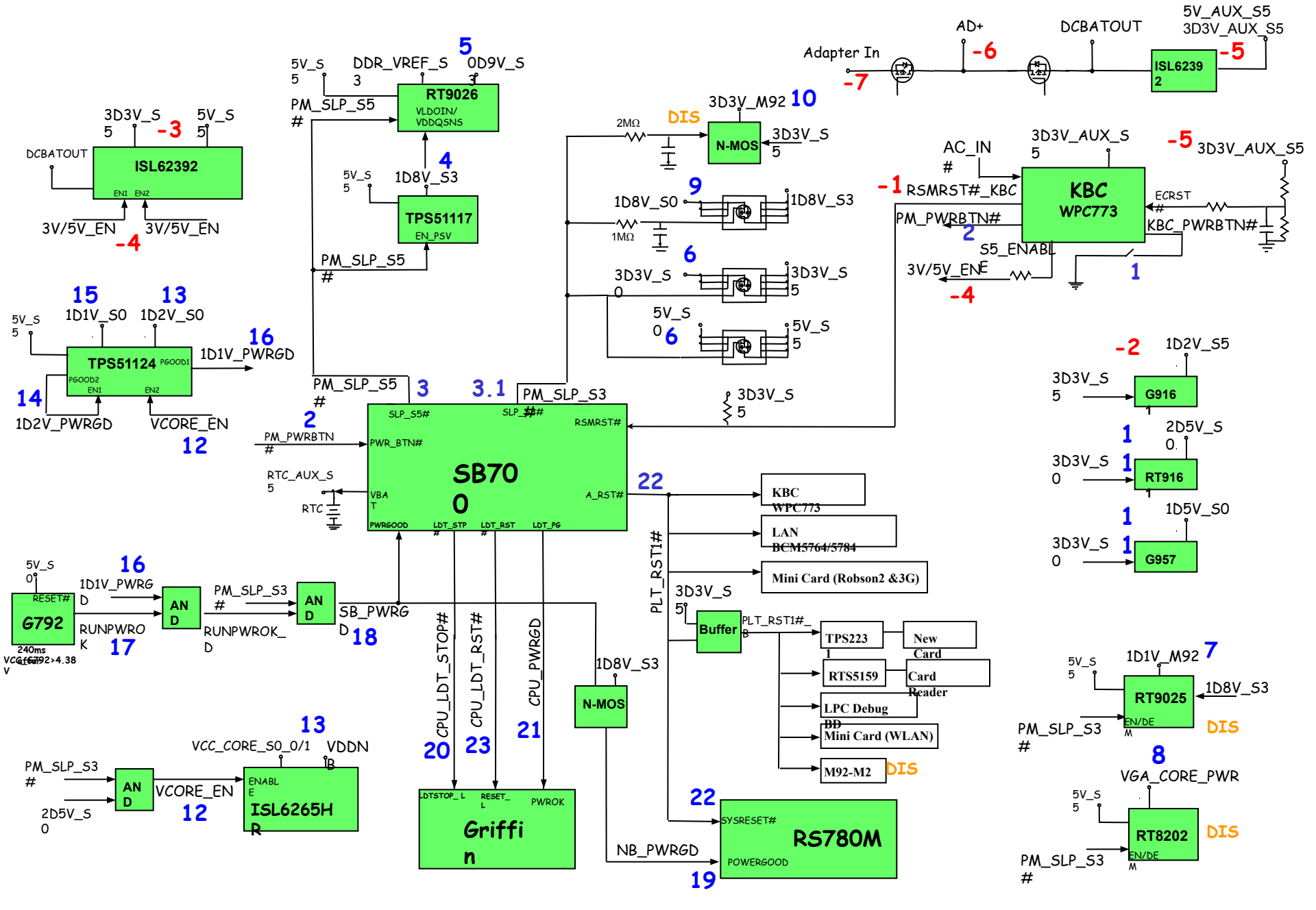
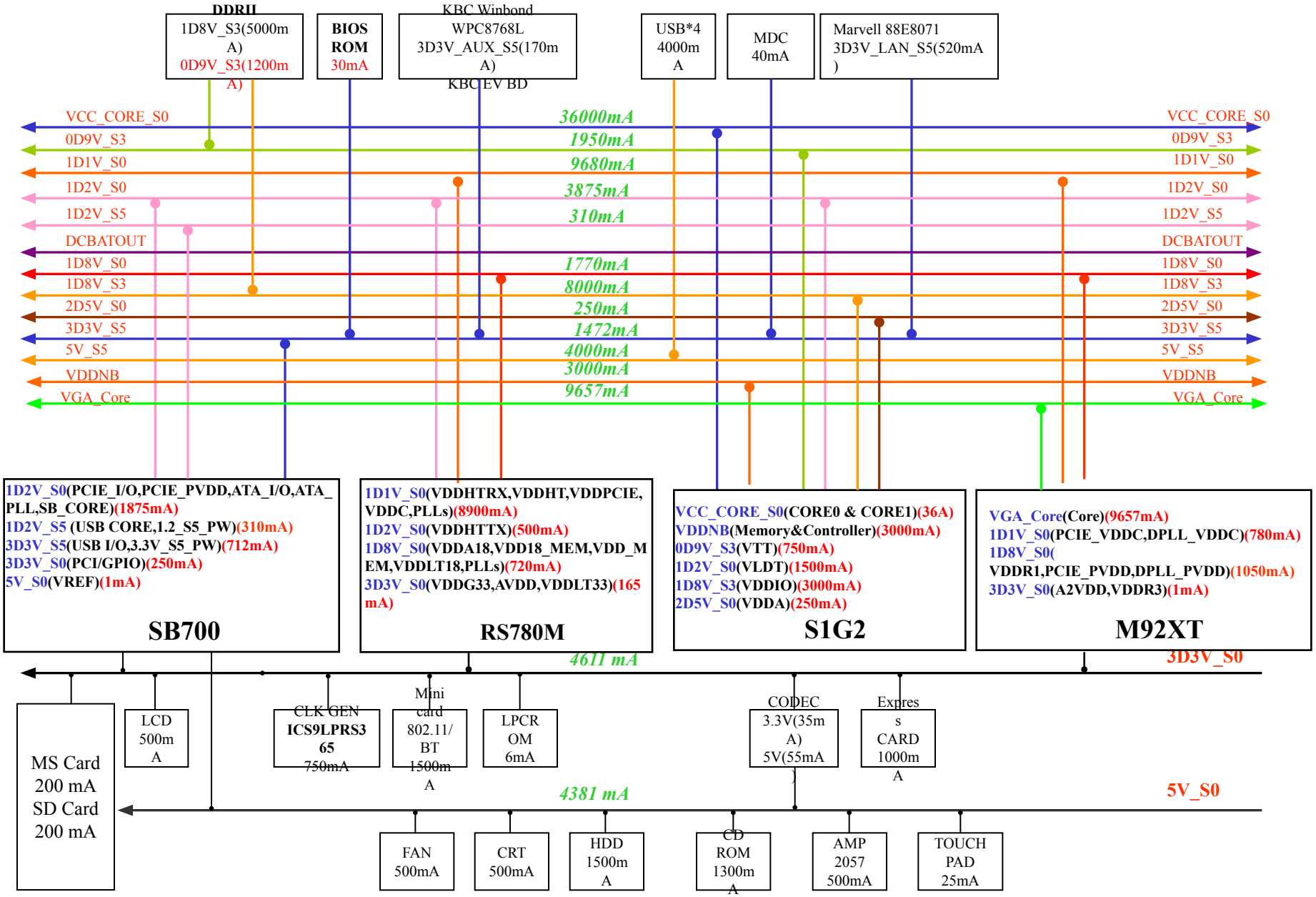
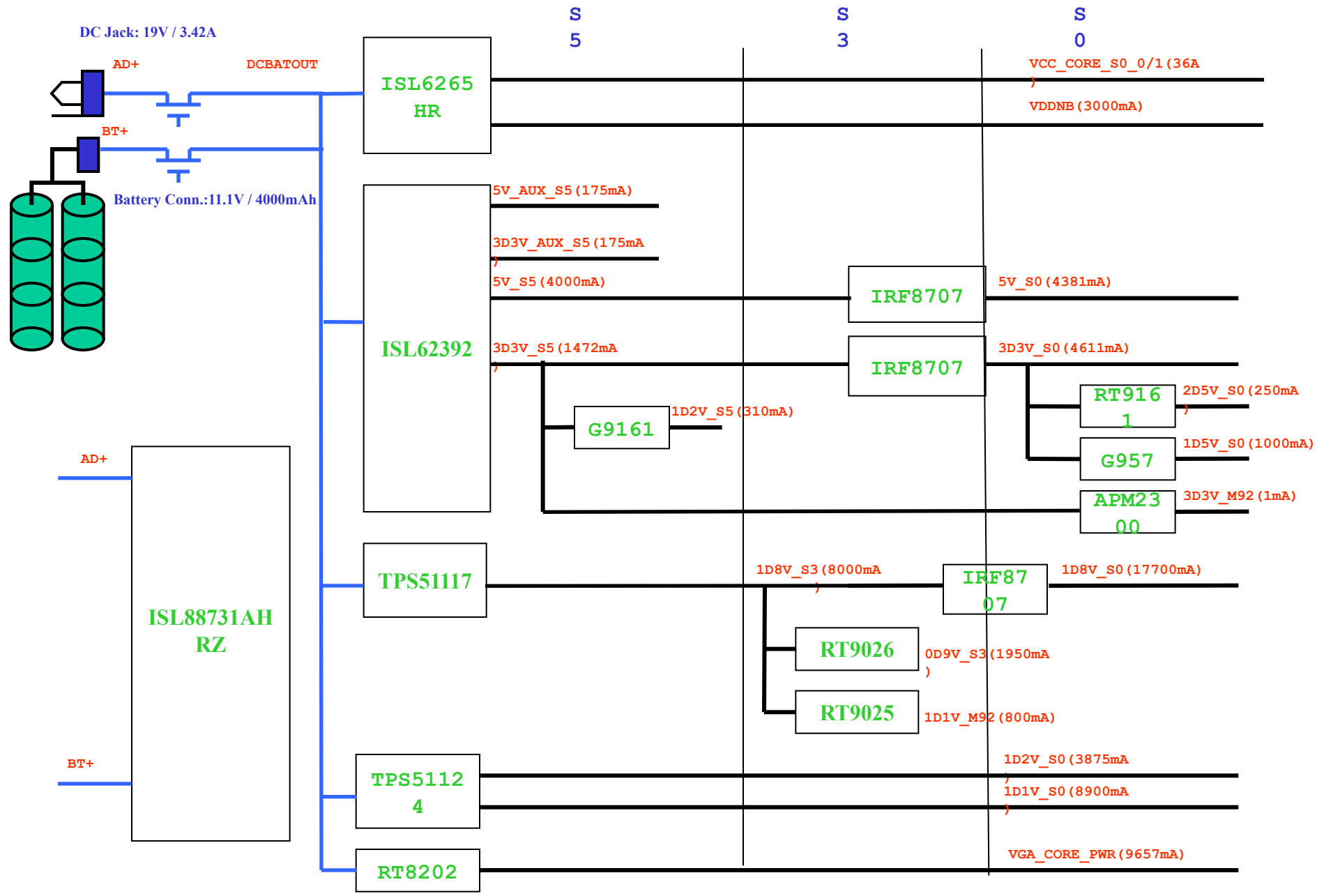
JV50-PU Power ON/RESET Sequence



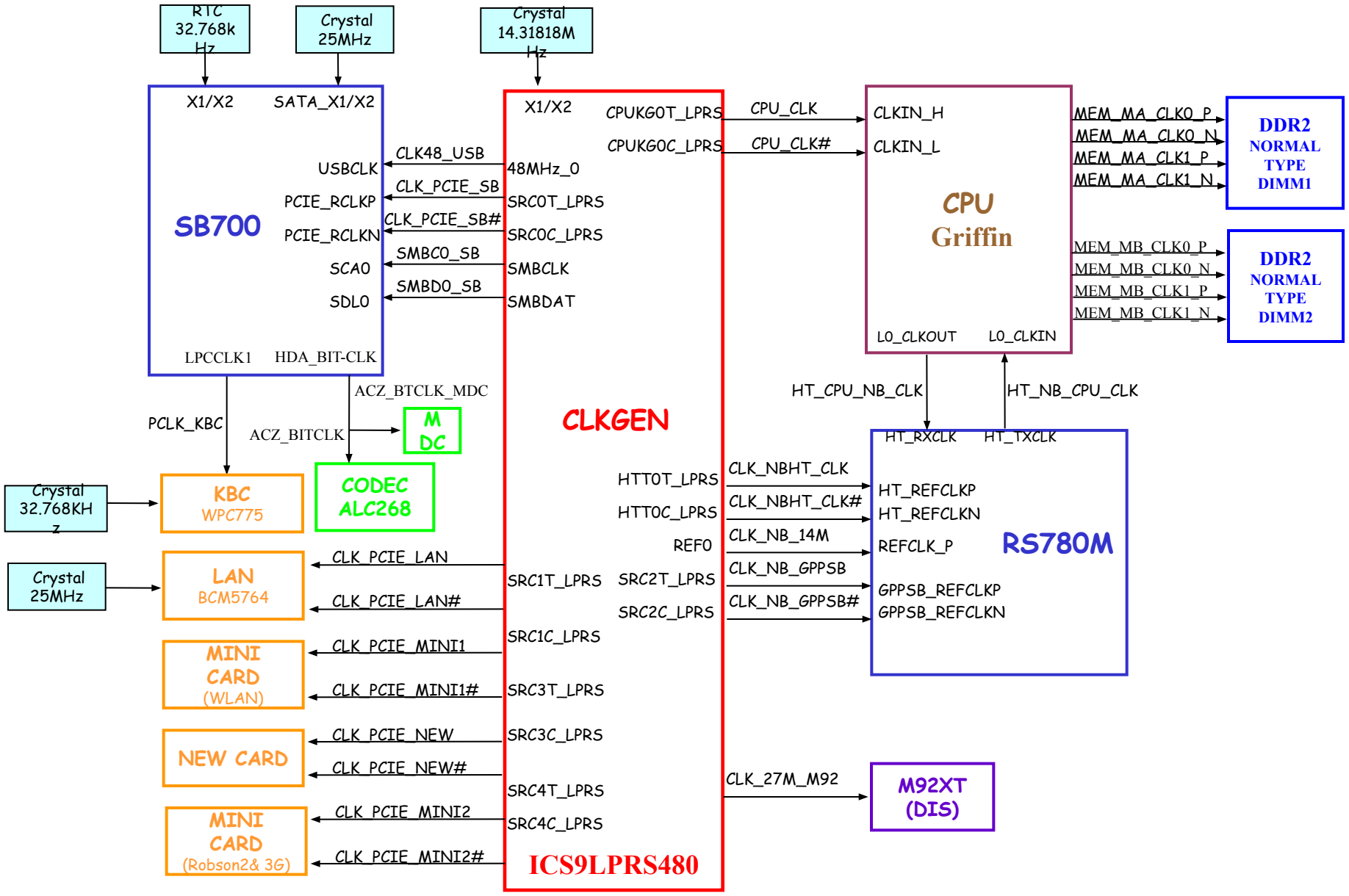
JV50-PU Power Budget



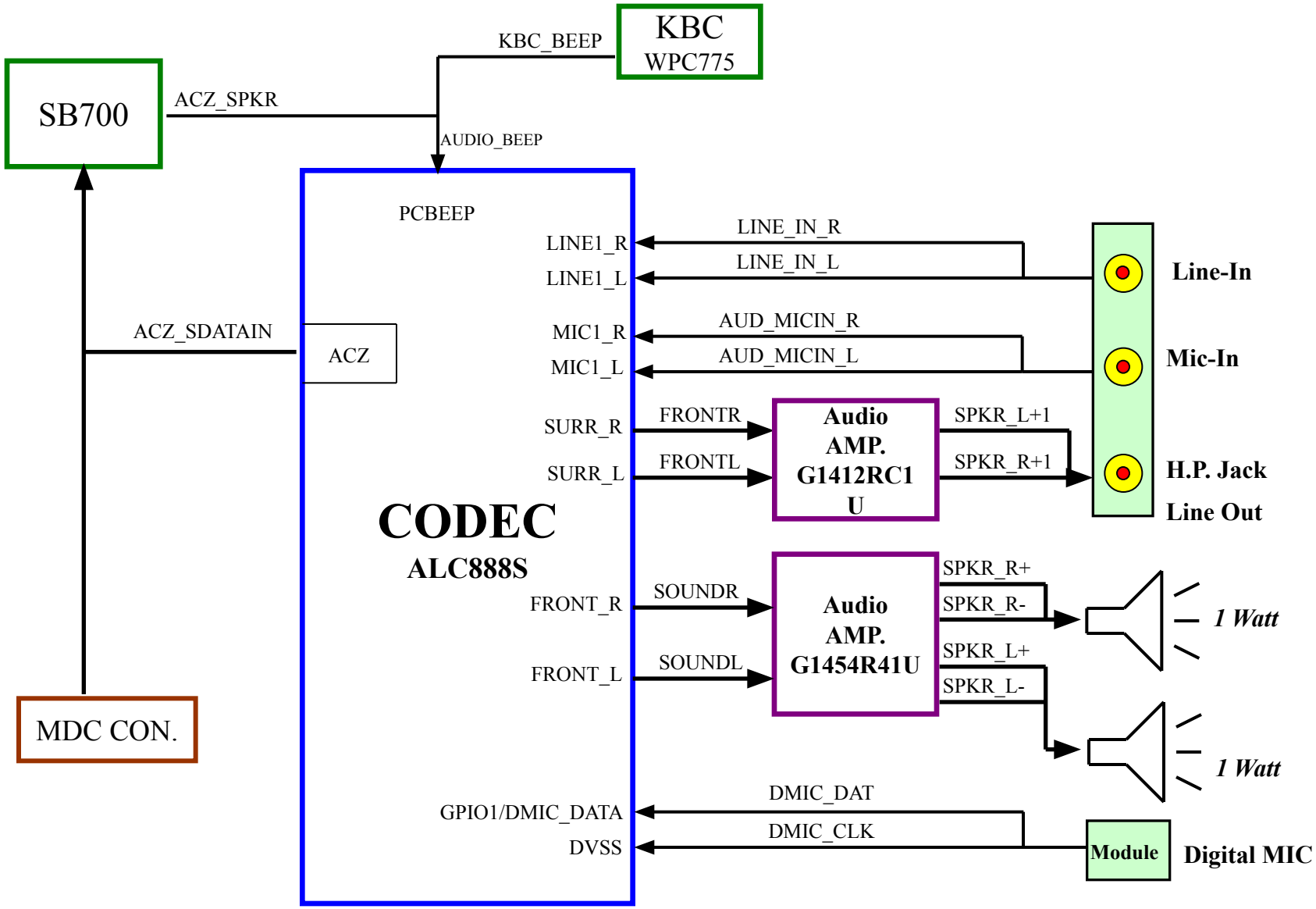
JV50-PU POWER BLOCK DIAGRAM



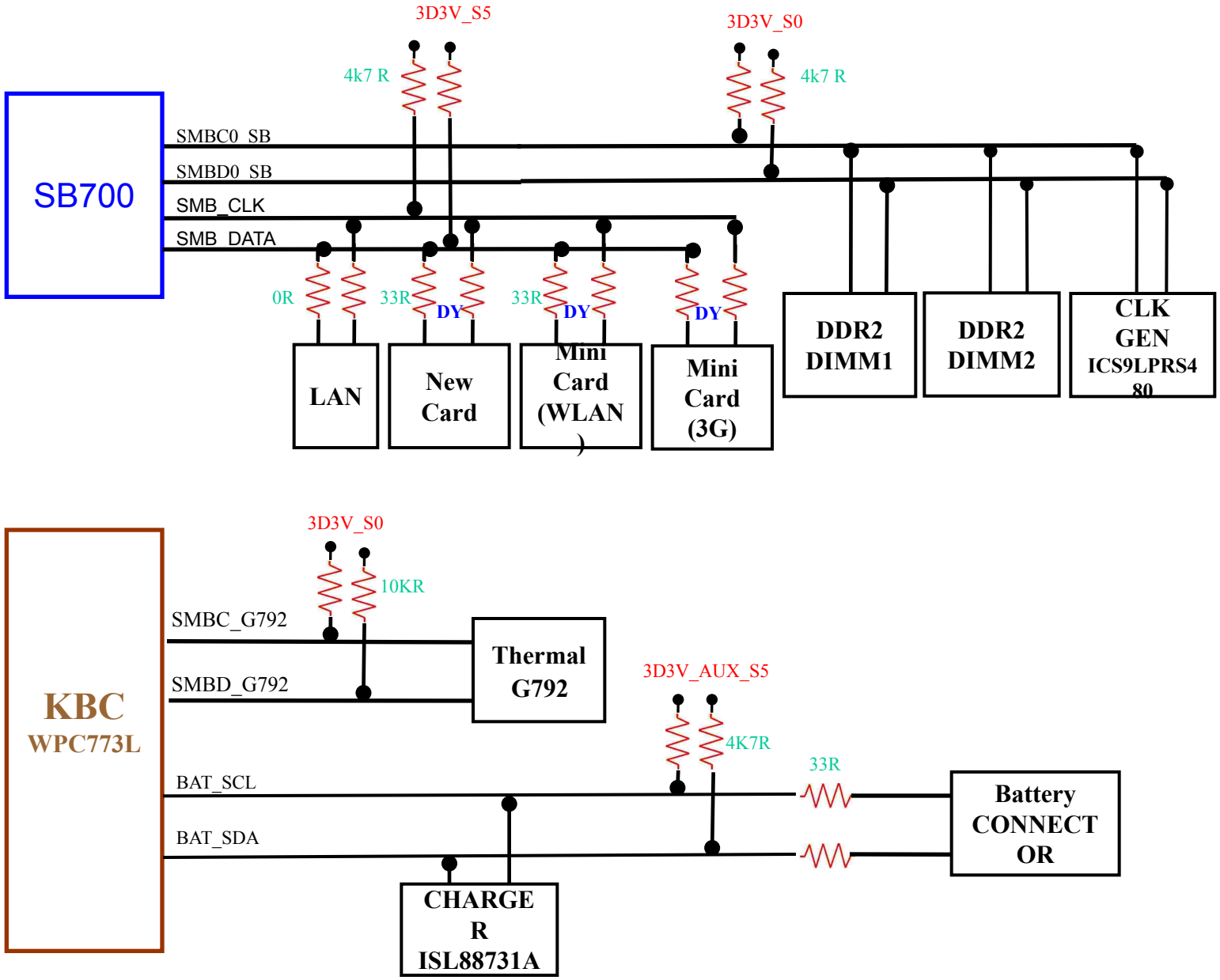
JV50-PU Clock Block Diagram



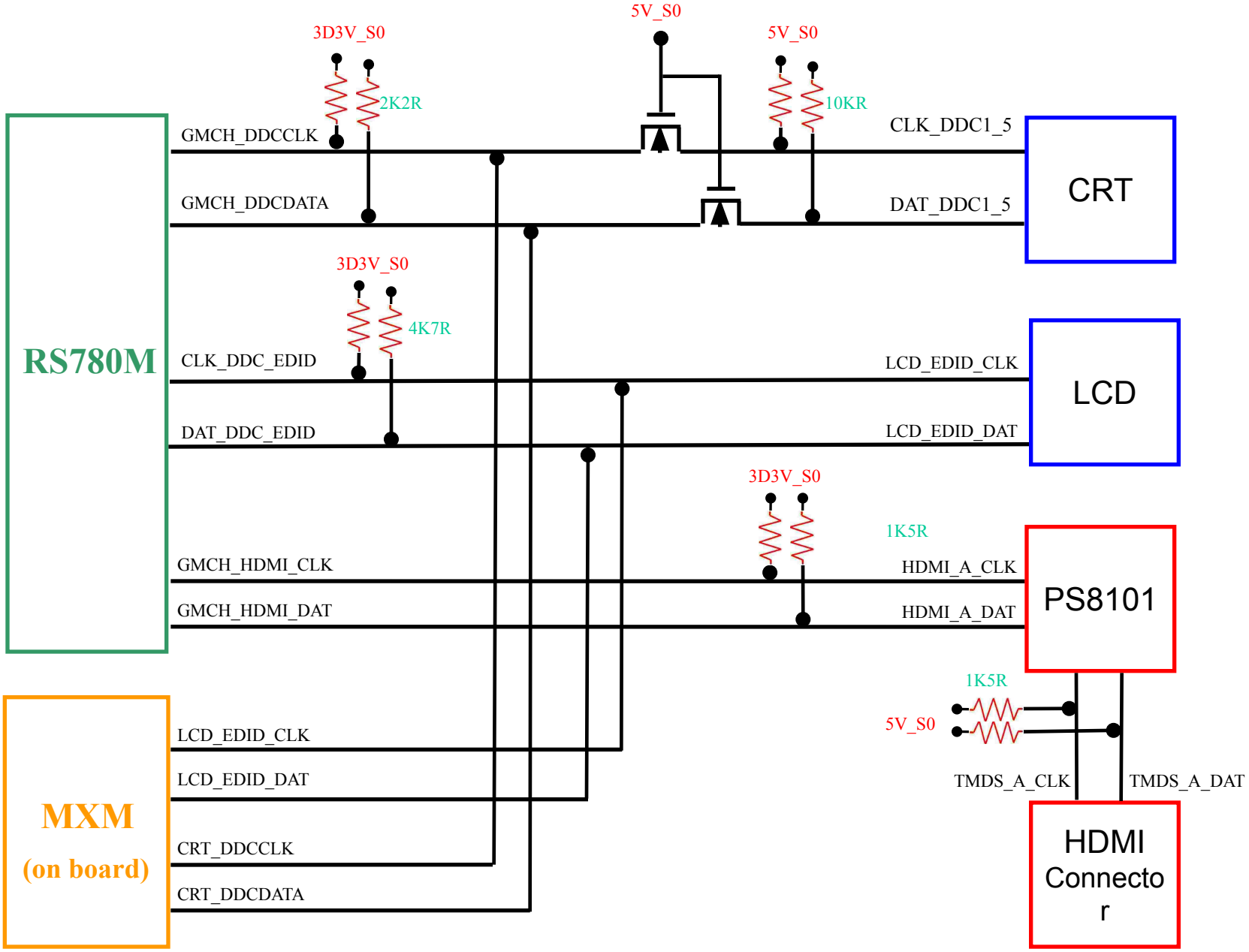
JV50-PU Audio Block Diagram



JV50-PU SMB Interface-1



JV50-PU SMB Interface-2

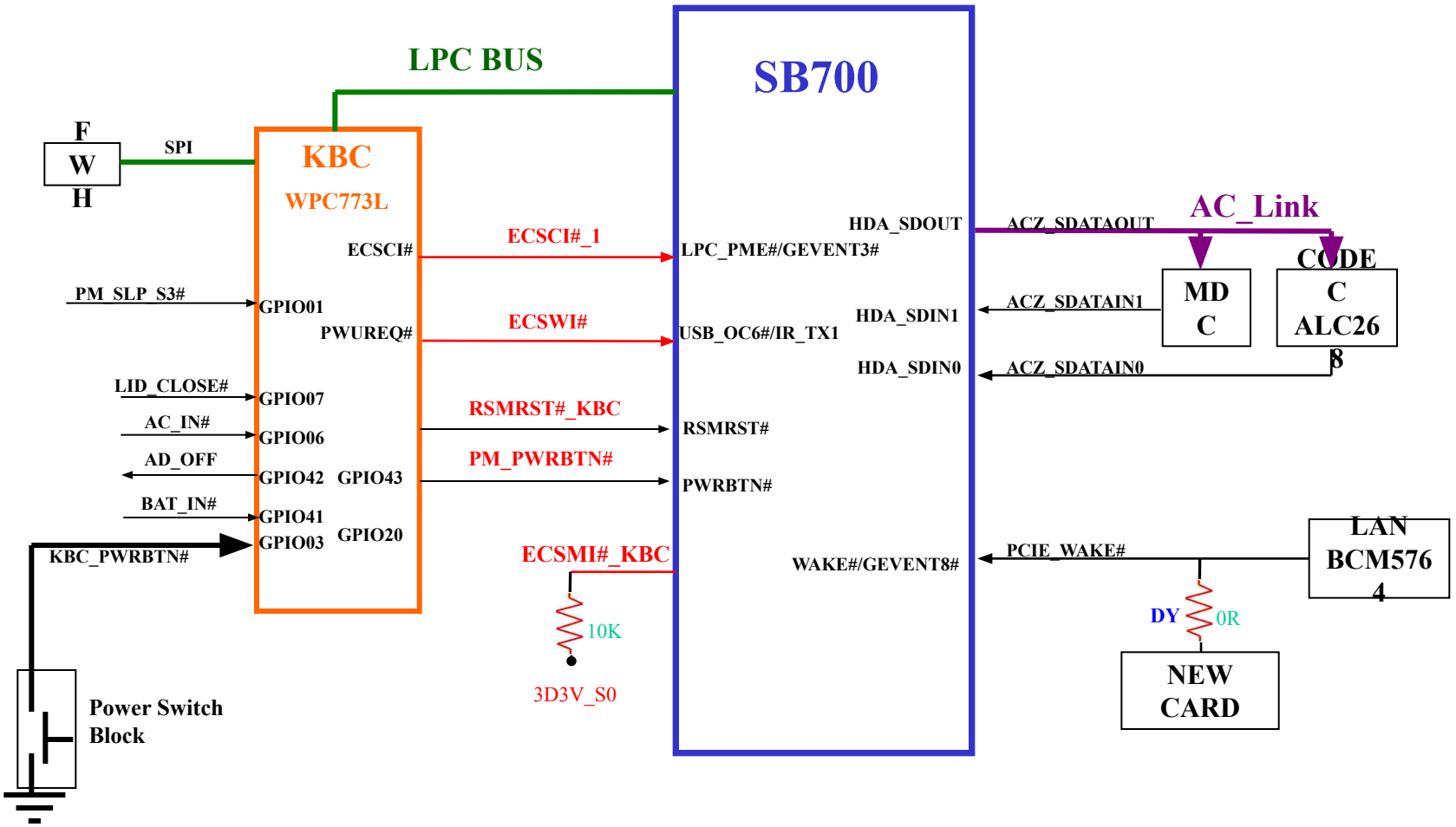


SMI在DOS底下動作

SCI在windows底下動作

SWI是指wake up event

JV50-PU SMI/SCI/SWI Interface



From S3 state wakeup event: (1) Power Button; (2) WOL (AC Only); (3) Embedded Modem (AC Only) ;(4) RTC; (5) Lid; (6) Battery Critical

JV50-PU VCC_CORE Block Diagram