2012 EU ALSA Training
P9X79 SERIES

GRMA Brain_HUNG

P9X79 – Agenda

- Intel X79 Platform Structure
- P9X79 Series Architecture
- New Feature
- Difference With P8 Series
- Clock Distribution
- Power Flow & Critical Power on X79 Platform
- Power Sequence
- Embedded Controller Introducing
- SIO and Other Power Chipset Introducing
- Communication BUS Introducing

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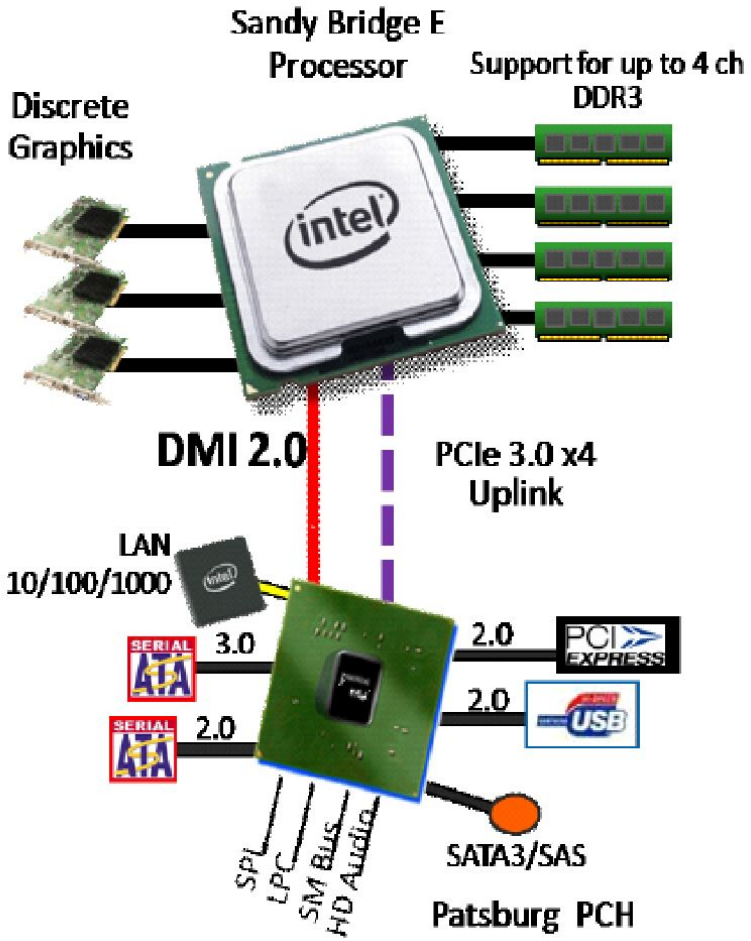
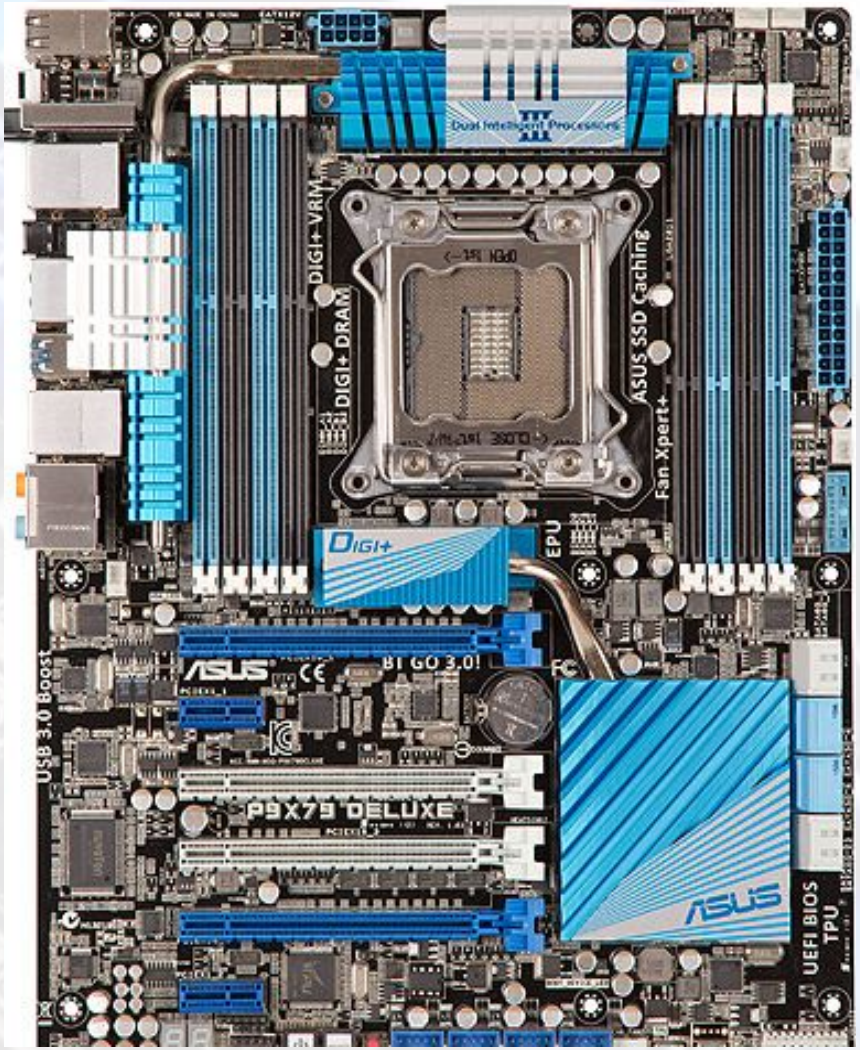
Intel X79 Platform Structure



- CPU 6C/12T, 4C/8T
- Support PCIe 3.0
- DRAM support up to 4ch, 8xDIMM, Max. 64GB
- Supports NVIDIA® 3-Way SLI™ Technology
  Supports AMD Quad-GPU CrossFireX™ Technology
- SATA 6G *2, SATA 3G *4
- USB 2.0 *14
- Remove SAS port

Intel X79 Platform Structure

- Support 8GB,MAX is for 64GB
- Support DDR3 2400(O.C.)/2133(O.C.) 1866/1600/1333/1066
- Support Intel® Extreme Memory Profile(XMP)
- Support DIGI+ Power Control
- 2 + 2 Phase Control



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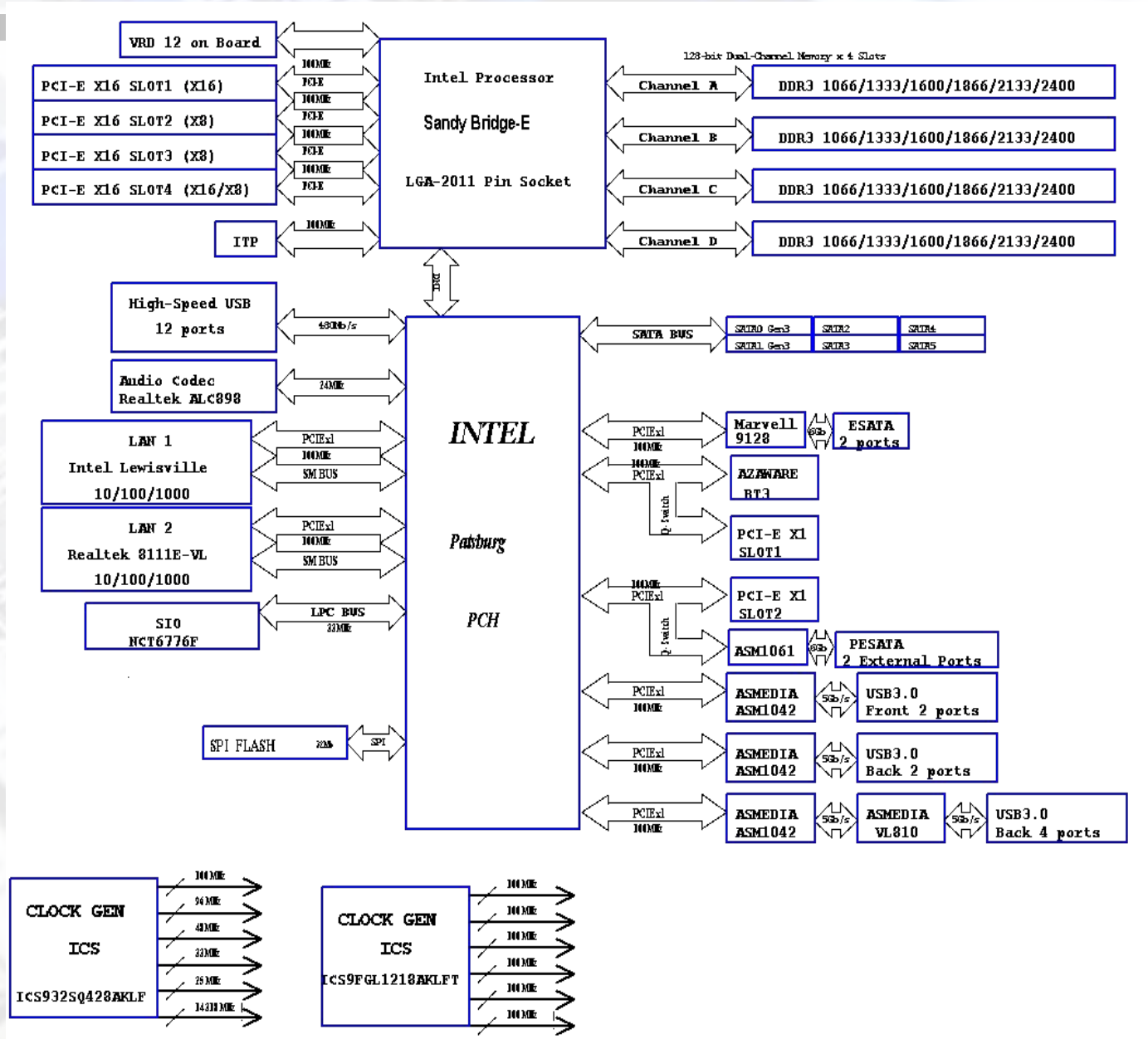
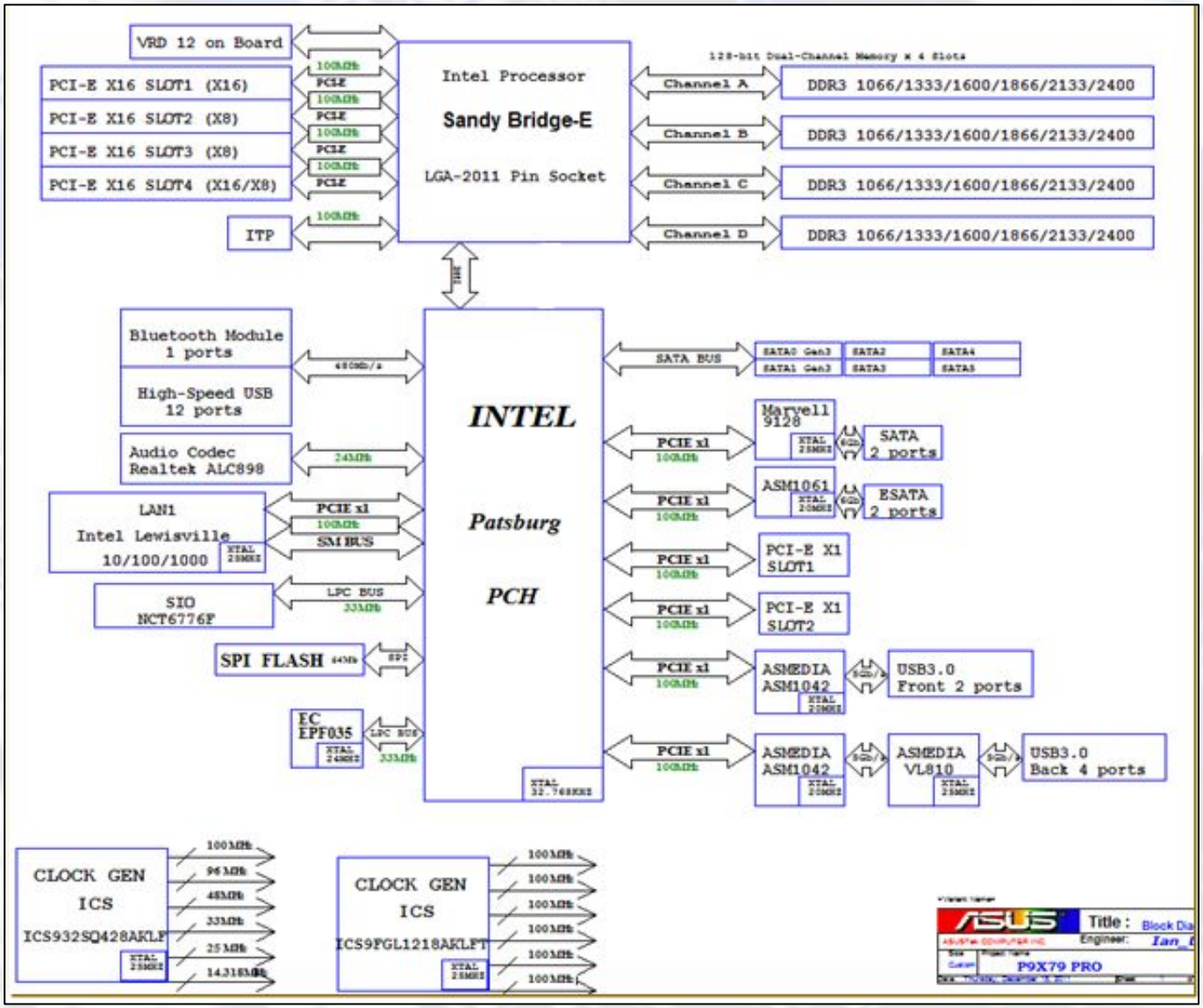
P9X79 Deluxe - Architecture



P9X79 PRO - Architecture



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New Feature – DIGI+ Power Control

Digital Power : CPU + DRAM

Intelligent Digital Power Controller (CPU)

Intelligent Digital Power Controller (DRAM)

- Most Precise Adjustment on CPU & DRAM
- Extreme Performance & O.C. Capability for CPU & DRAM
- High System Stability

New Feature – USB BIOS Flashback

Smart chip control without boot-up

No need to open chassis

Complete within only ONE click

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P9X79 Deluxe – Compare with P8 Series

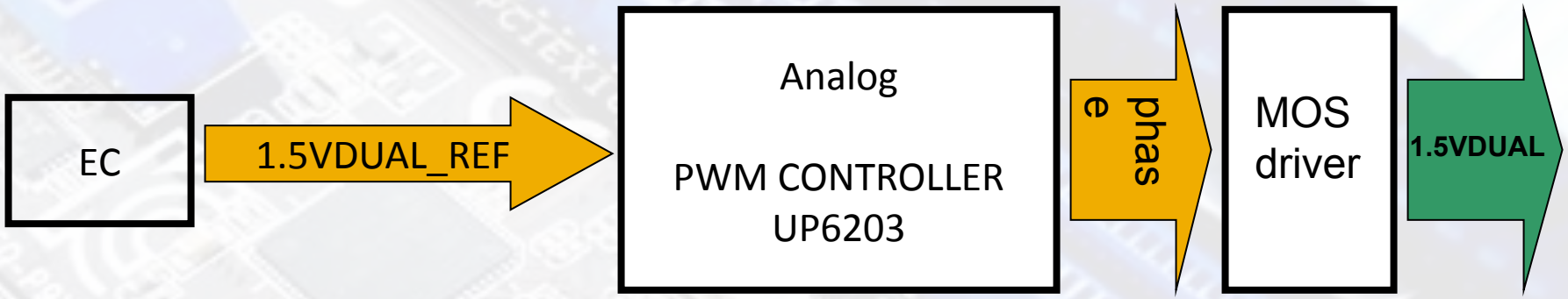
- DRAM power control: Analog □ DIGITAL
- Clock Generator: PCH Internal □ External
- E-SATA support 6G □ Asmedia1061

Architecture	Raw Bit Rate	Interconnect Bandwidth	Bandwidth per Lane per Direction	Total Bandwidth for x16 Link
PCIe 1.x	2.5 GTps	2 Gbps	~250 MBps	~8 GBps
PCIe 2.x	5 GTps	4 Gbps	~500 MBps	16 GBps
PCIe 3.0	8 GTps	8 Gbps	~1 GBps	~32 GBps

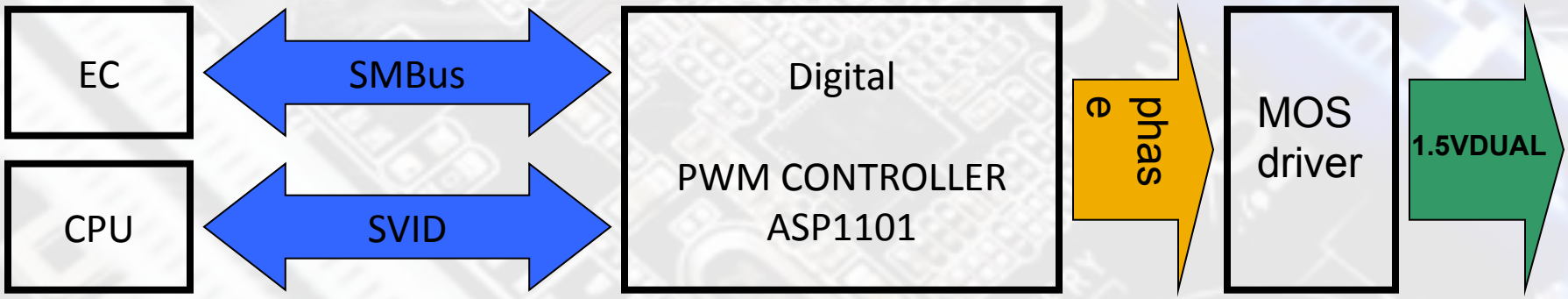
- X79 is native support PCIe 3.0
- BIOS can park setting on gen2 or gen3 for compatibility.

P8 & P9 series DRAM power control

P8 series DRAM power control



P9 series DRAM power control



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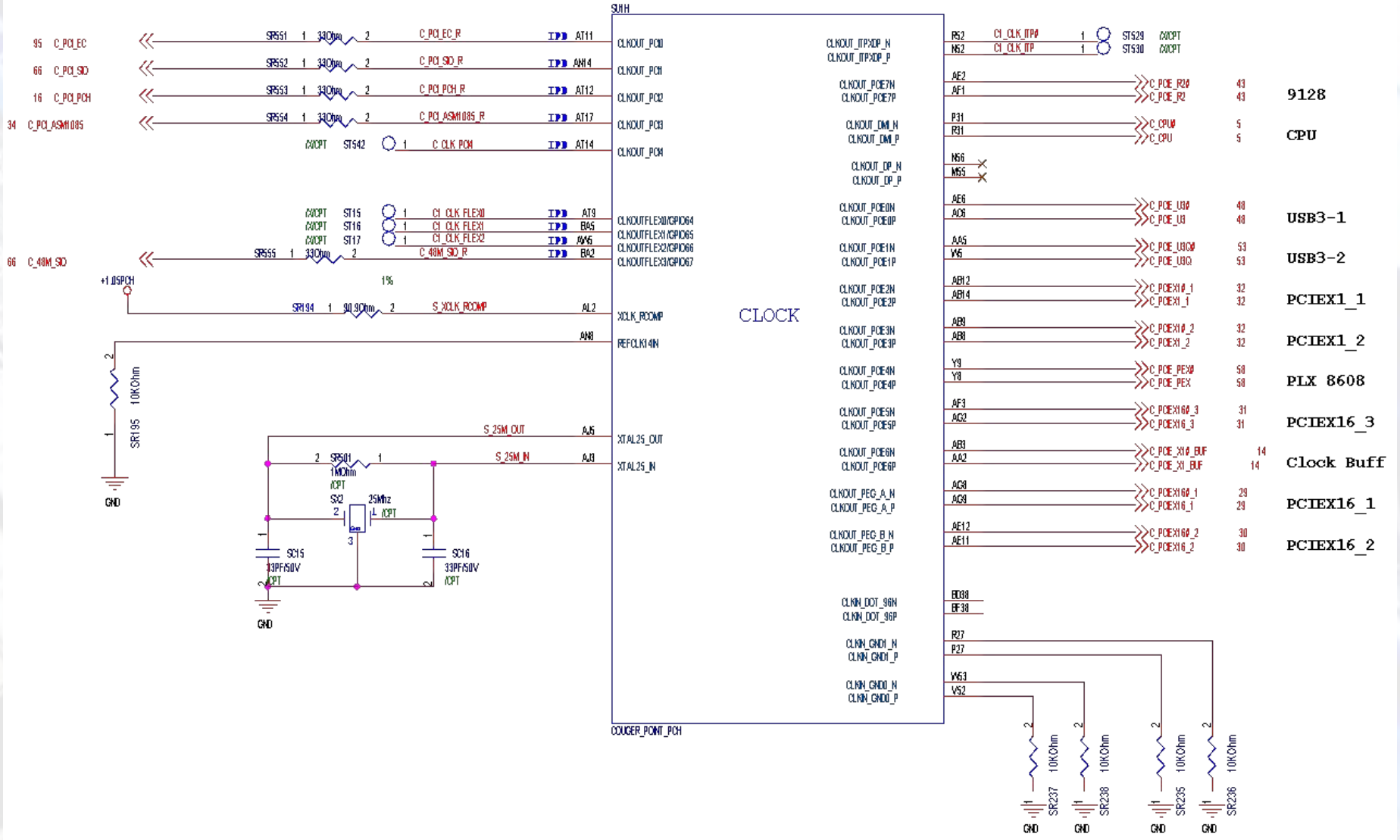
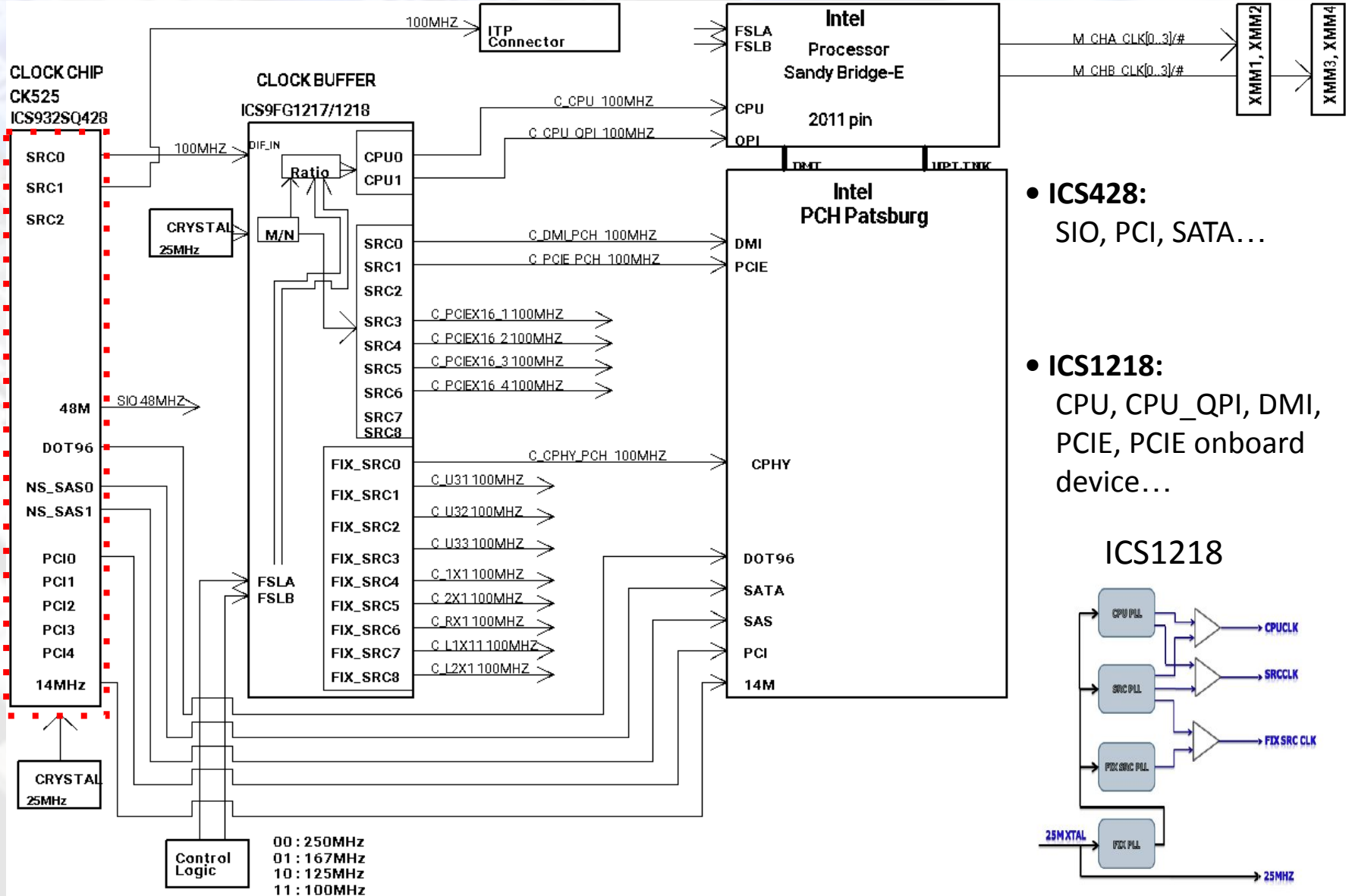
P8 Series - Clock Distribution



P9X79 Deluxe - Clock Distribution

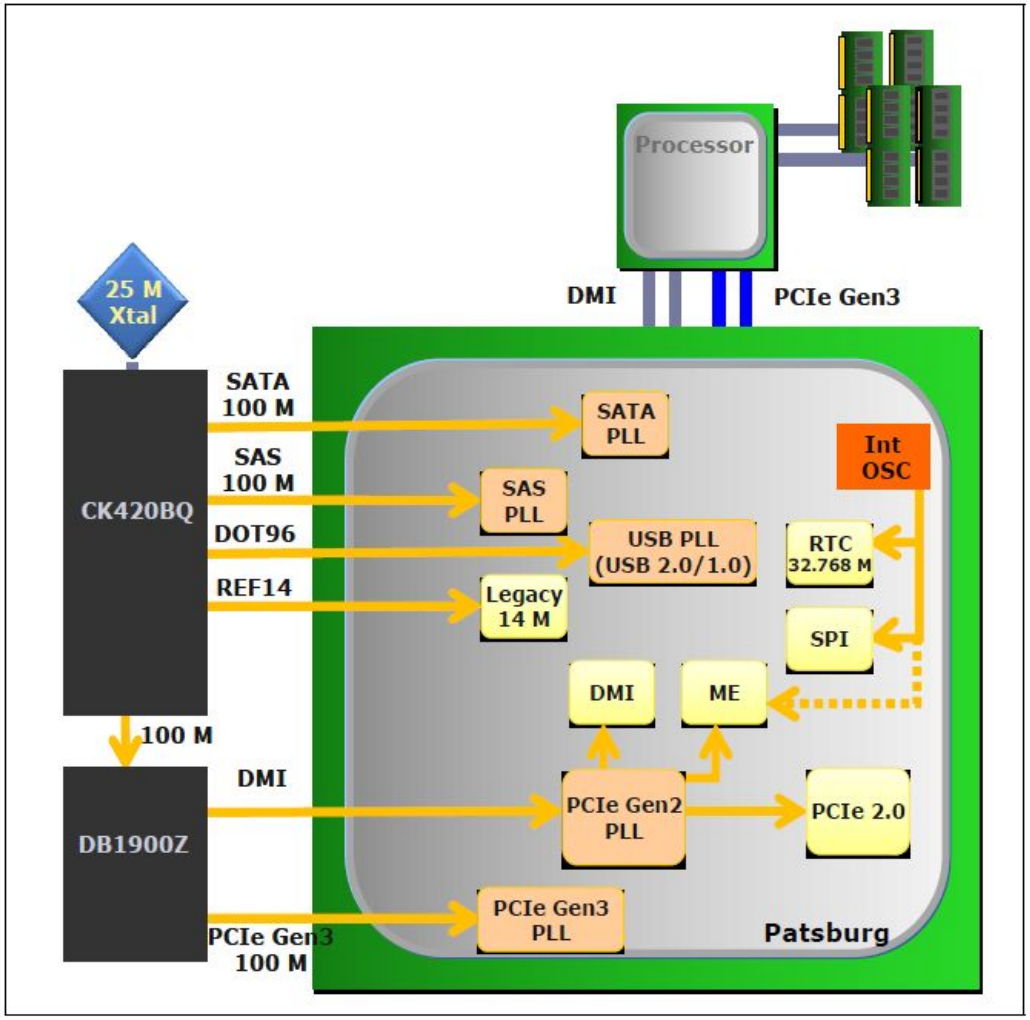


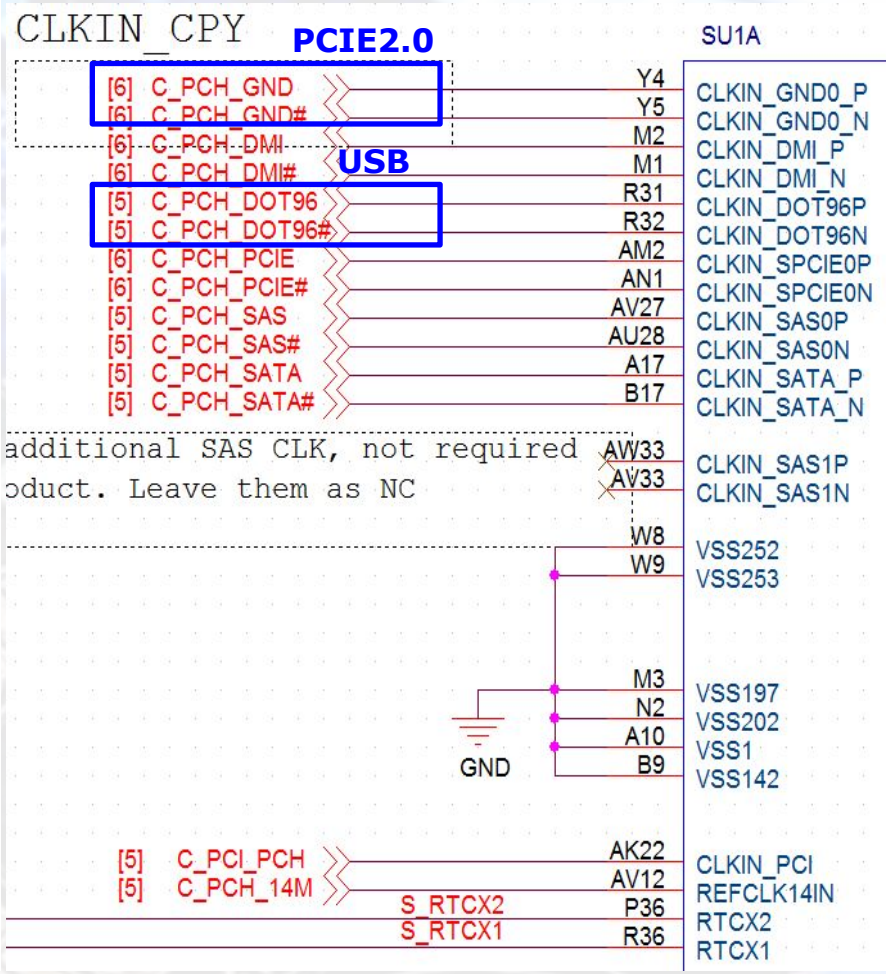
- **ICS428:**
  SIO, PCI, SATA…

- **ICS1218:**
  CPU, CPU_QPI, DMI, PCIE, PCIE onboard device…

ICS1218

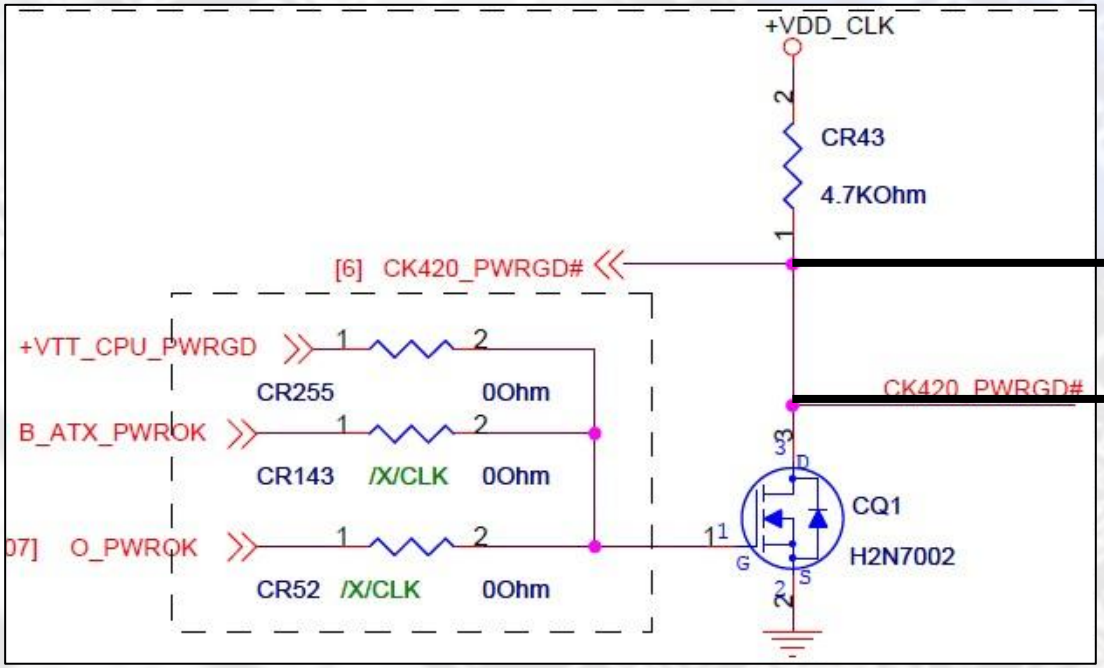
Patsburg Chipset High-Level Clock Diagram

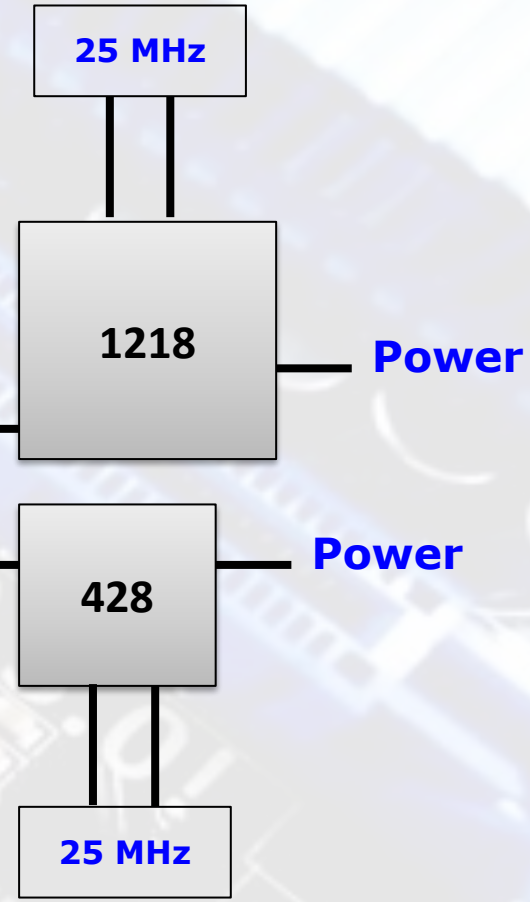




P9X79 Deluxe – Clock Generator

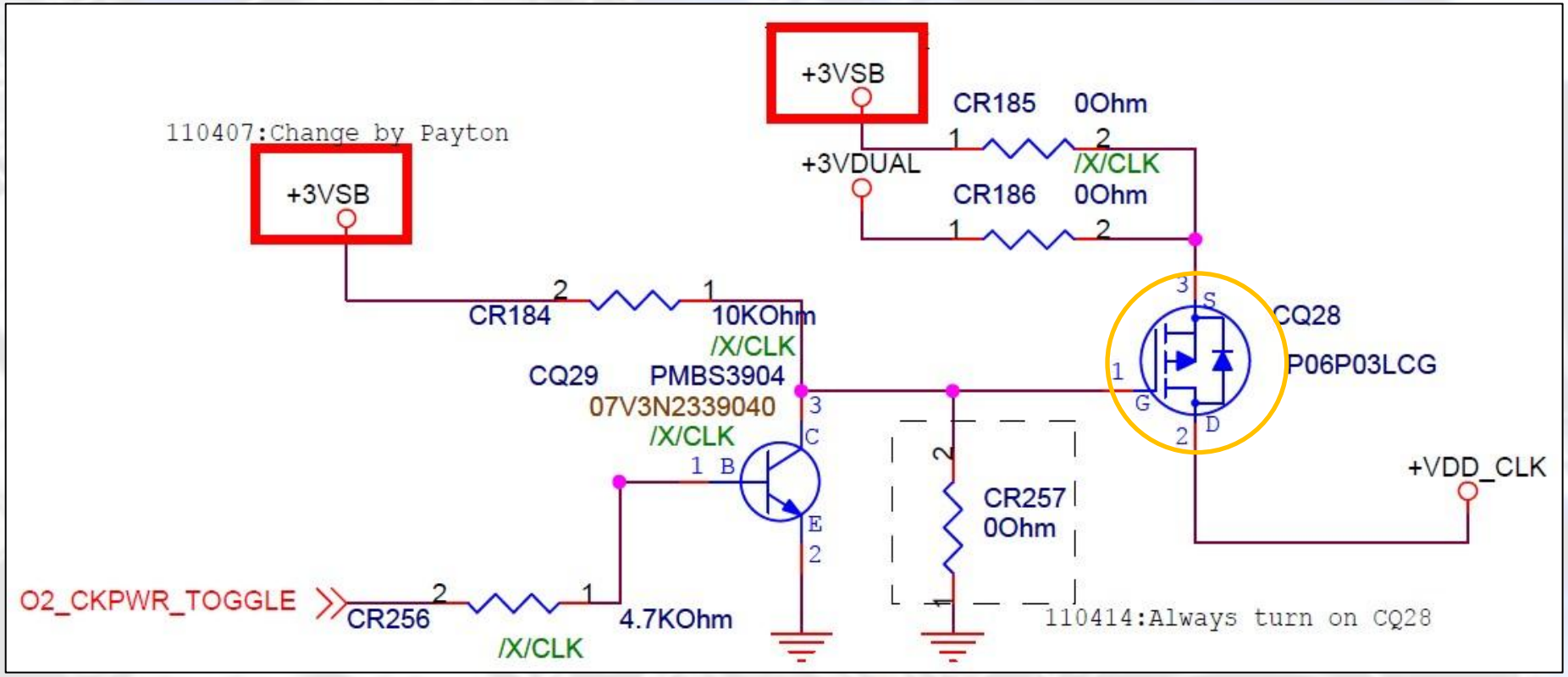
+VTT_CPU_PWRGD → CK420_PWRGD#





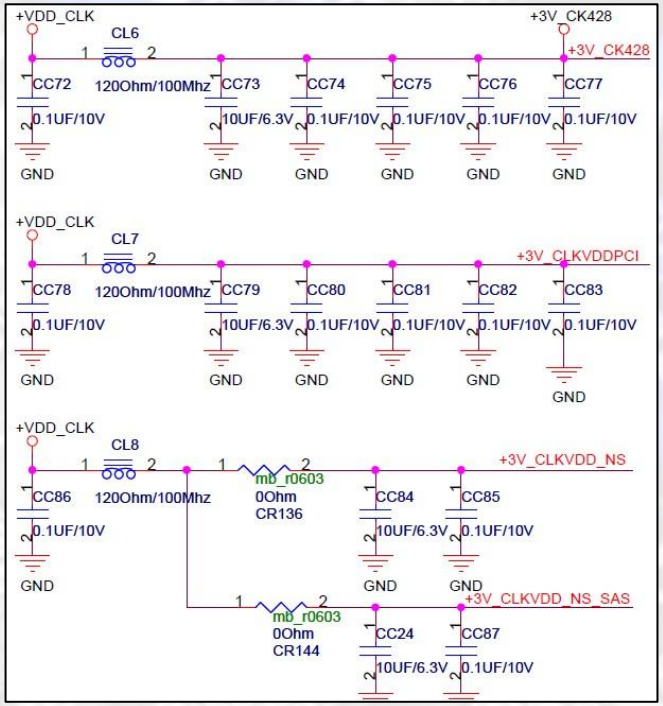
Power for Clock Generator

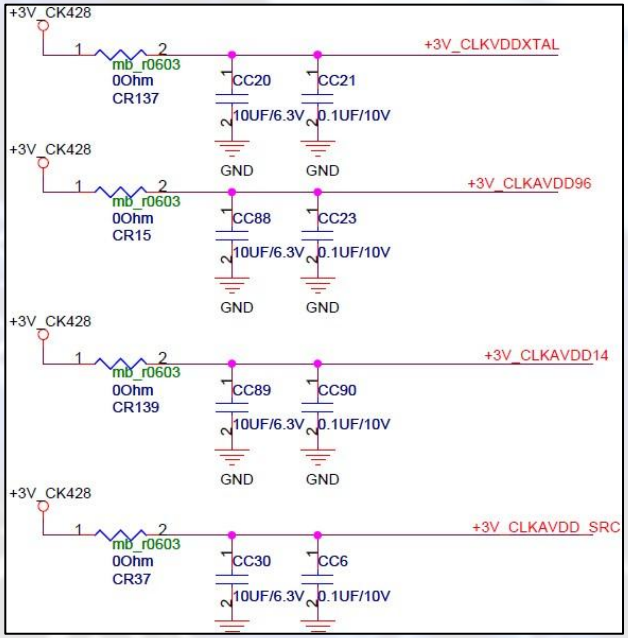
+3VDUAL → +VDD_CLK



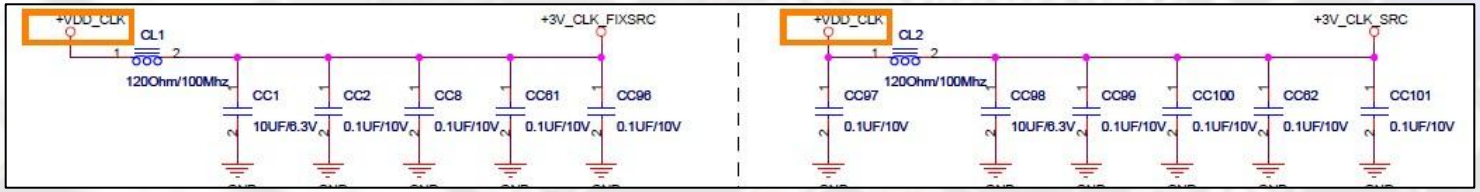
Power Distribution for CLK GEN

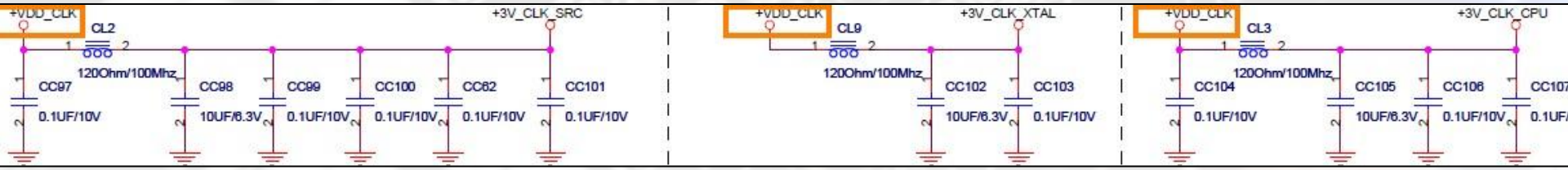
428 CLK GEN



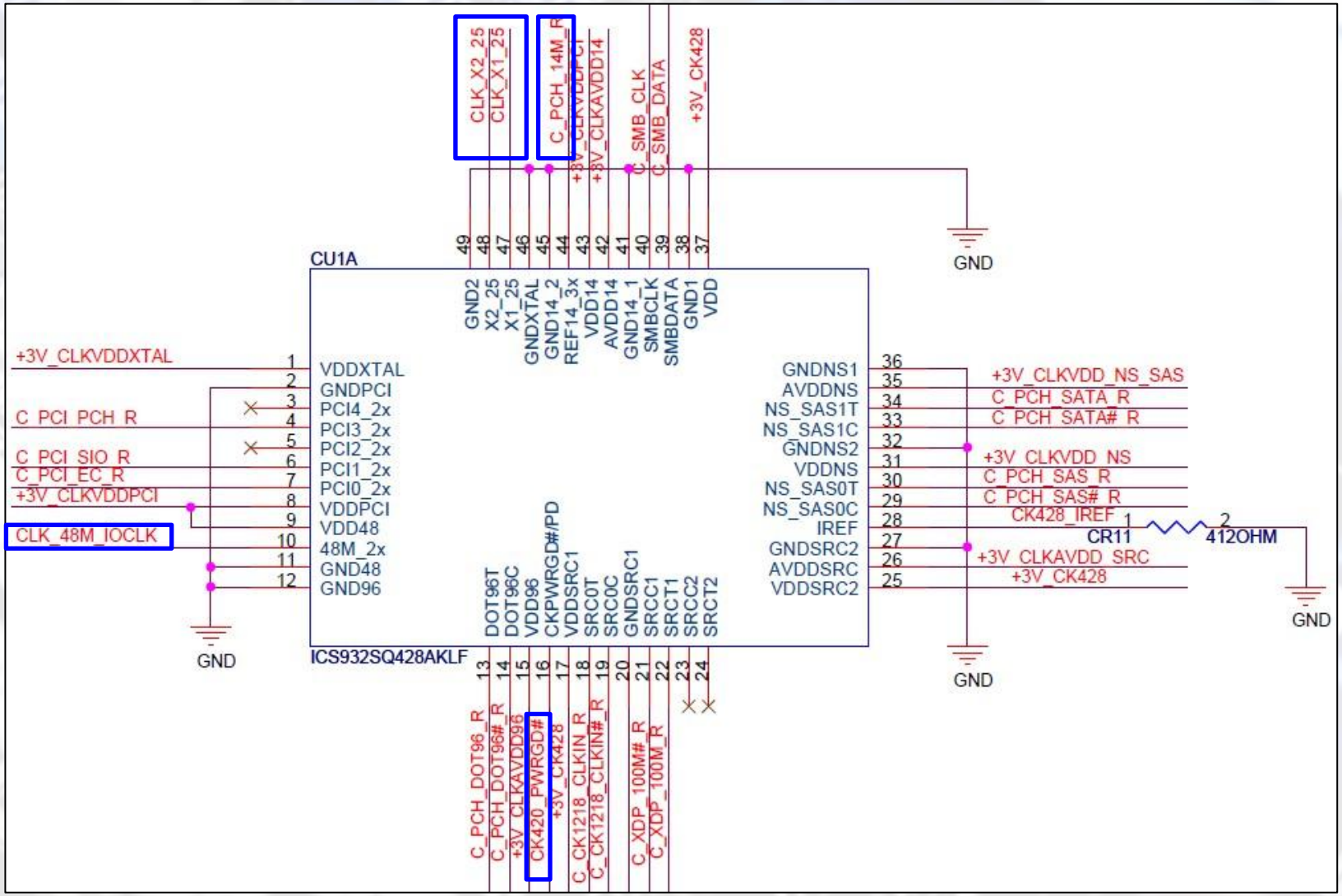


1218 CLK GEN

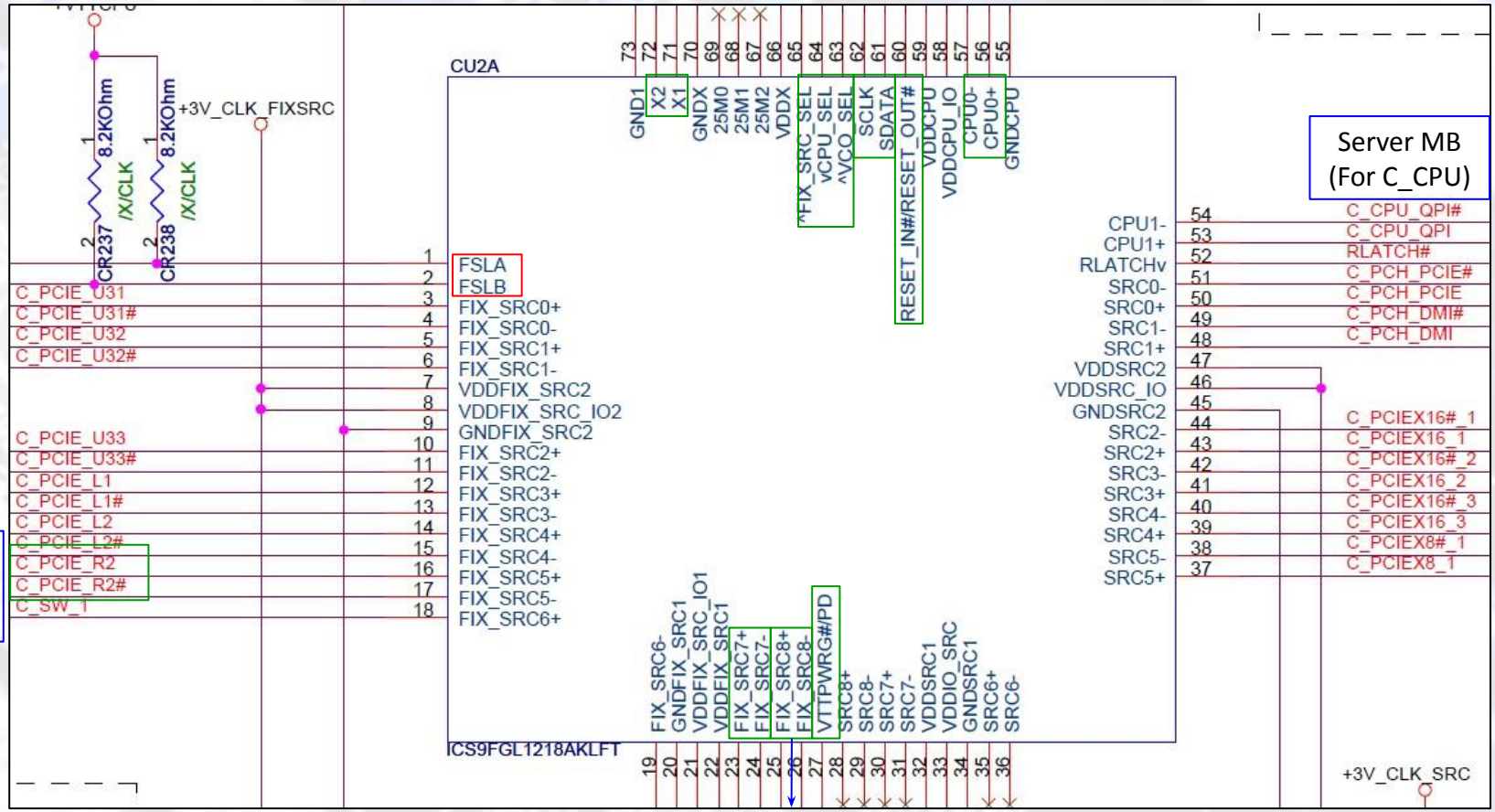




Clock Generator of ICS394SQ428



Clock Generator of ICS9FG1218



Server MB
(For C_CPU)

SAS

Marvall
9128
(SATA)

C_PCH_GND
(ex: E-SATA)

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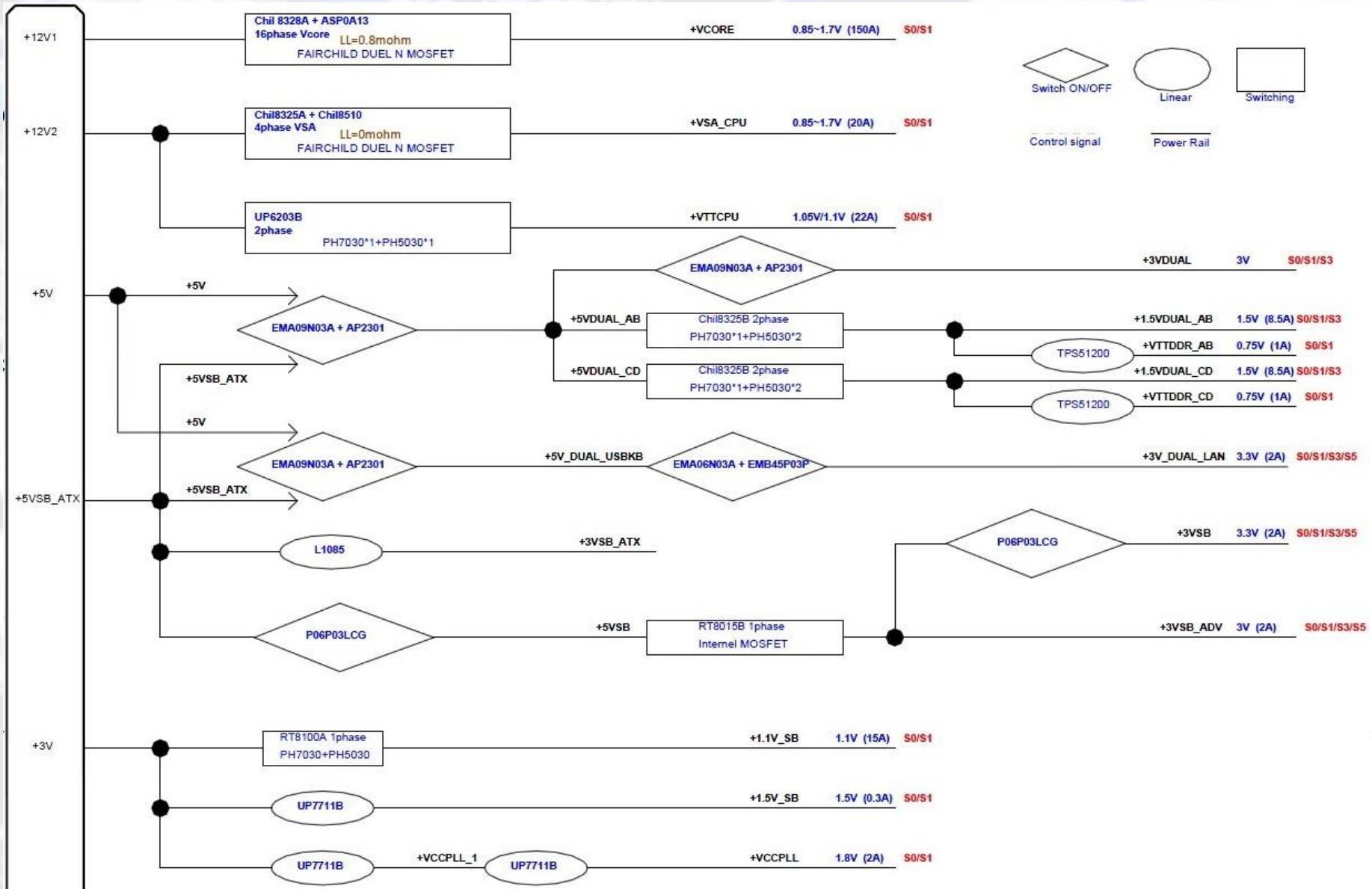
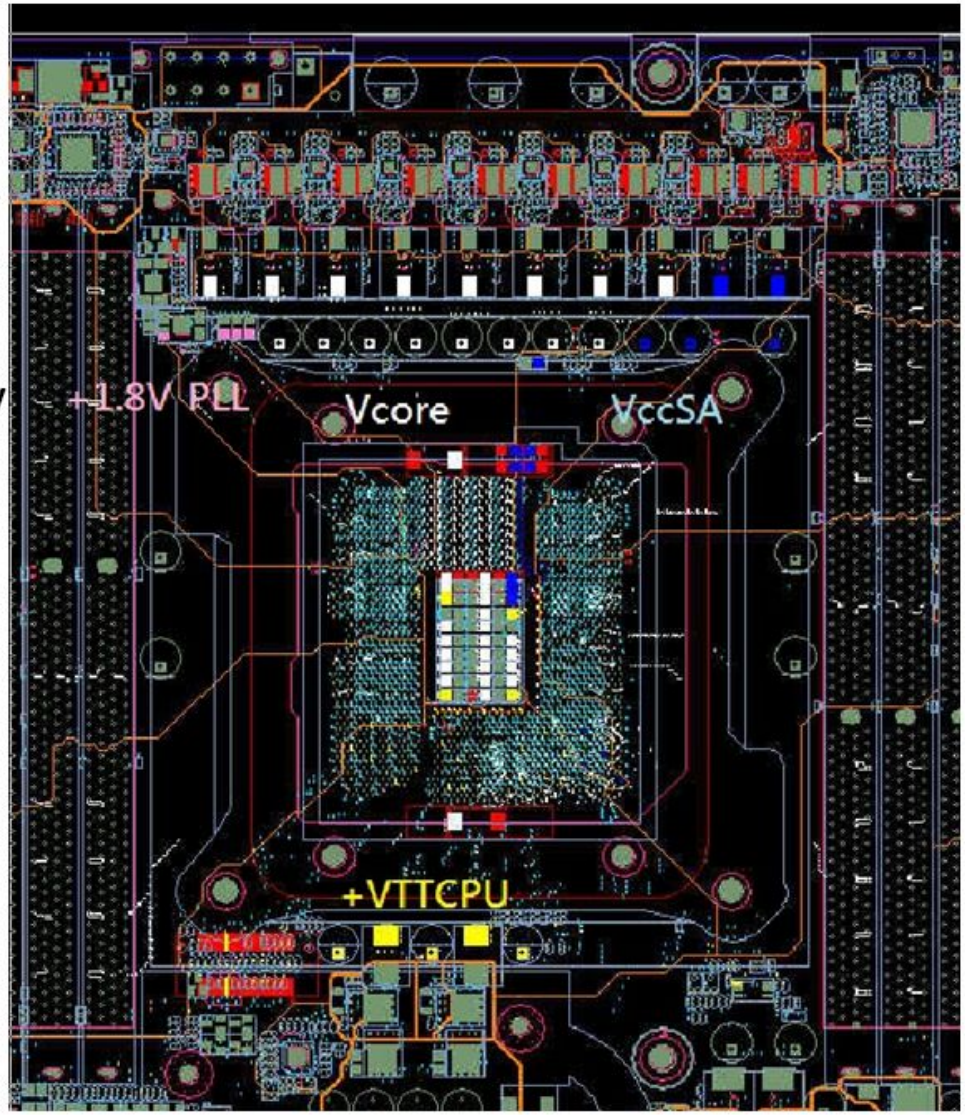
P9X79 Deluxe – Power Flow



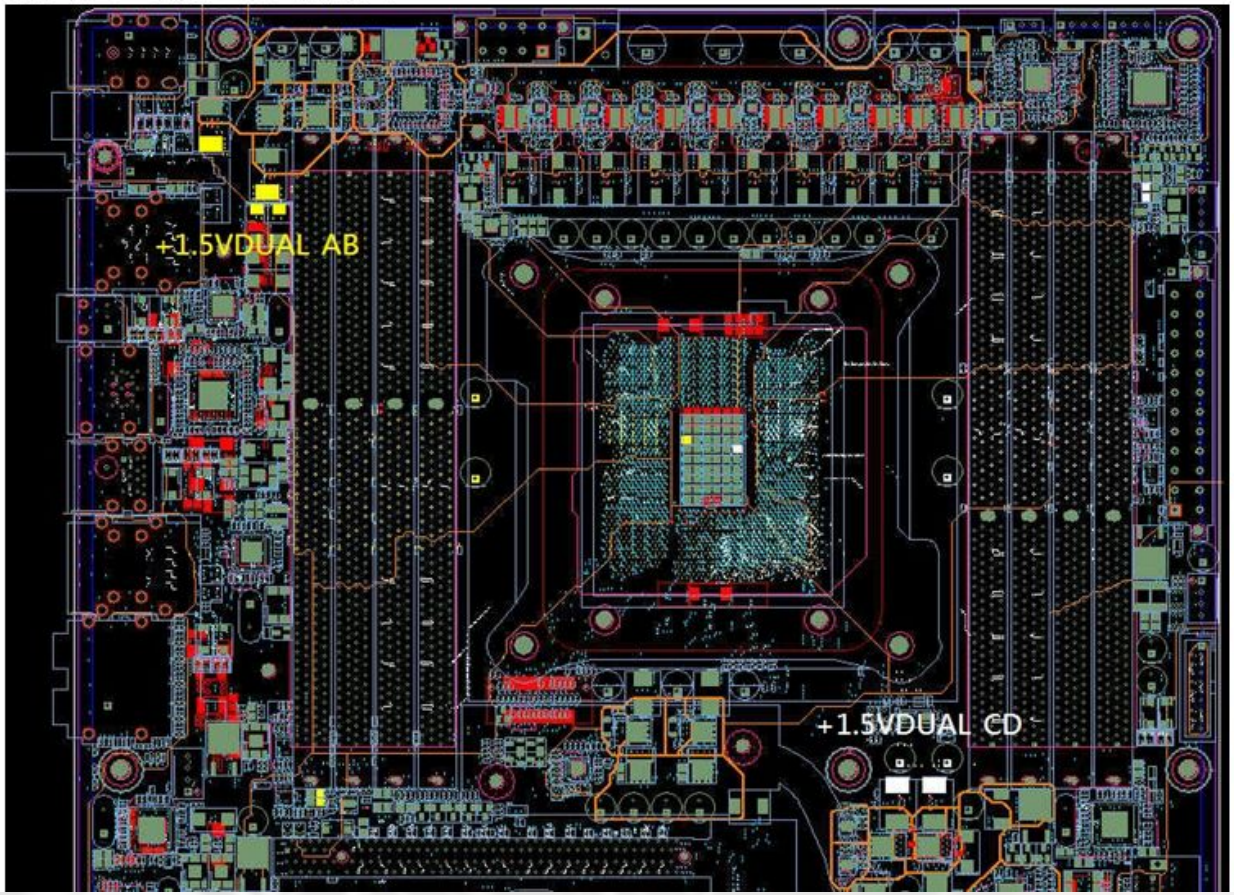
P9X79 Deluxe – CPU Voltage

- CPU
  - Vcore : 1.0~1.2V
  - VccSA : 1.0~1.2V
  - +1.8VPLL : 1.8V
  - +VTTCPU : 1.05V
  - +1.5VDUAL_AB
  - +1.5VDUAL_CD



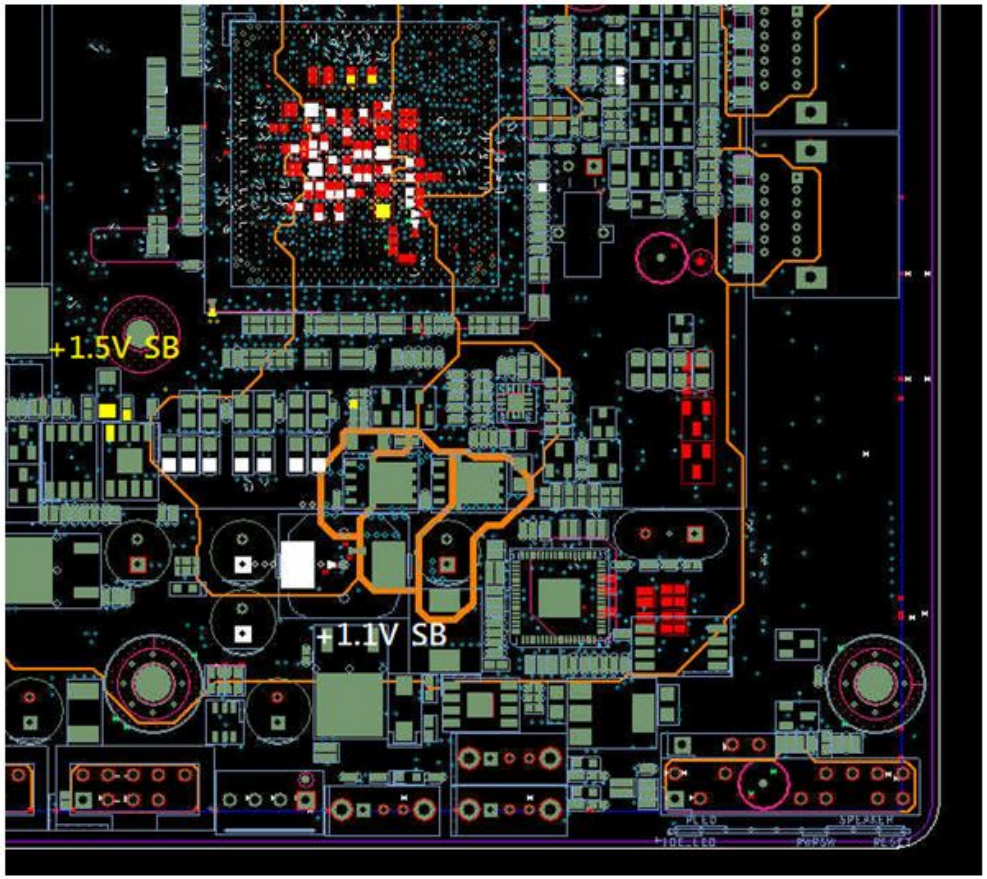
P9X79 Deluxe – DRAM Voltage

- DRAM
  - +1.5VDUAL_AB : 1.5V
  - +1.5VDUAL_CD : 1.5V



P9X79 Deluxe – PCH Voltage

- PCH
  - +1.1V_SB : +1.1V
  - +1.5V_SB : +1.5V



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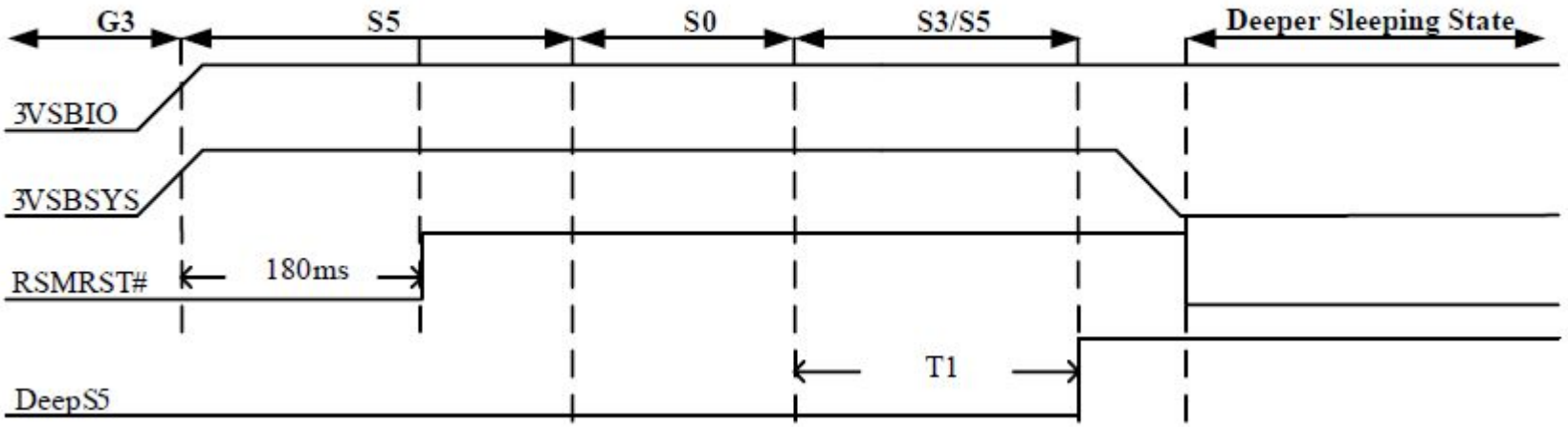
P9X79 Power Status - ACPI

G3: Battery S0: All Power S3: Standby and Dual Deep S5: Only ATX Power

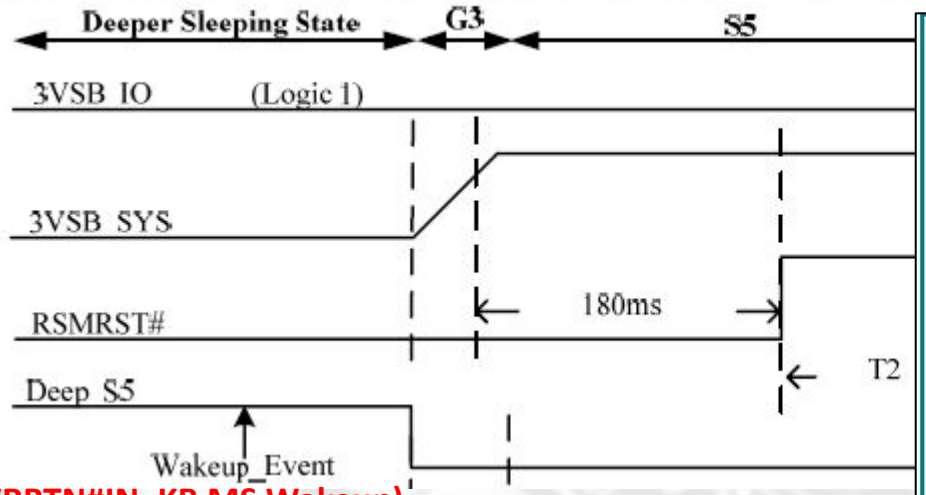
Mode Description		Battery Power	Standby_ATX Power	Standby Power	Dual Power	Main Power	
G3	Time	V					
S0	Working Status	V	V	V	V	V	Working Status
S1	CPU Suspend	V	V	V	V	V	Power on Suspend
S2		V	…	…	…	…	
S3	Suspend to RAM	V	V	V	V		Suspend to RAM
S4	Suspend to Disk	V	V	V	…		Suspend to Disk
S5	Soft Off	V	V	V	…		SoftOff
Deep S5	Deep Soft Off (EuP)	V	V	…	…		Deep Soft Off (EuP)
Power		3V_BAT	5VSB_ATX, 3VSB_ATX	5VSB, 3VSB,	1.5V_DUAL, 3V_DUAL	12V, 5V, 3V, VCORE	

P9X79 Power – Deep S5 State

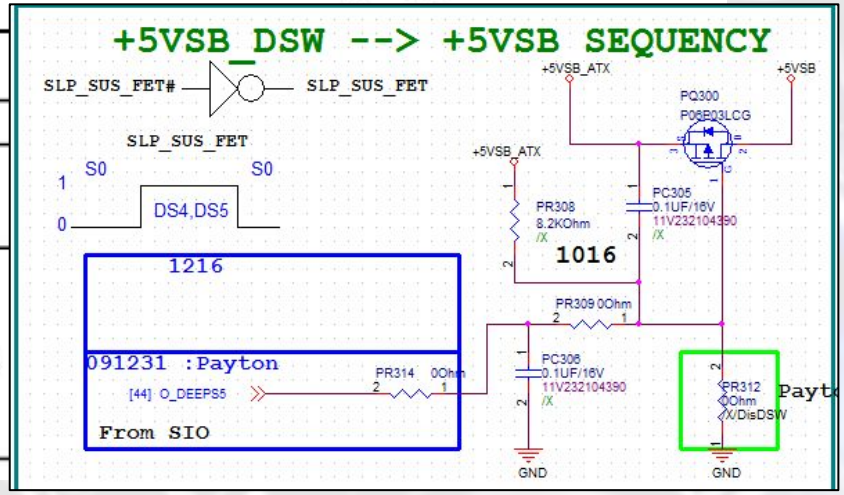
When ASSC is enabled (Enter into Deeper Sleeping State)



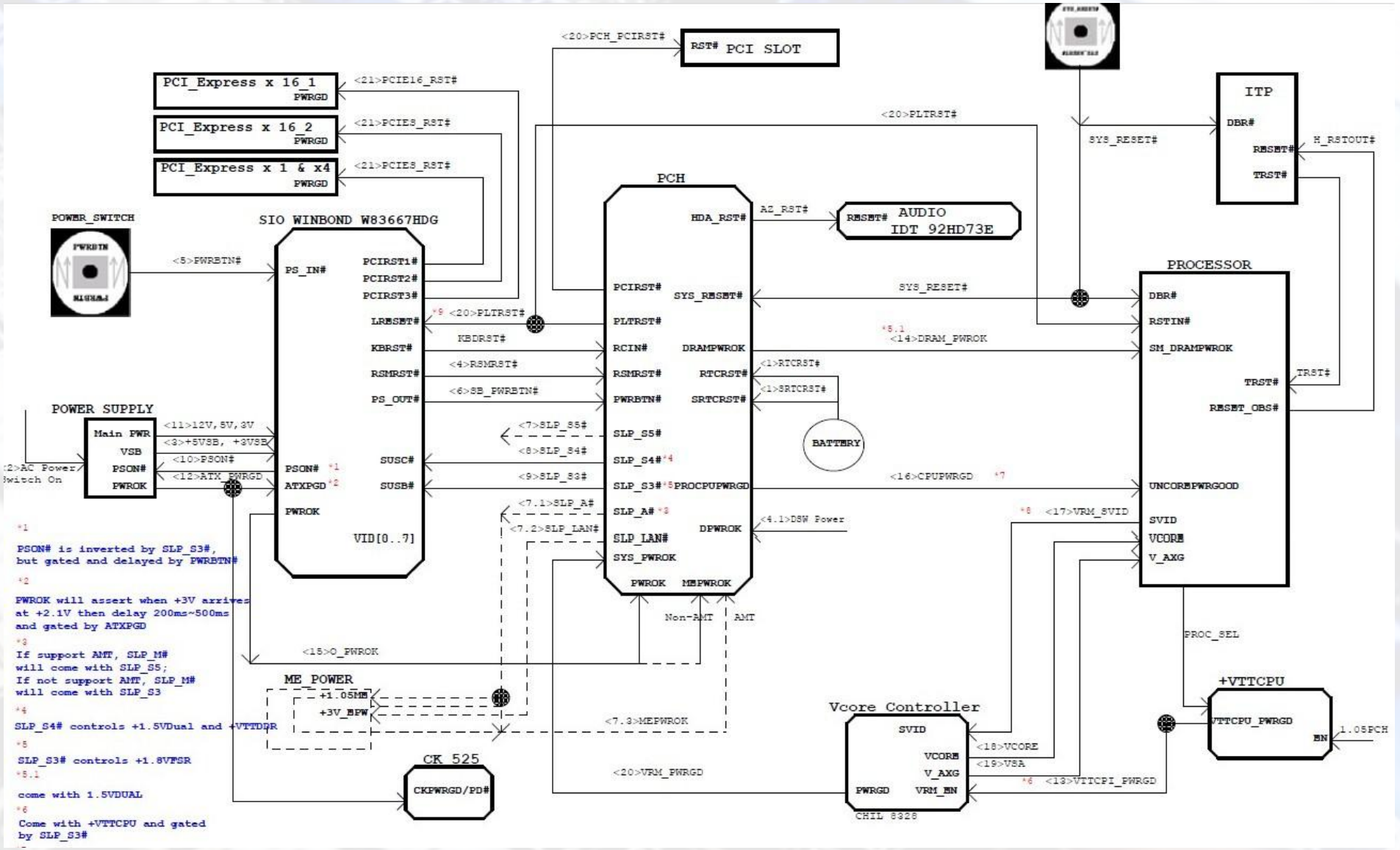
6.8.3 When ASSC is enabled (Exit Deeper Sleeping State)



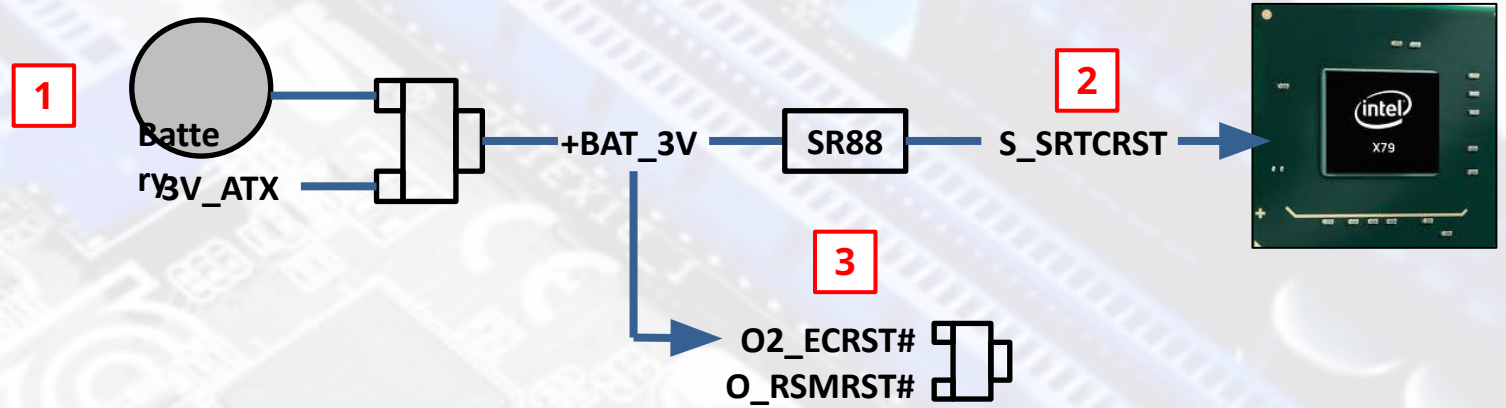
(PWRBTN#IN, KB MS Wakeup)

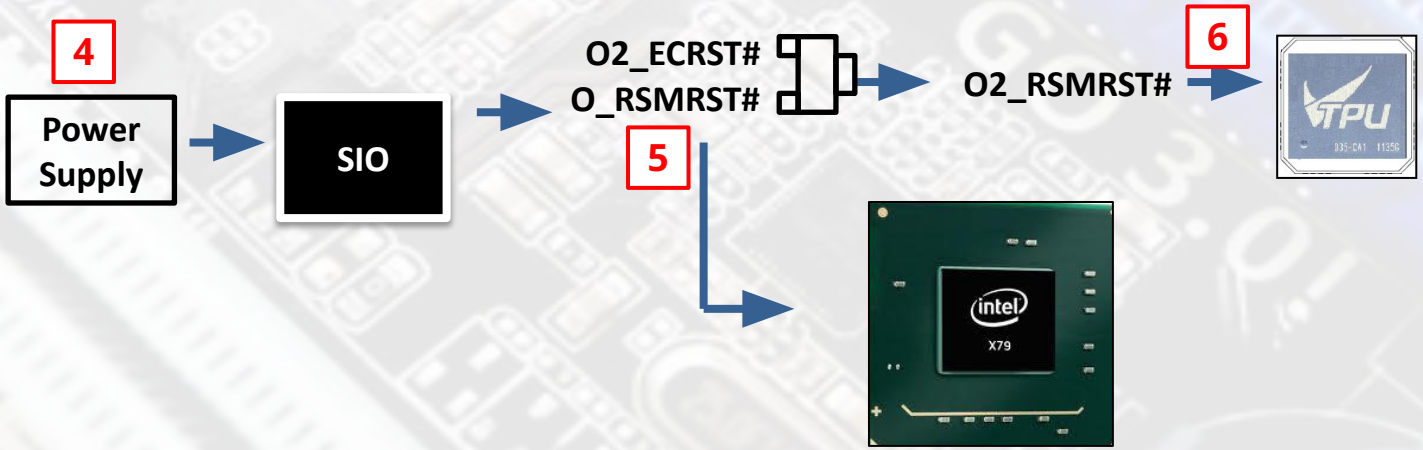


P9X79 Deluxe - Power Sequence

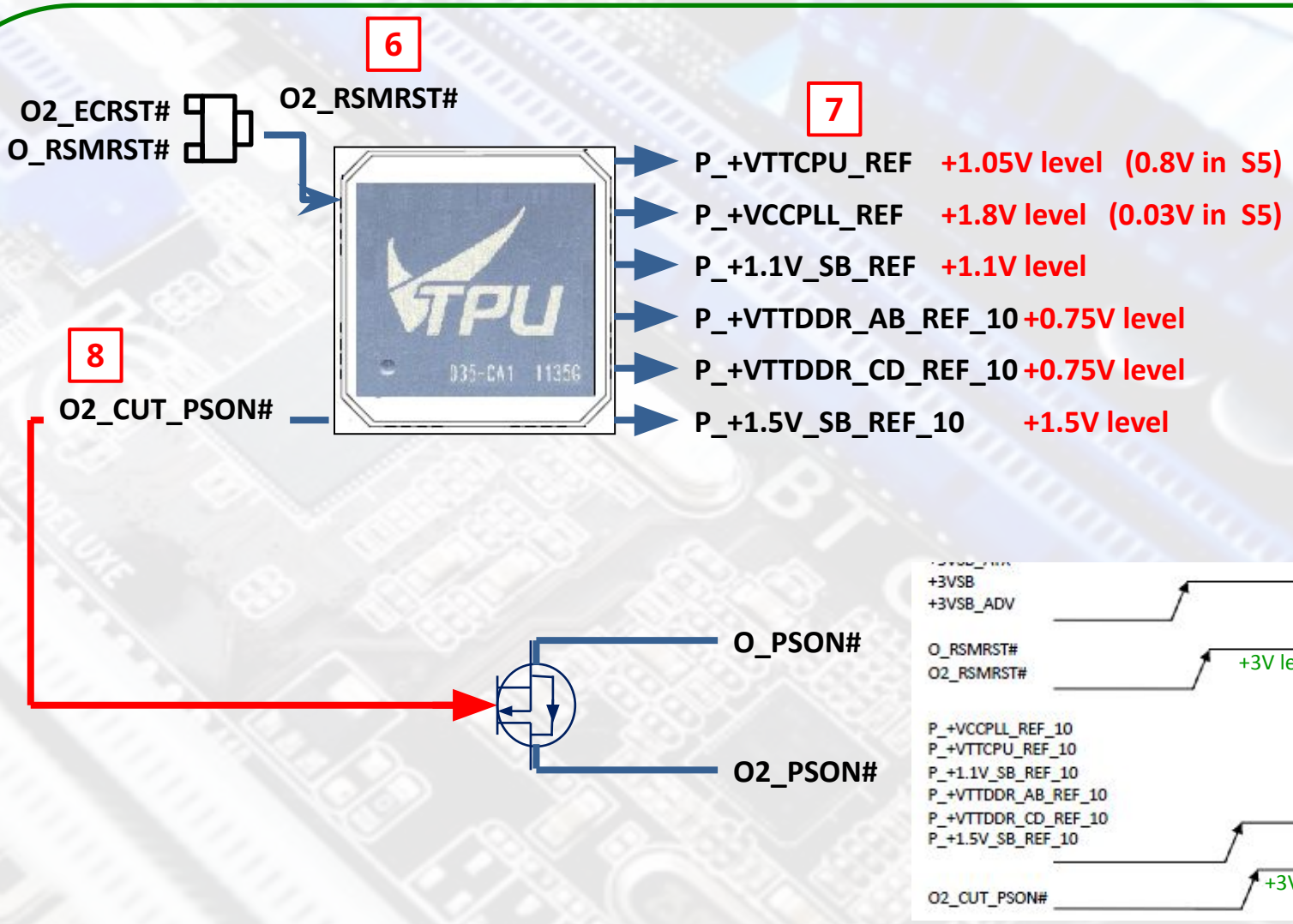


P9X79 Deluxe - Power Sequence (1)

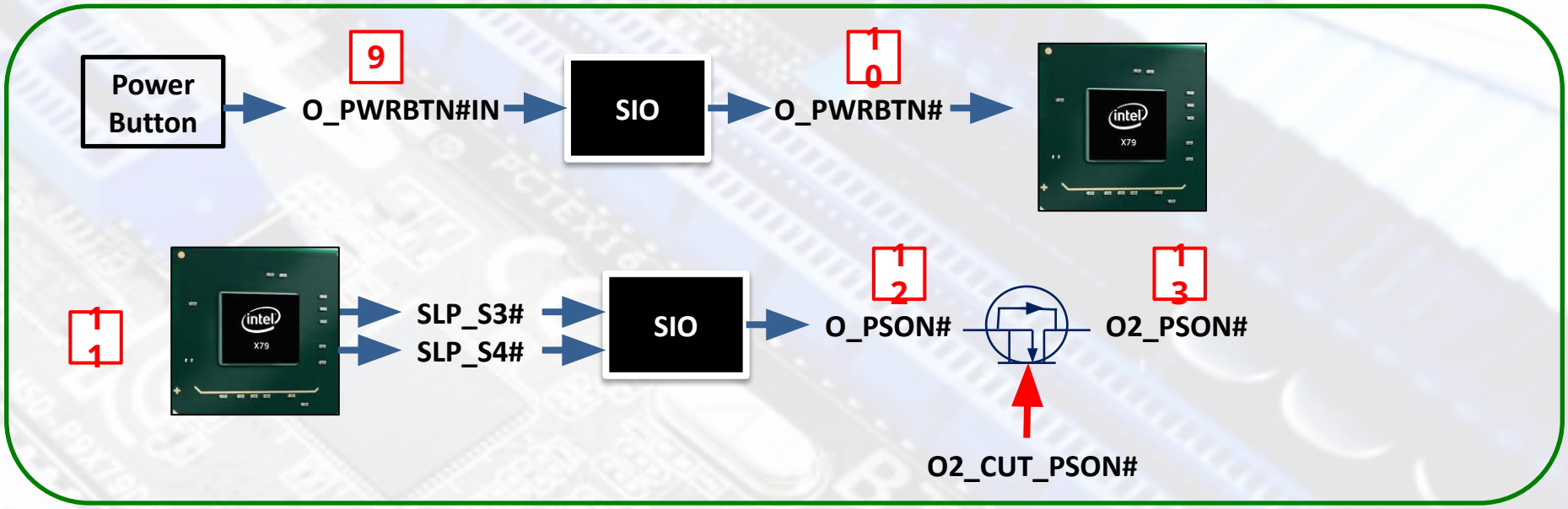


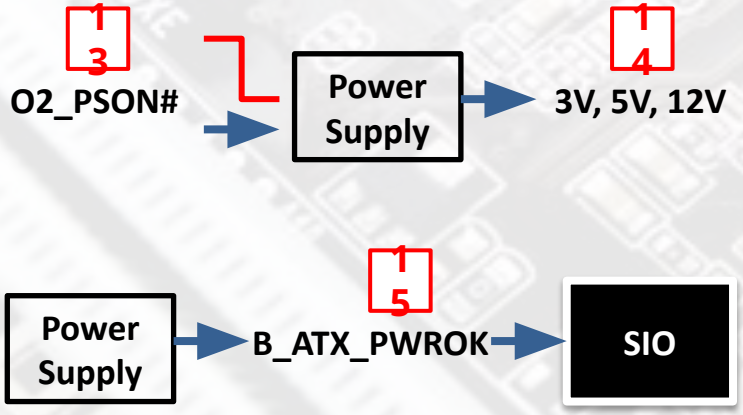


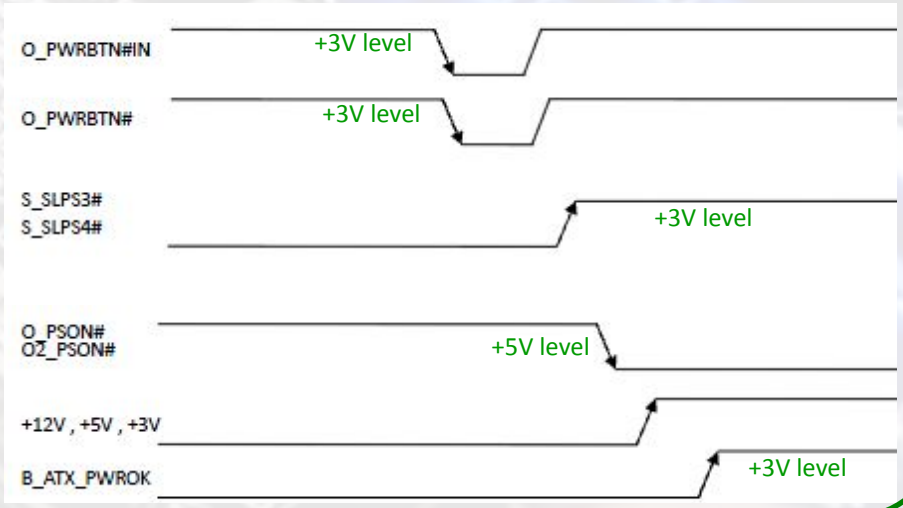
P9X79 Deluxe - Power Sequence (2)



P9X79 Deluxe - Power Sequence (3)







P9X79 Deluxe - Power Sequence (4)

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+VTT_CPU, +1.5VDUAL_AB, +1.5VDUAL_CD, +1.1V_SB, +1.5V_SB

+1.05V level +1.5V level +1.5V level +1.1V level +1.5V level

+1.5VDUAL_CD → SR1478

17

+VDDQ_AB_PWRGD
S_DRAMPWROK → H_DRAMPWROK_AB

IC → +VDDQ_CD_PWRGD
S_DRAMPWROK → H_DRAMPWROK_CD

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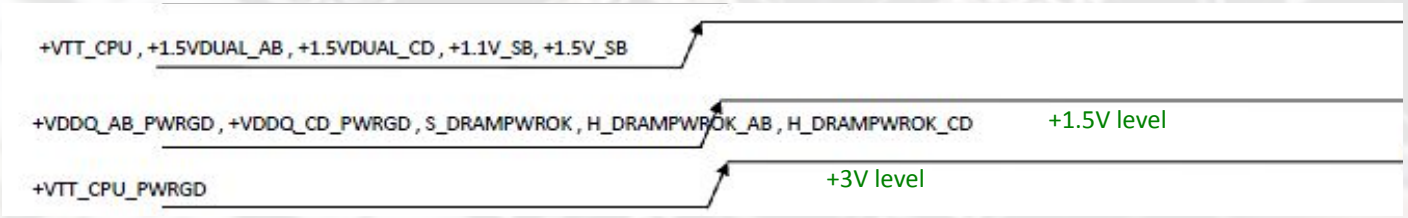
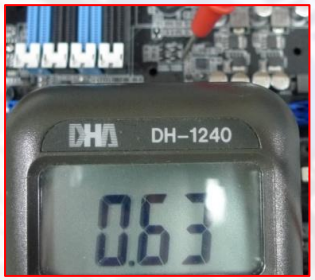
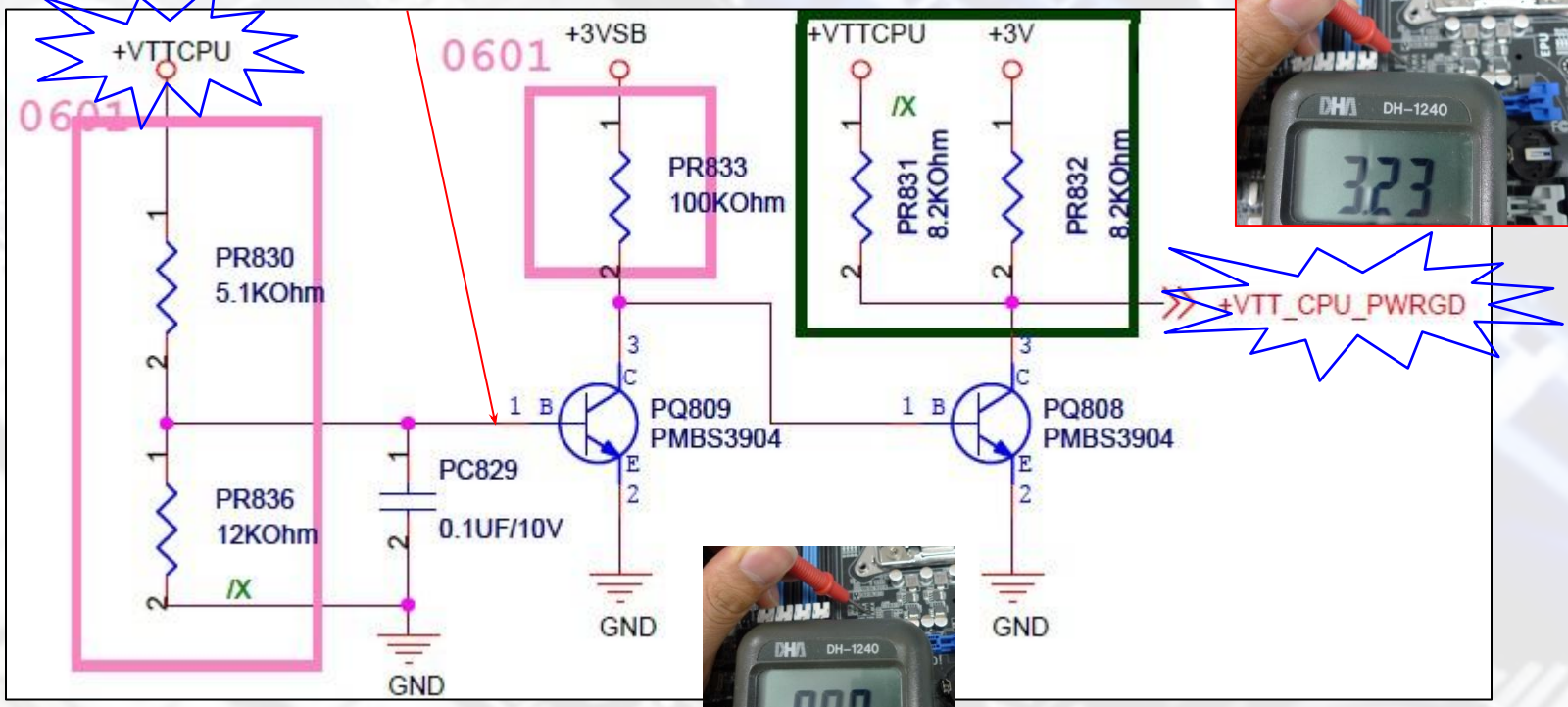
+VTT_CPU → MB Logic Circuit → +VTT_CPU_PWRGD



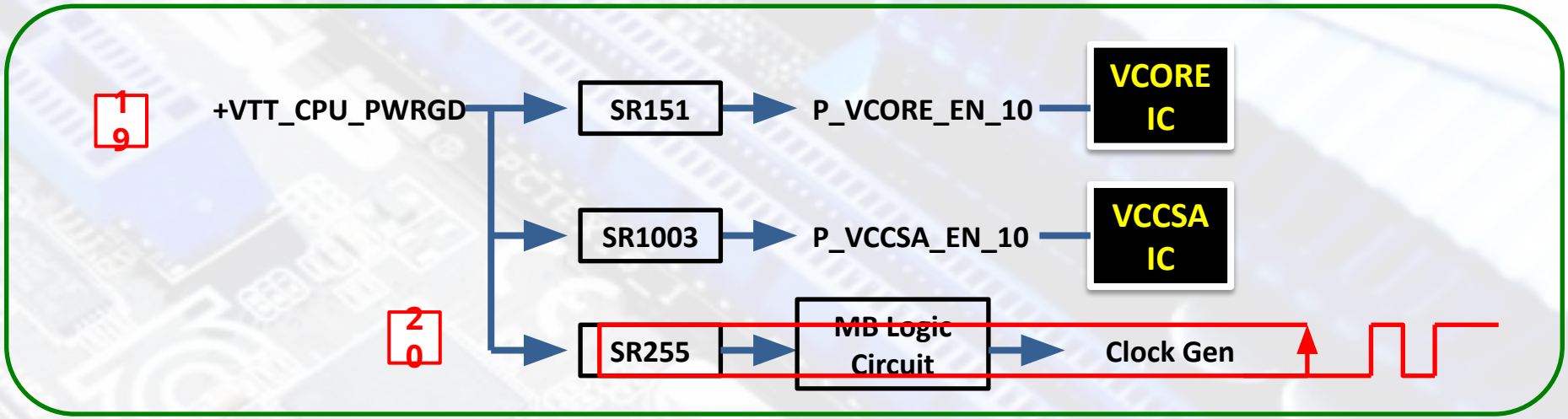
MB Circuit : VTTCPU=>VTTCPU_GD

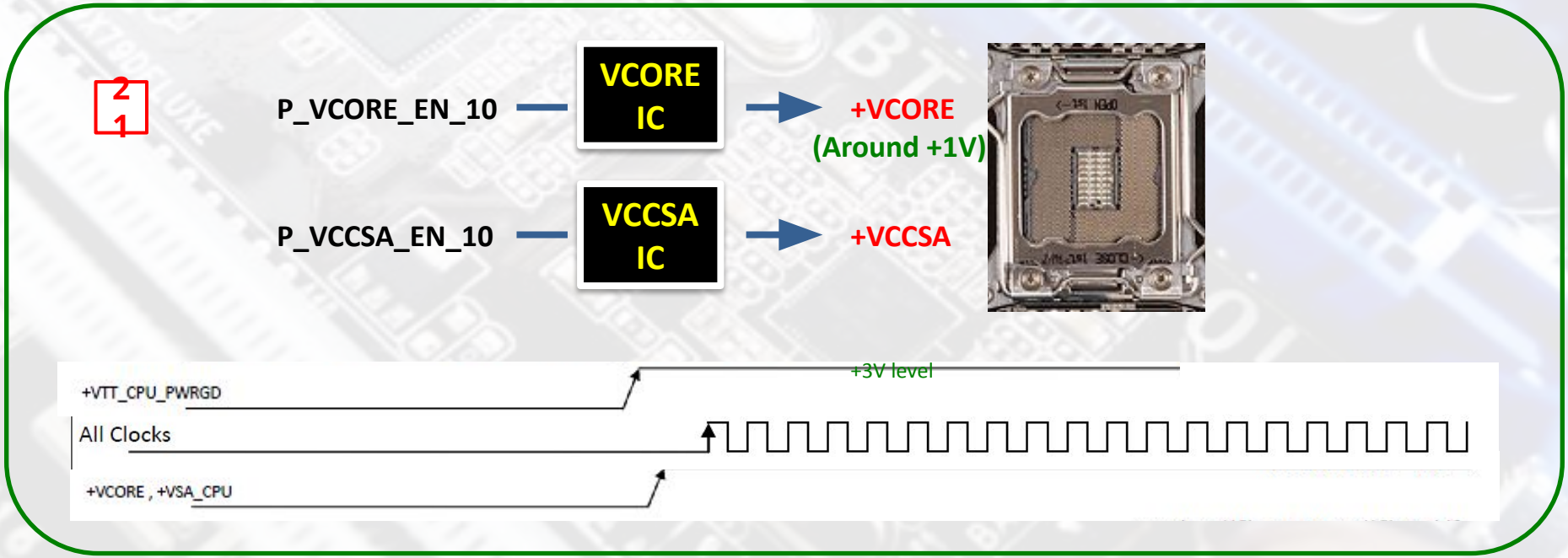
- +VTTCPU => VTT_CPU_PWRGD





P9X79 Deluxe - Power Sequence (5)





P9X79 Deluxe - Power Sequence (6)

22

VCORE IC → P_VCORE_VRDY_6 → MB Logic Circuit → O2_GPI1 → O2R64 → O2_GPO1

O2_GPI1 → EC

O2_GPO1 → SR535 → S_VRMPWRGD → 

VCORE IC → +VSA_CPU_PWRGD → MB Logic Circuit → P_+VCCPLL_REF_R_10

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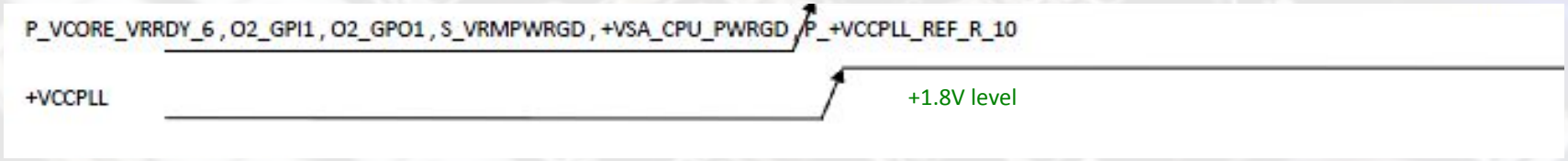
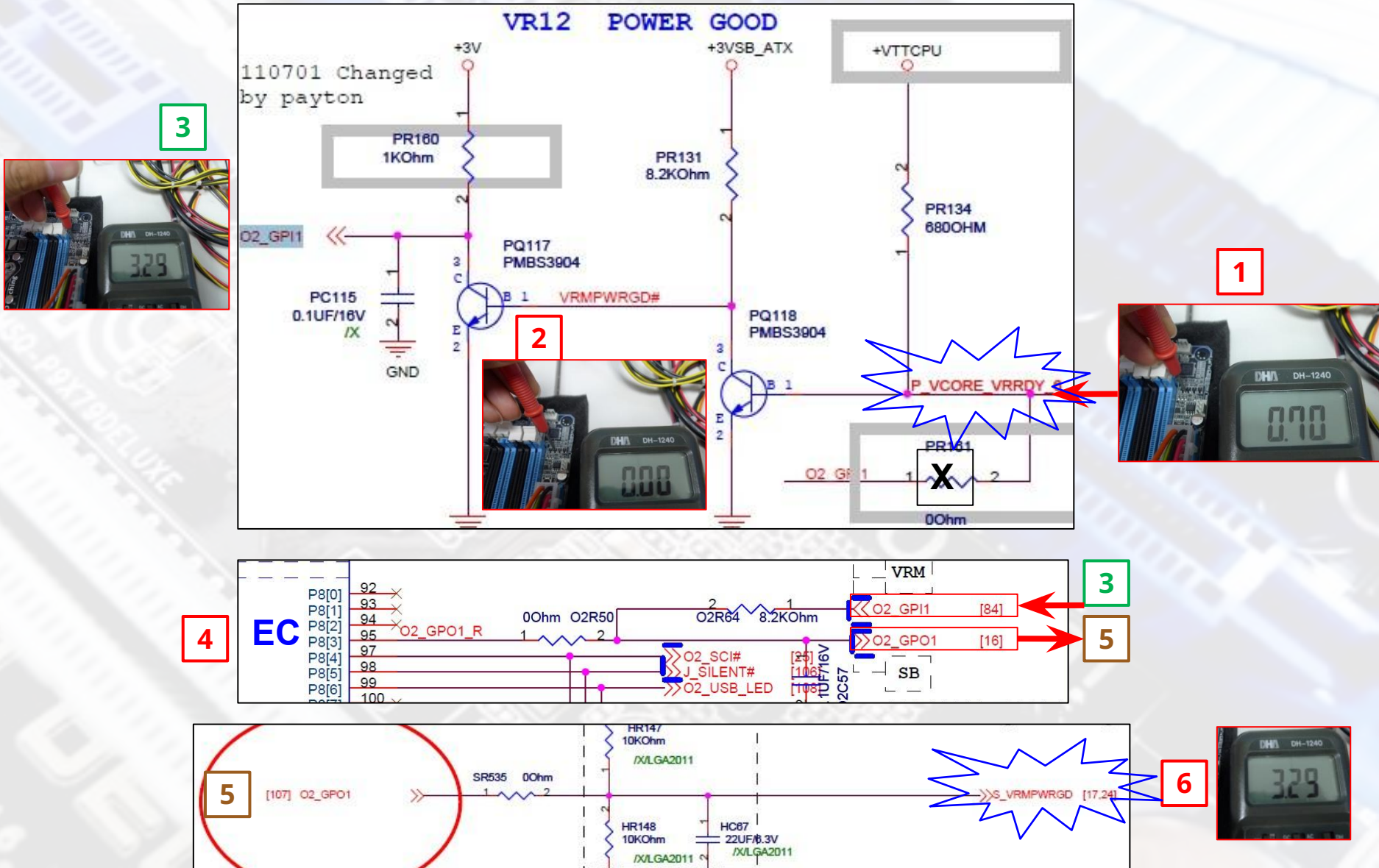
P_+VCCPLL_REF_R_10 → VCCPLL IC → +VCCPLL



MB Circuit : VRRDY=>SYS_PWRGD

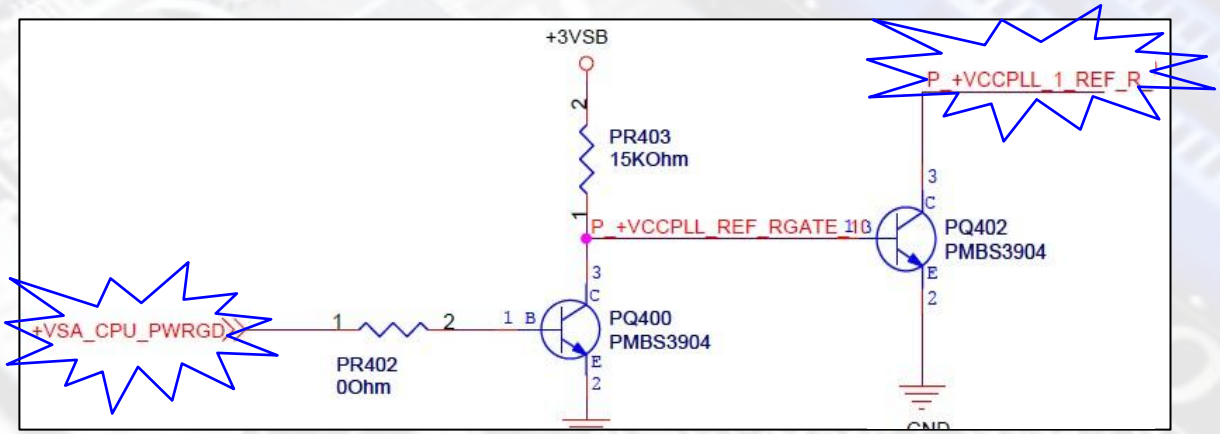


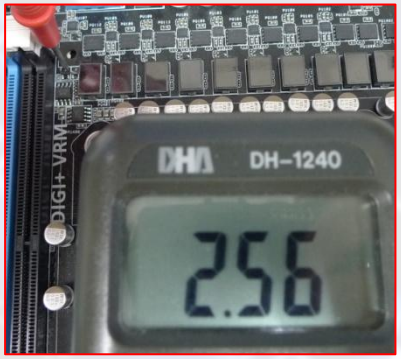
MB Circuit : VSA_PG=>VCCPLL_1_REF

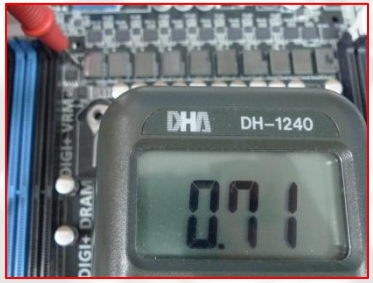
- +VSA_CPU_PWRGD => P_+VCCPLL_REF_R_10

On P67, No sequence requirement on +CPUPLL

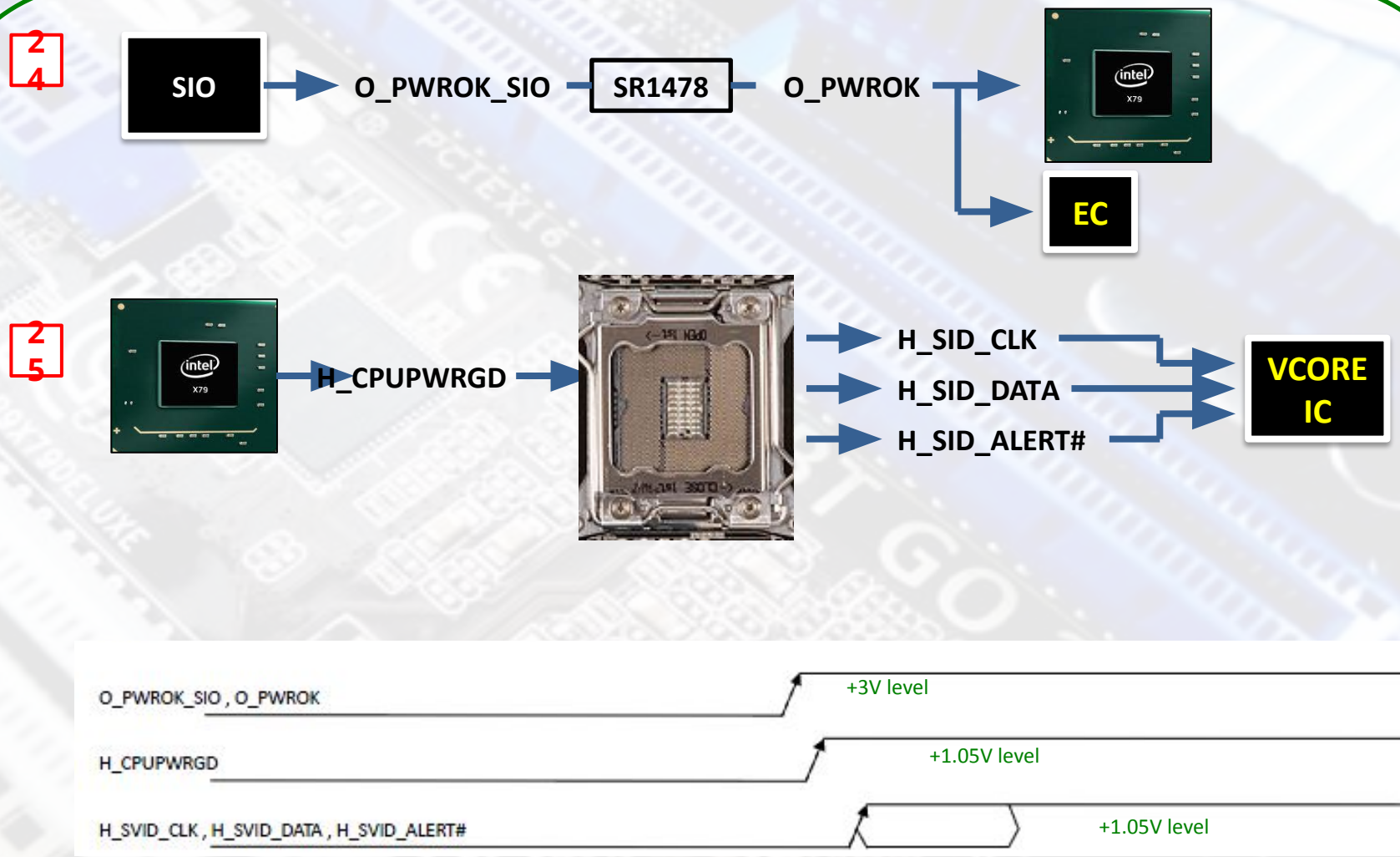
On X79, need use VSA_PWRGD to enable +CPUPLL



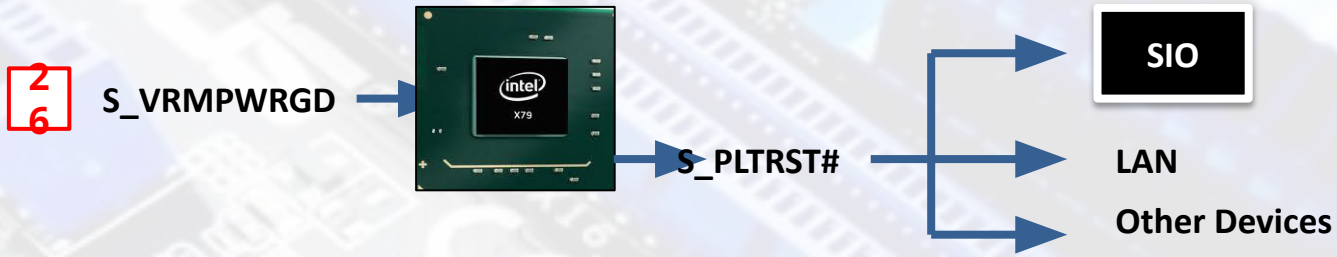


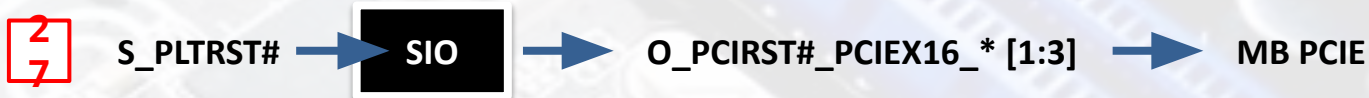


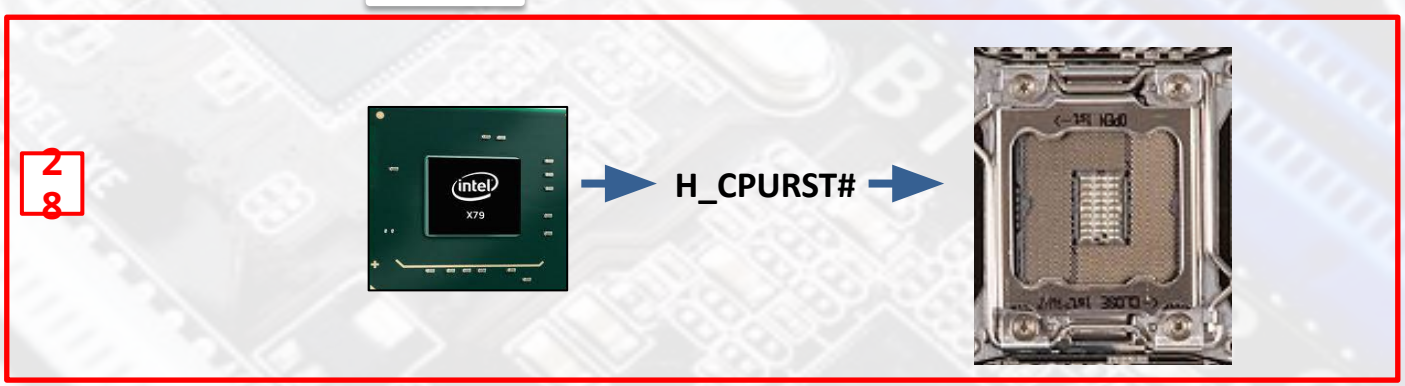
P9X79 Deluxe - Power Sequence (7)

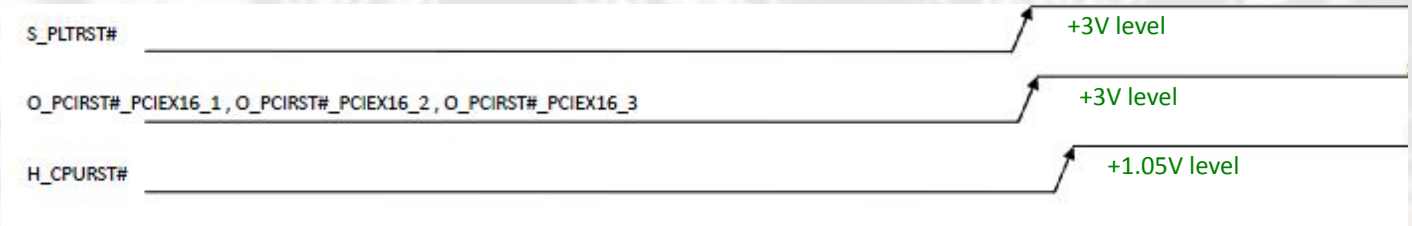


P9X79 Deluxe - Power Sequence (8)







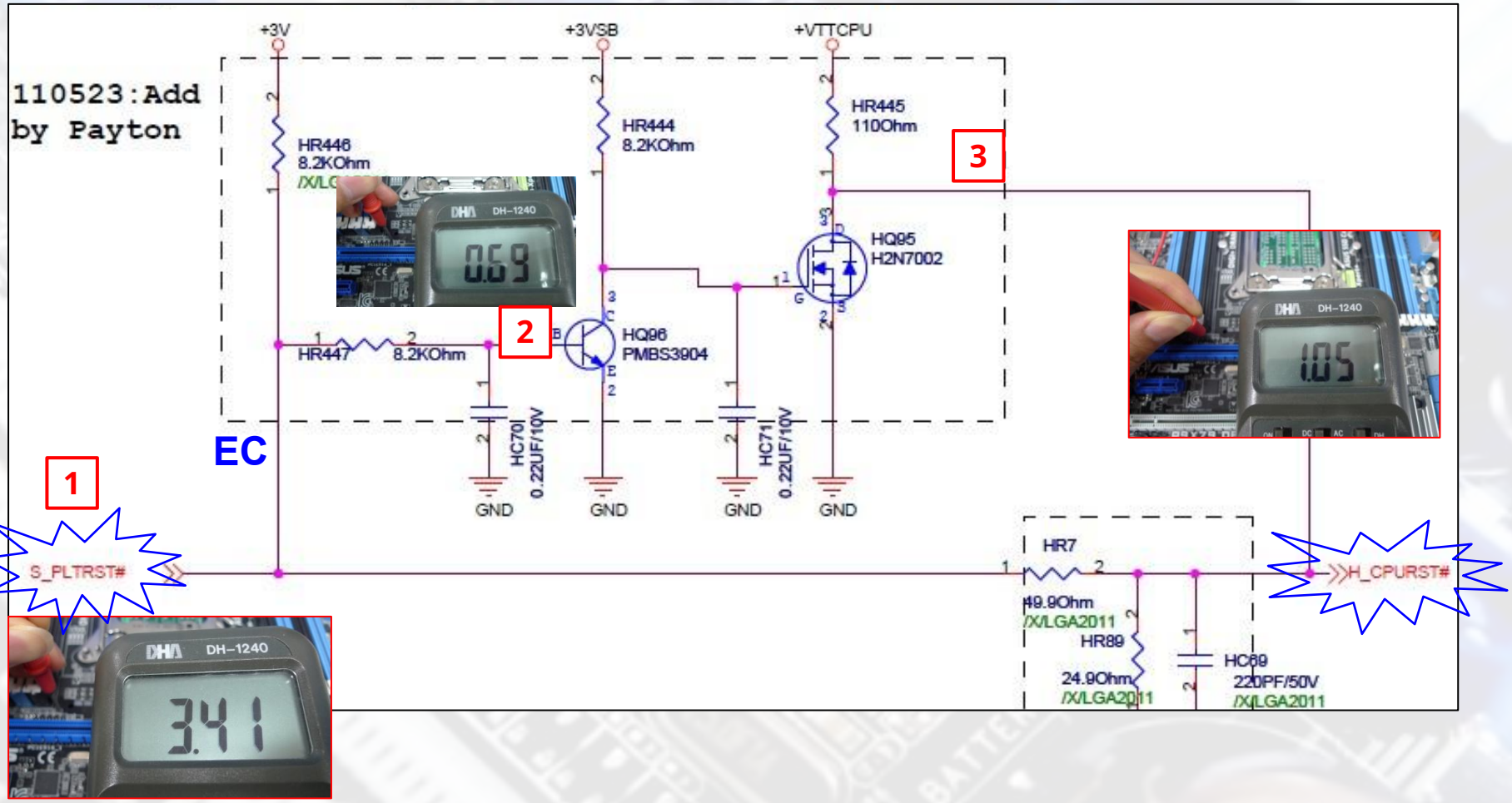


P9X79 – Agenda

- Intel X79 Platform Structure
- P9X79 Series Architecture
- New Feature
- Difference With P8 Series
- Clock Distribution
- Power Flow & Critical Power on X79 Platform
- Power Sequence
- **Embedded Controller Introducing**
- SIO and Other Power Chipset Introducing
- Power theory and working condition
- Communication BUS Introducing

MB Circuit : PLTRST=>CPURST

- S_PLTRST => H_CPURST#



P9X79 Deluxe – Embedded Controller (1)

- **EC is a 8051 micro-processor**
- **EC functions**
  - DIGI+ Power Control--**SMBUS interface**
  - Over-voltage control, 3.2V/512=6.25mV/step--**PWM interface**
  - Voltage sense--**ADC interface**
  - TPU, EPU & EUP Control --**GPIO interface**
  - Memory OK--**GPIO interface**
  - PWM Fan Control--**PWM & Fan-in interface**
  - SIO & PCH -- **LPC interface**
  - BIOS

P9X79 Deluxe – Embedded Controller (2)

PWM interface
PIN33 O2_PWM0(VCCPLL)
PIN34 O2_PWM1(VTTCPU)
PIN35 O2_PWM2(1.1V_SB)
PIN36 O2_PWM3(VTTDDR_AB)
PIN37 O2_PWM4(VTTDDR_CD)
PIN38 O2_PWM5(1.5V_SB)

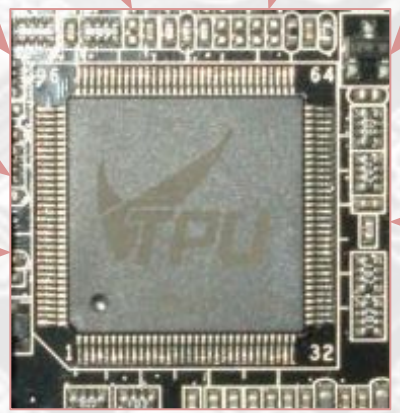
LPC interface
PIN115 F_LAD0
PIN116 F_LAD1
PIN117 F_LAD2
PIN118 F_LAD3
PIN108 F_SERIRQ#
PIN111 S_SLPRST#
PIN112 F_FRAME#
PIN113 C_PCI_EC

GPIO interface
(TPU)
PIN11 O2_OC_OK_R
(EPU)
PIN9 O2_EPU_R
PIN70O2_+5VDUAL_USBKB_EUP
(MEM OK)
PIN36 O2_MEM_OK_R

PWM & FAN in interface
PIN6 O2_SEN_FAN1
PIN7 O2_SEN_FAN2
PIN8 O2_SEN_FAN3
PIN52 O2_FANPWR_PWM1
PIN53 O2_FANPWR_PWM2
PIN54 O2_FANPWR_PWM3

SMBUS interface
PIN69 O2_SMB_SWITCH
(Power)
PIN72 O2_SMB1_DATA
PIN73 O2_SMB1_CLK
(EEPROM)
PIN76 O2_SMB2_DATA
PIN77 O2_SMB2_CLK

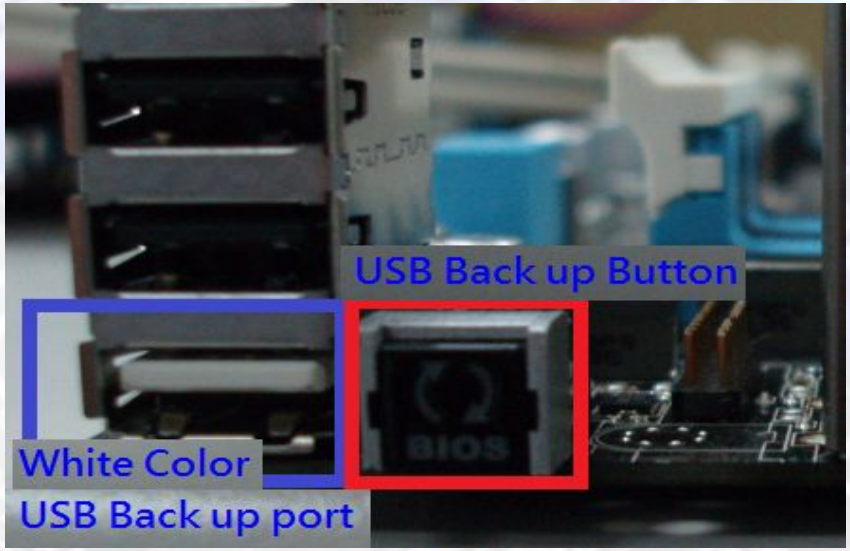
Flashback interface
PIN84 O2_USB_SEL
PIN85 O2_USB_IN_R
PIN86 O2_SPI_SWITCH
PIN99 O2_USB_LED
(USB)
PIN44 O2_USB+
PIN45 O2_USB-
(SPI)
PIN101 O2_SPI_CLK
PIN102 O2_SPI_DO
PIN103 O2_SPI_DI
PIN104 O2_SPI_CS#



Control Signals
(Power)
PIN48,65,83,96 +3VSB
PIN31 O2_VDDA
PIN30,32 O2_VREF
(CLK)
PIN81 XCLKO
PIN82 XCLKI
(Reset)
O2_RSMRST#
(PWRGD)
PIN108 O2_GPO1_R
PIN128 O2_GPI1
(Others)
PIN39 O2_GPO2
PIN40 O2_GPO3
PIN78 S_SLPS3#
PIN79 S_SLPS4#
PIN67 O_PWROK
PIN63 O2_CUT_PSON
PIN98 J_SILENT#

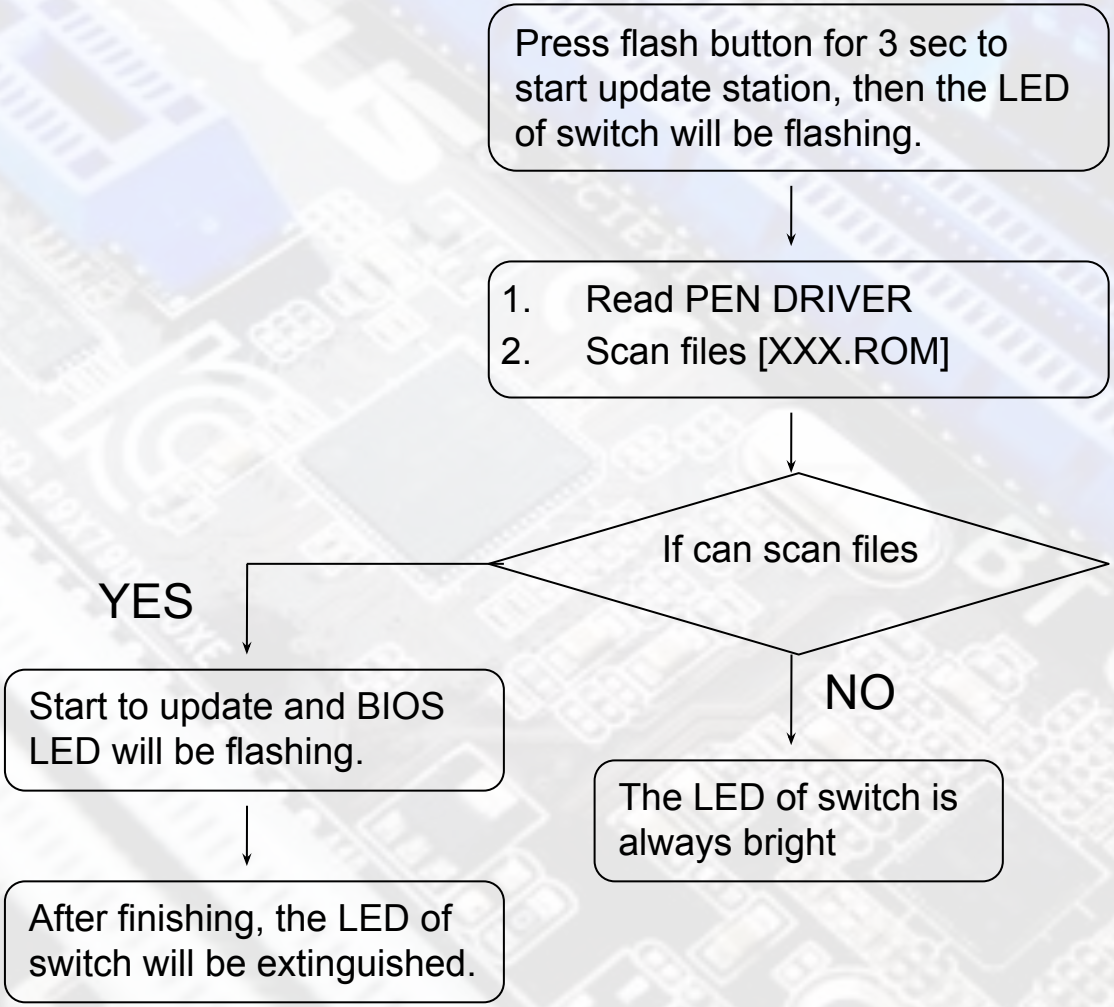
EC USB Back up function - 1

- USB Back up Condition



- USB Type : FAT32、FAT type
- BIOS Image : Follow X79 each Model Crash free naming(EX: **X79 DLX: P9X79D.ROM、X79 PRO: P9X79PRO.ROM**…)

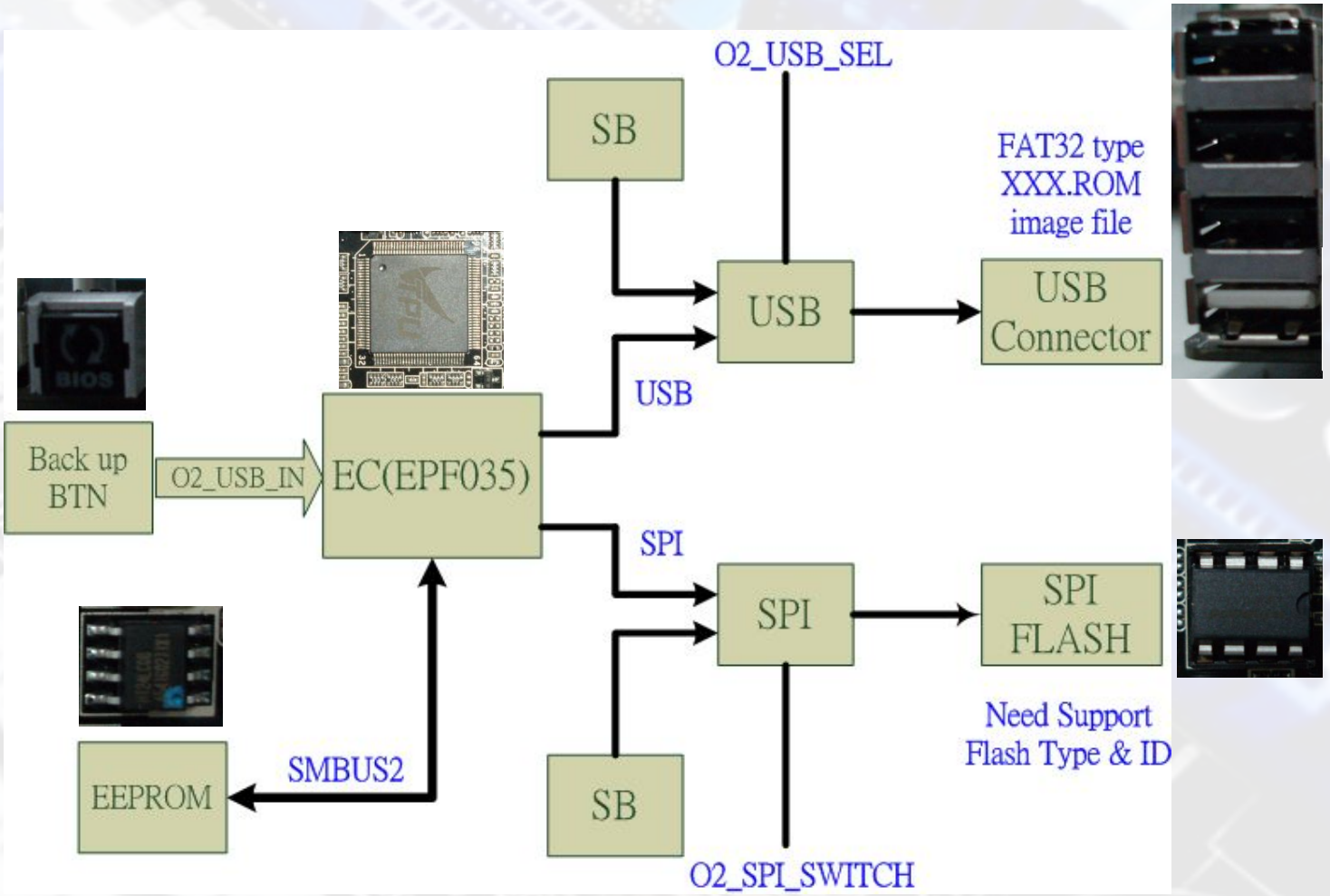
EC USB Back up function - 2



According these signals connecting to EC, EC can realize present system status

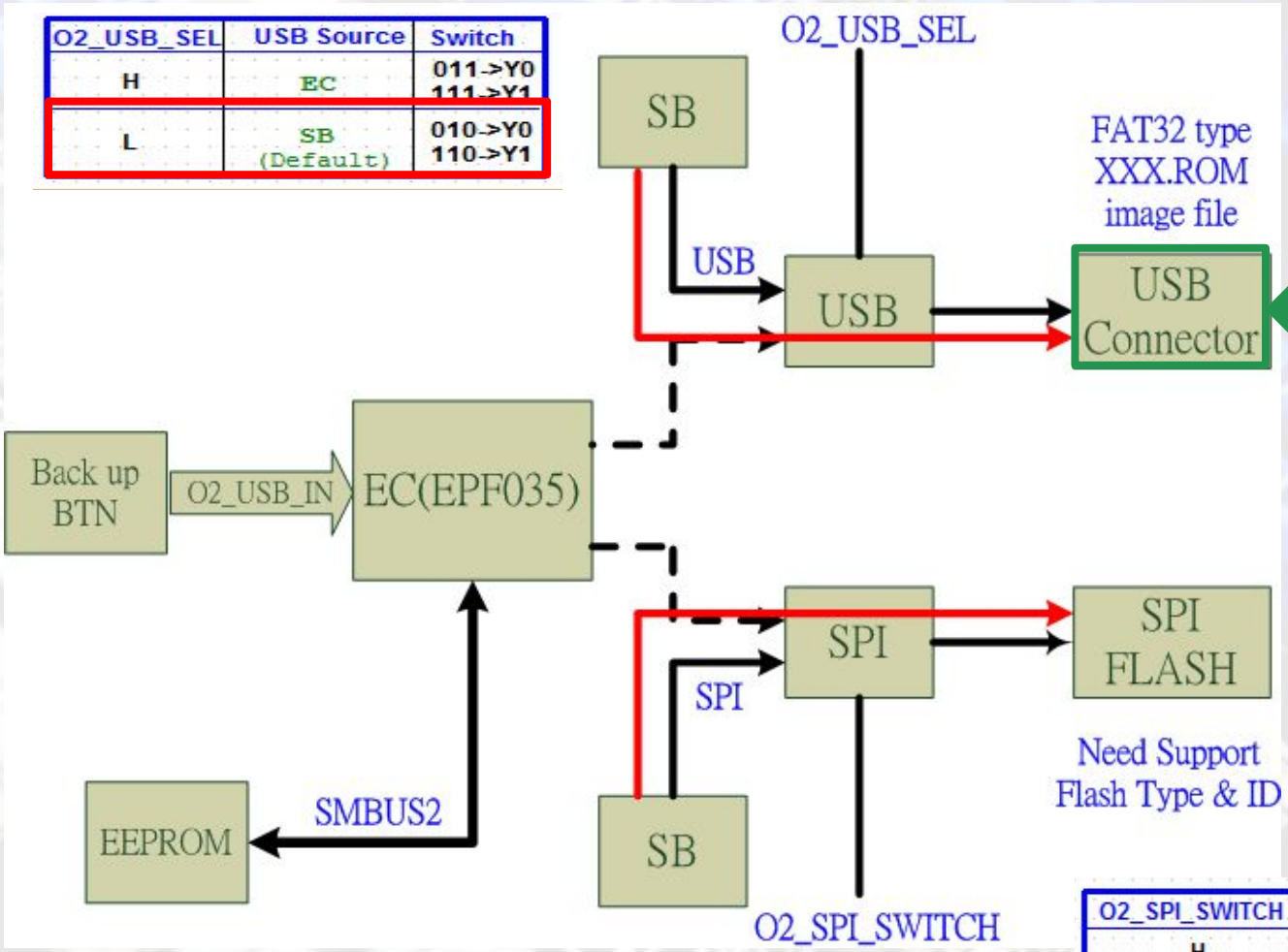
	SLP_S3	SLP_S4	PWROK
G3	0	0	0
S5	**0 or 1**	**0**	**0**
S0	1	1	1
S1	1	1	1
S3	0	1	0
S4	0	0	0

EC USB Back up function - 3



EC USB Back up function - 4

O2_USB_SEL	USB Source	Switch
H	EC	011->Y0 111->Y1
L	SB (Default)	010->Y0 110->Y1



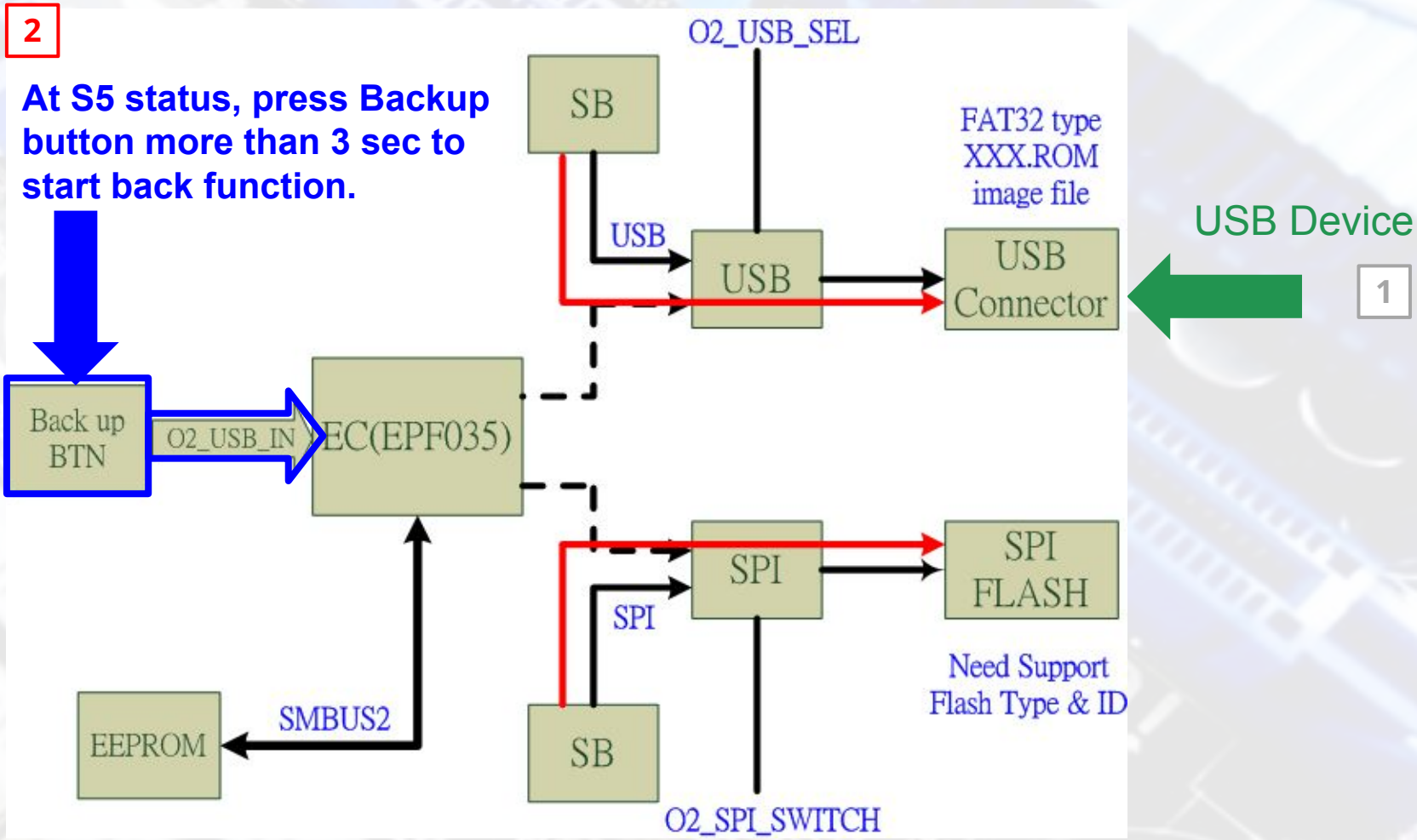
Default : **SB to USB**
SPI to SB

1

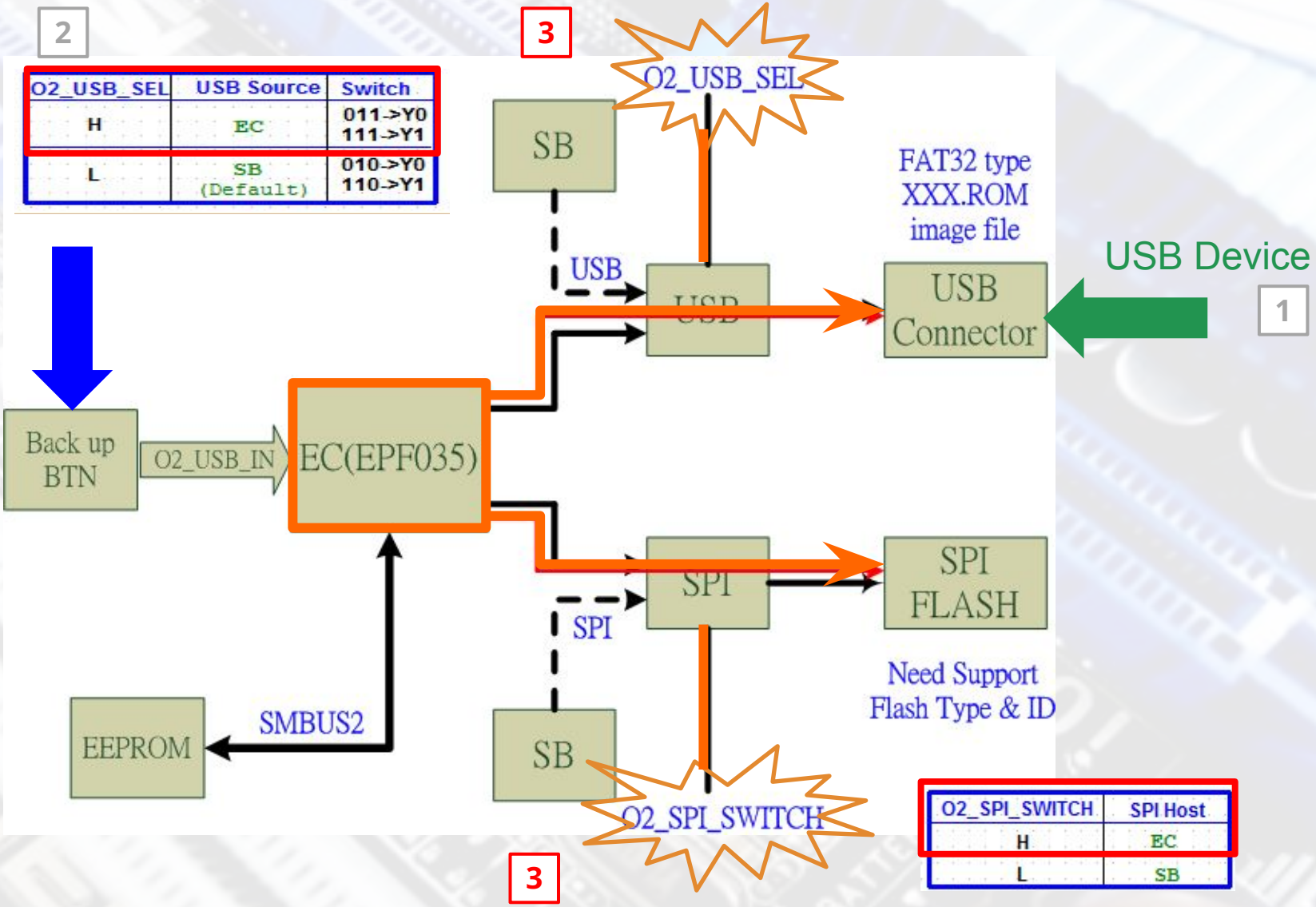
USB Device

O2_SPI_SWITCH	SPI Host
H	EC
L	SB

EC USB Back up function - 5



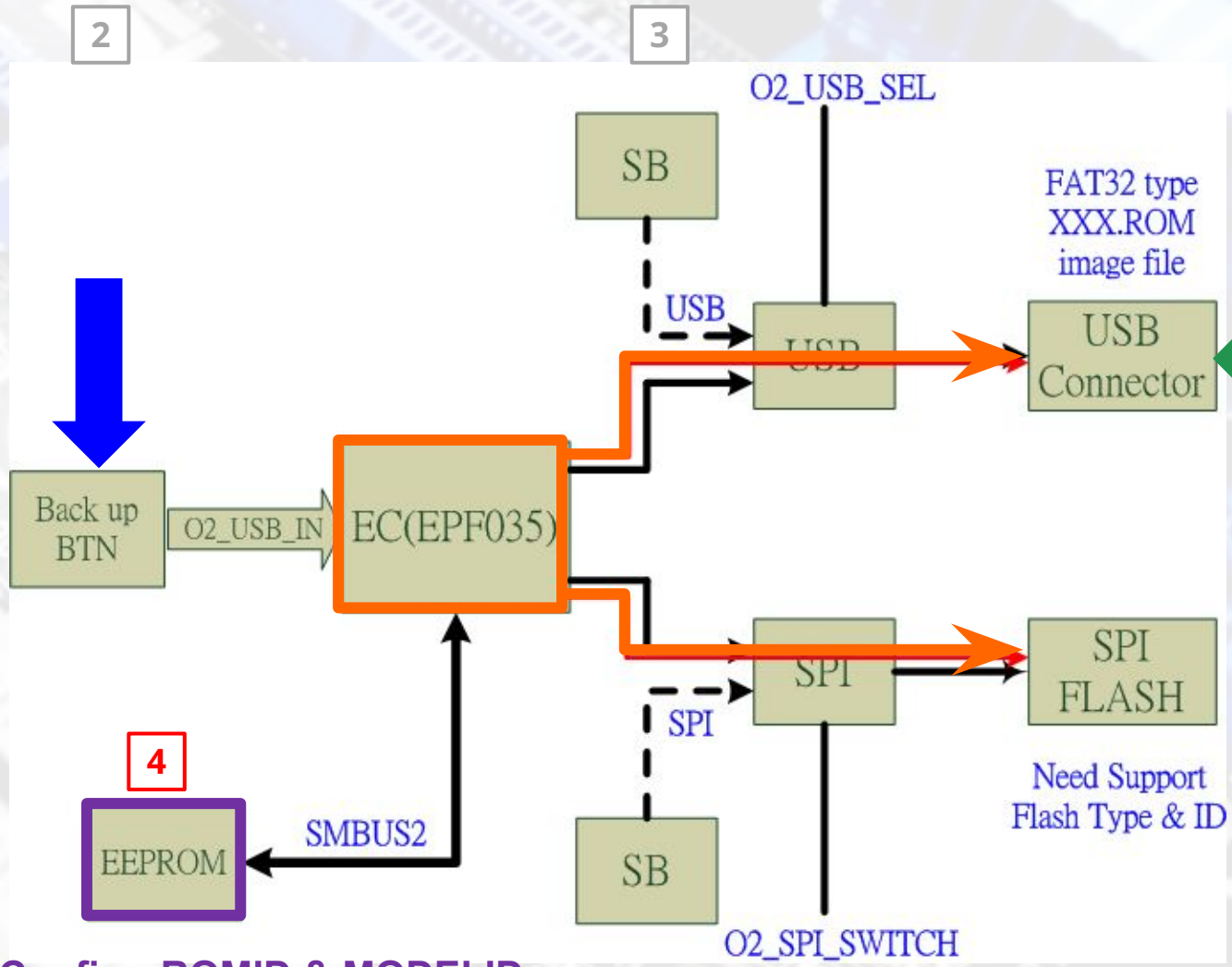
EC USB Back up function - 6



O2_USB_SEL	USB Source	Switch
H	EC	011->Y0 111->Y1
L	SB (Default)	010->Y0 110->Y1

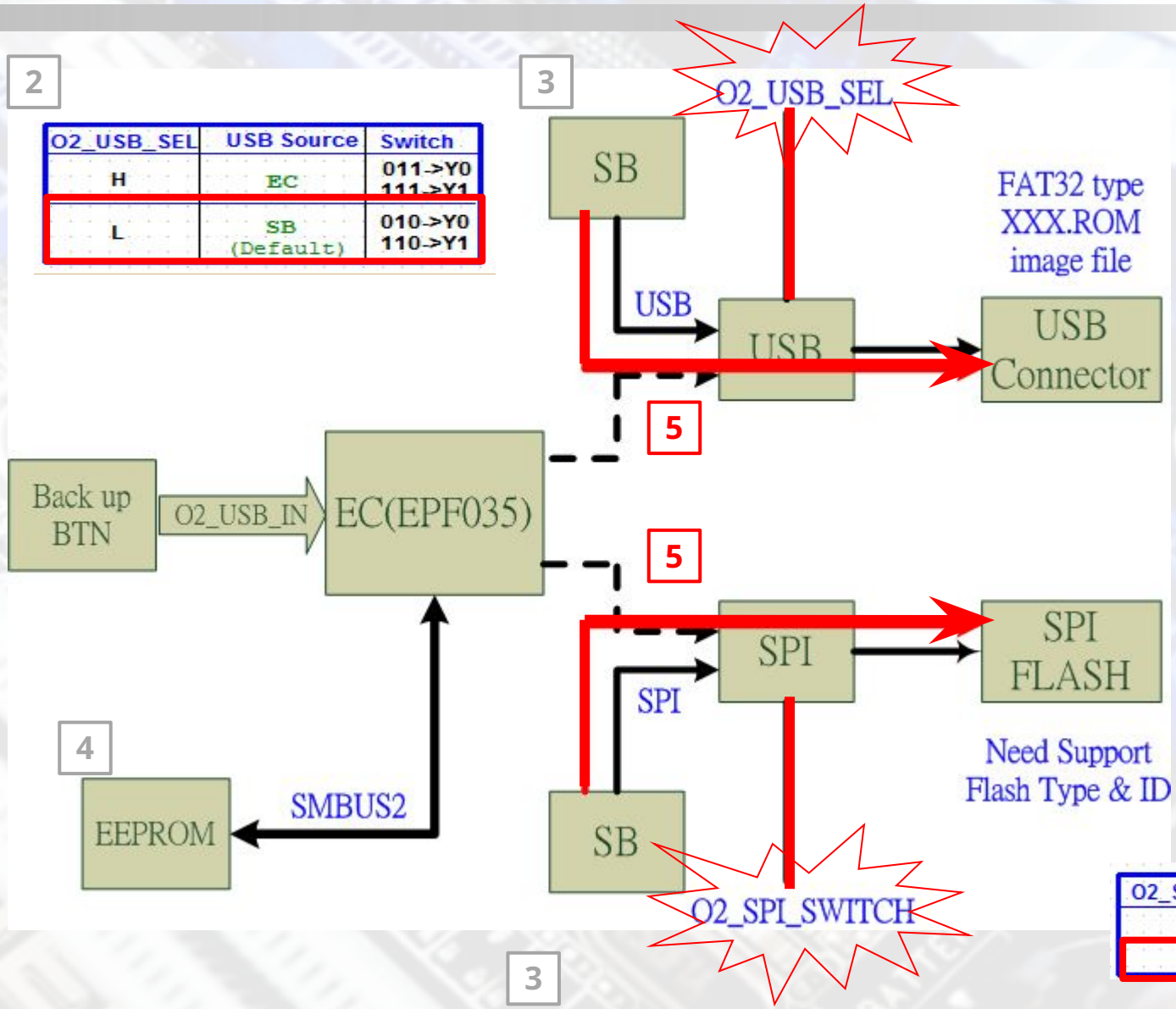
O2_SPI_SWITCH	SPI Host
H	EC
L	SB

EC USB Back up function - 7



Confirm ROMID & MODELID and others information are normal

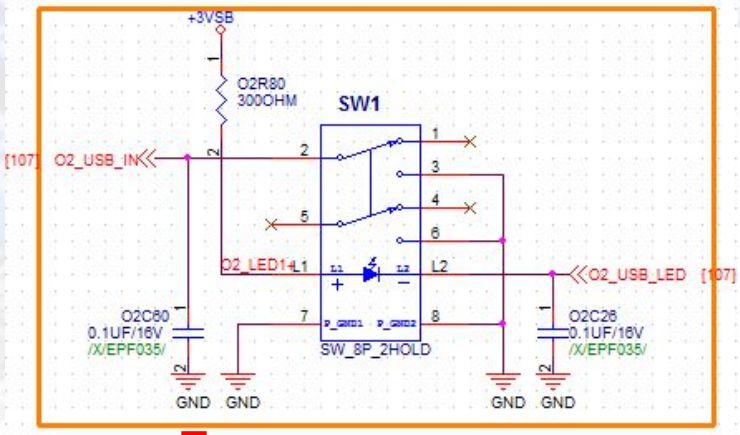
EC USB Back up Function - 8



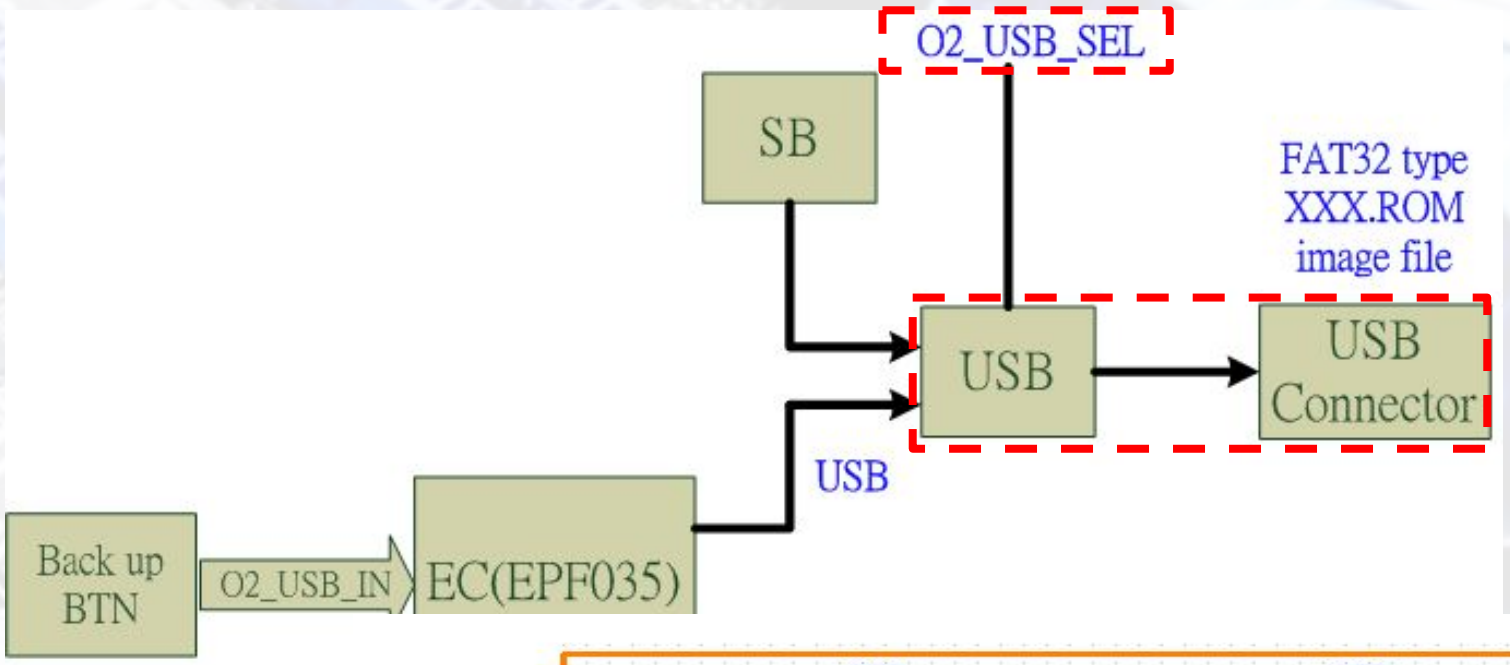
O2_USB_SEL	USB Source	Switch
H	EC	011->Y0 111->Y1
L	SB (Default)	010->Y0 110->Y1

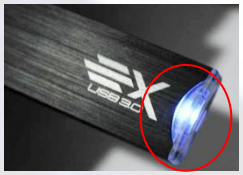
O2_SPI_SWITCH	SPI Host
H	EC
L	SB

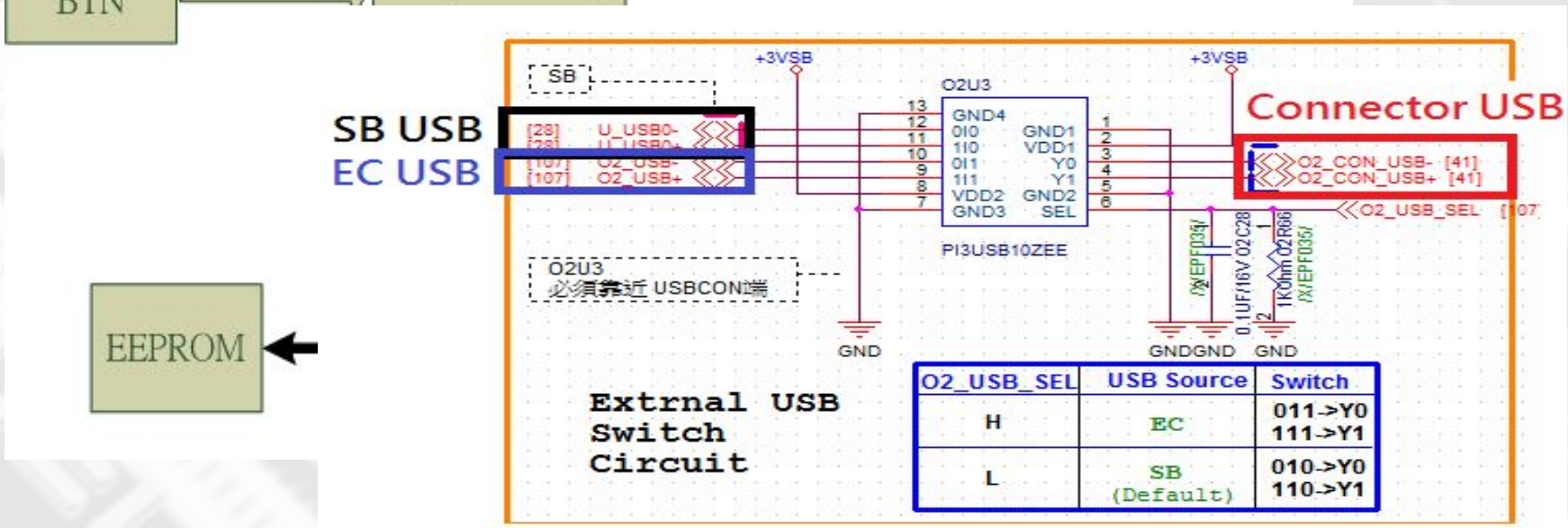
How to Debug Flashback Function - 1



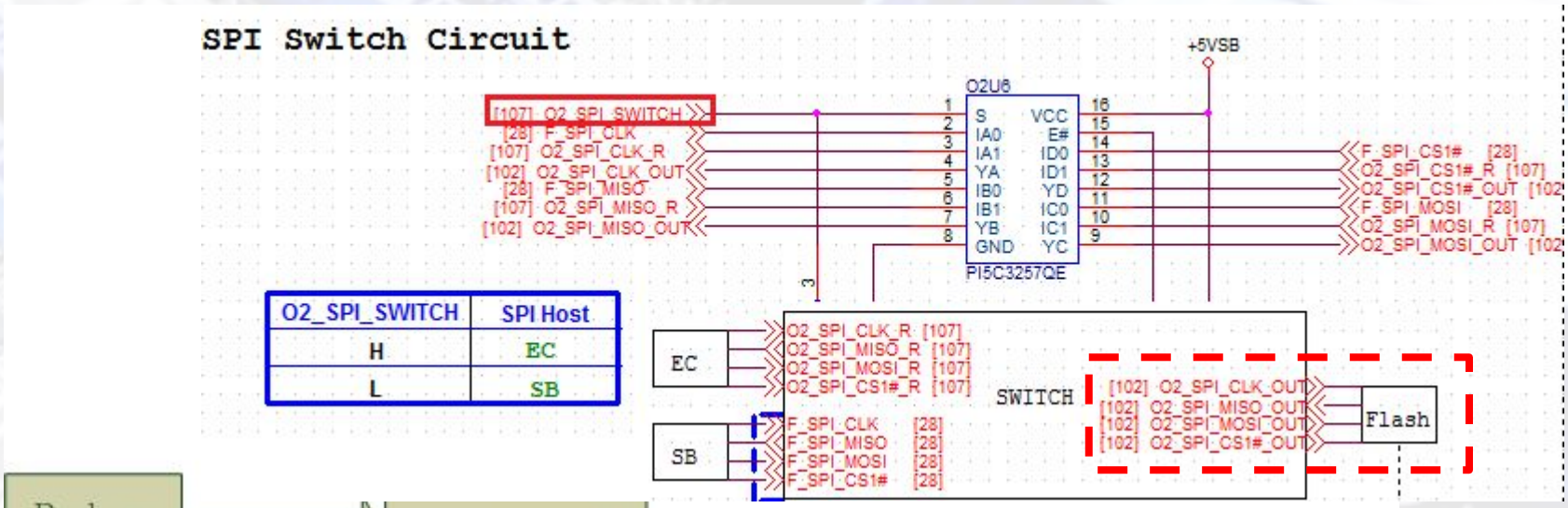
How to Debug Flashback Function - 2

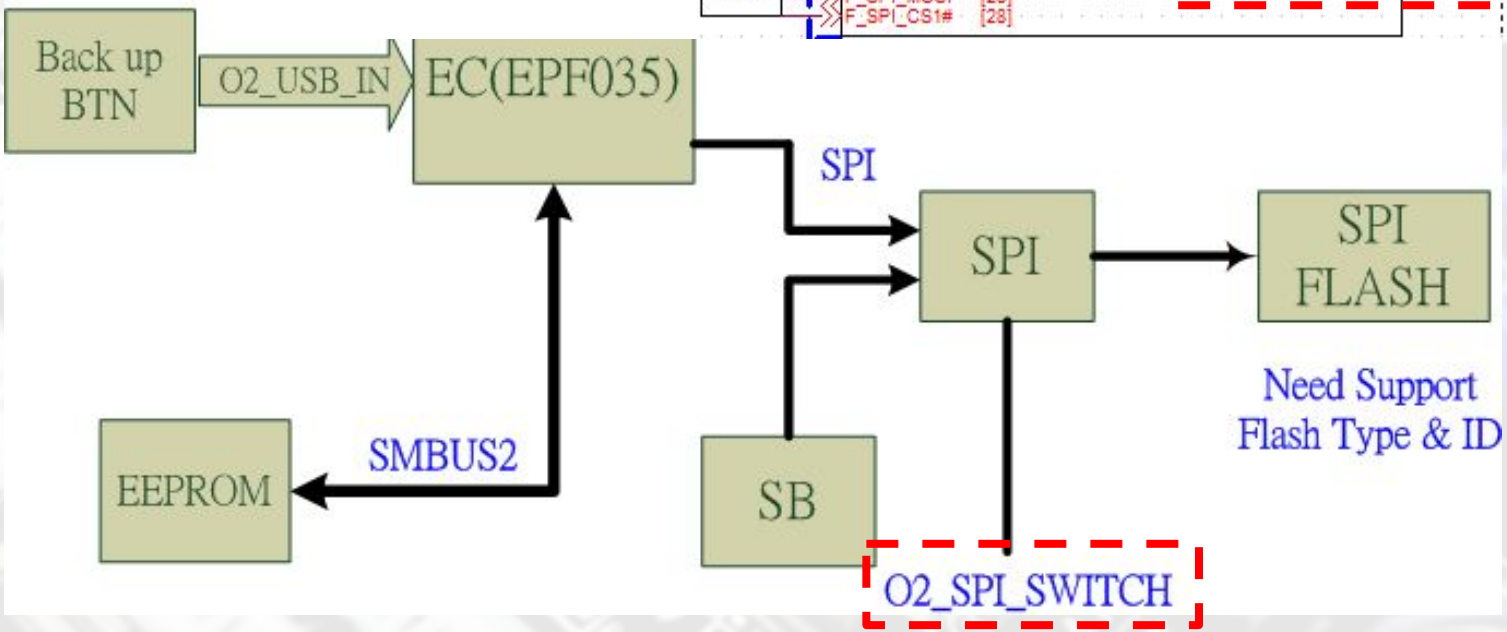




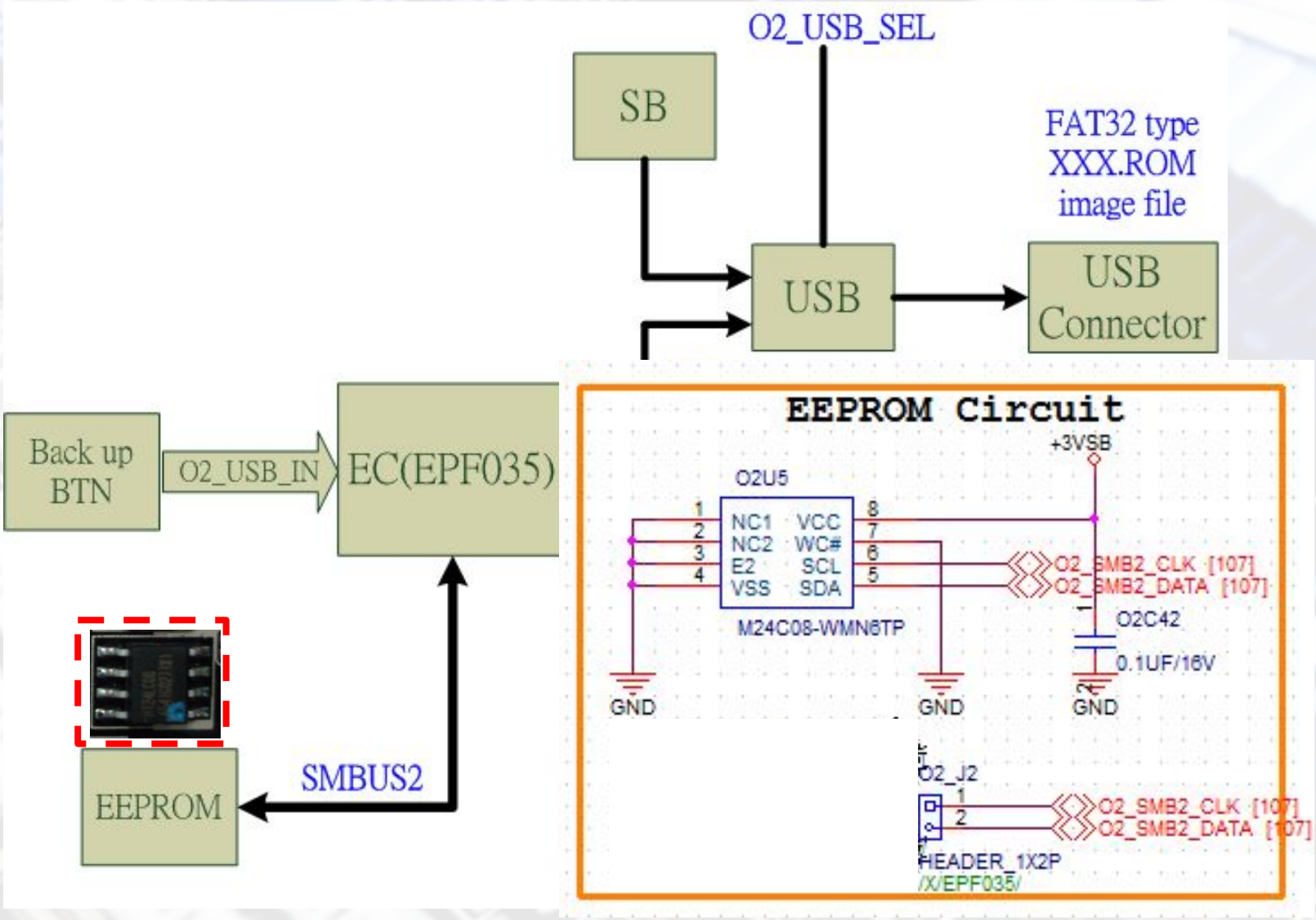


How to Debug Flashback Function - 3





How to Debug Flashback Function - 4



EC Broken Status

- When System BIOS update EC Firmware

EC Broken status:

- EC flash is corrupted

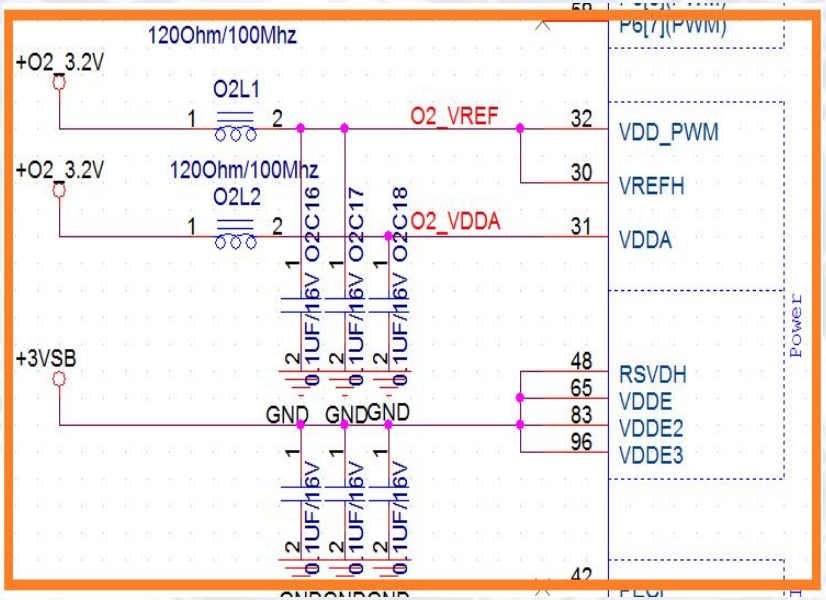
  The data in the EC or EC flash might be corrupted.
  Please contact ASUS Technical Support for help

- EC flash update fail

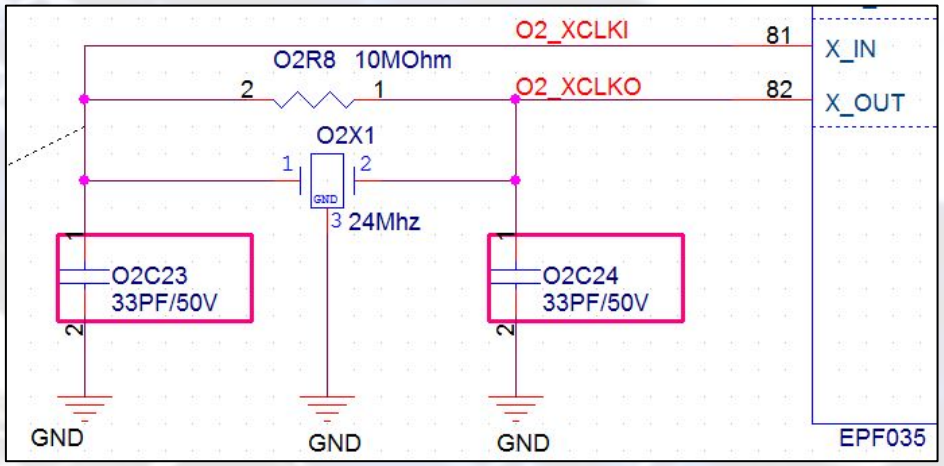
  The data in the EC or EC flash might be corrupted.
  Please contact ASUS Technical Support for help

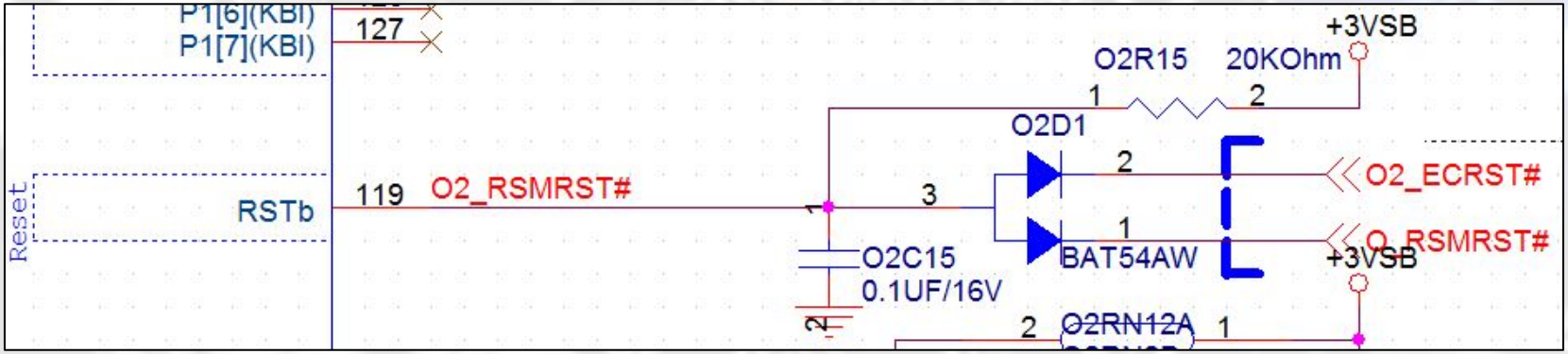
EC - Can’t Boot Status - 1

- **Power & Reset & XTAL:**



24 MHz Crystal

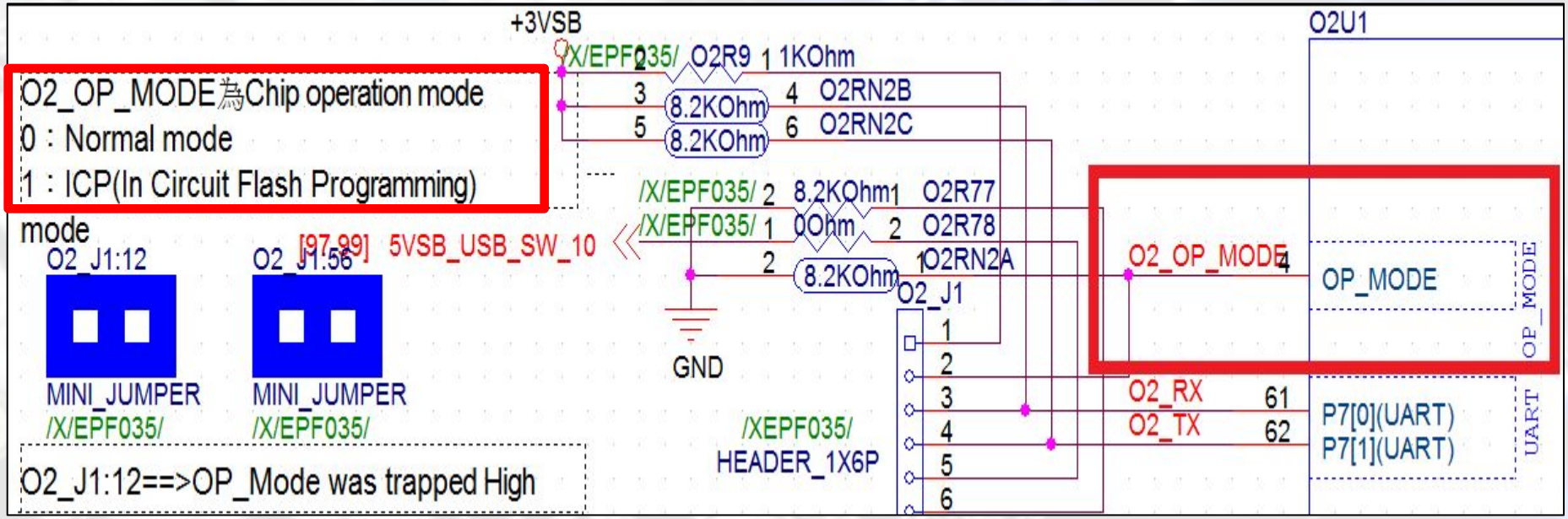




EC - Can’t Boot Status - 2

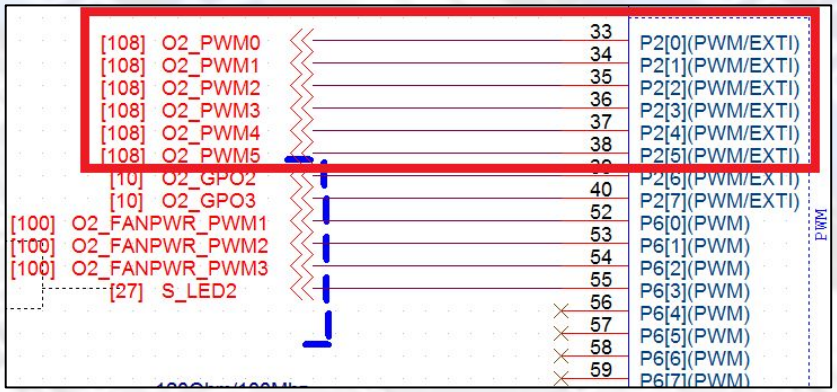
- **O2_OP_mode:**

This PIN is used for RD & factory to update EC firmware or flash programming.
Normal should always keep low.

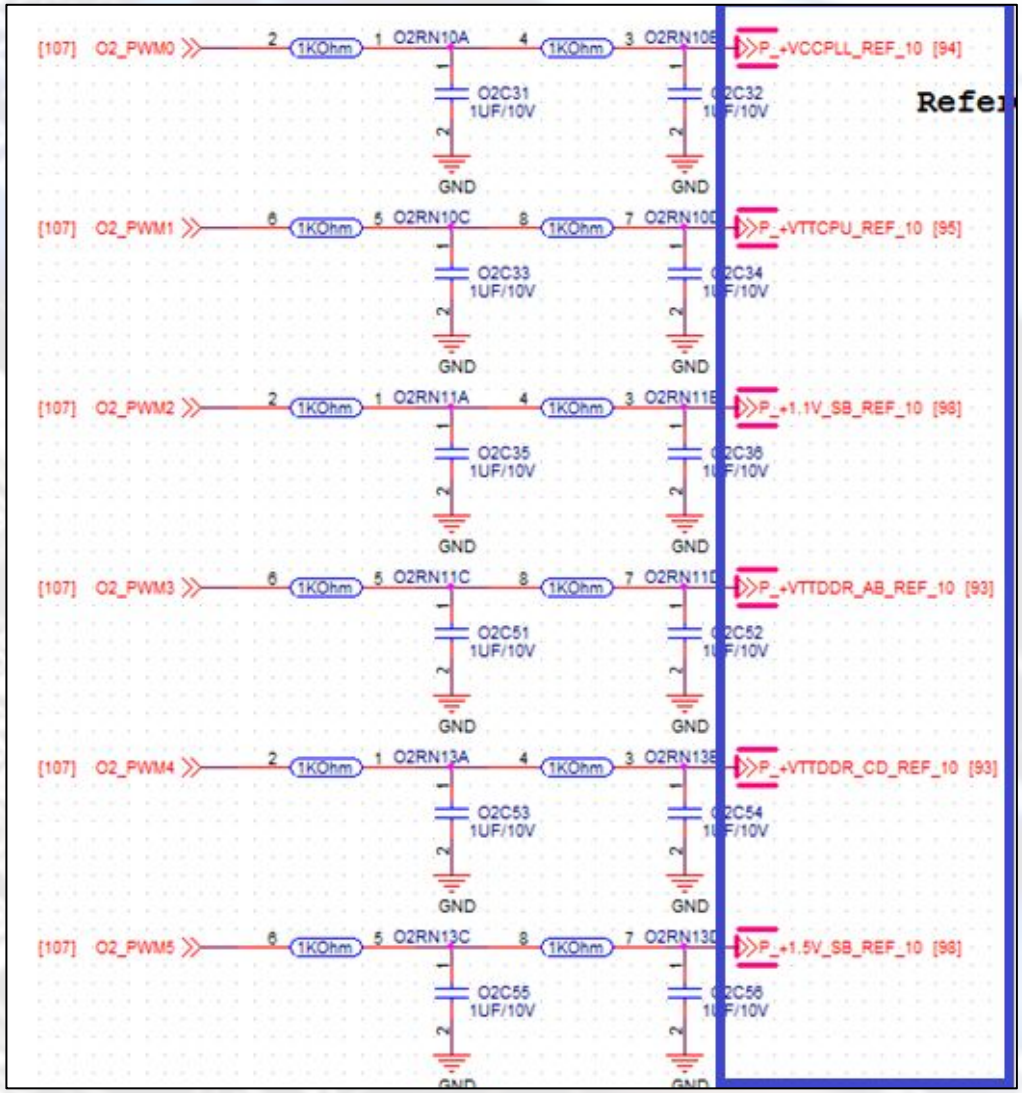


EC - Can’t Boot Status - 3

- **O2_PWM0~5:**



Input Voltage Reference	Output Voltage
P_+VCCPLL_REF_10	+VCCPLL
P_+VTTCPU_REF_10	+VTTCPU
P_+1.1V_SB_REF_10	+1.1V_SB
P_+VTTDDR_AB_REF_10	+VTTDDR_AB
P_+VTTDDR_CD_REF_10	+VTTDDR_CD
P_+1.5V_SB_REF_10	+1.5V_SB



EC - Can’t Boot Status - 4

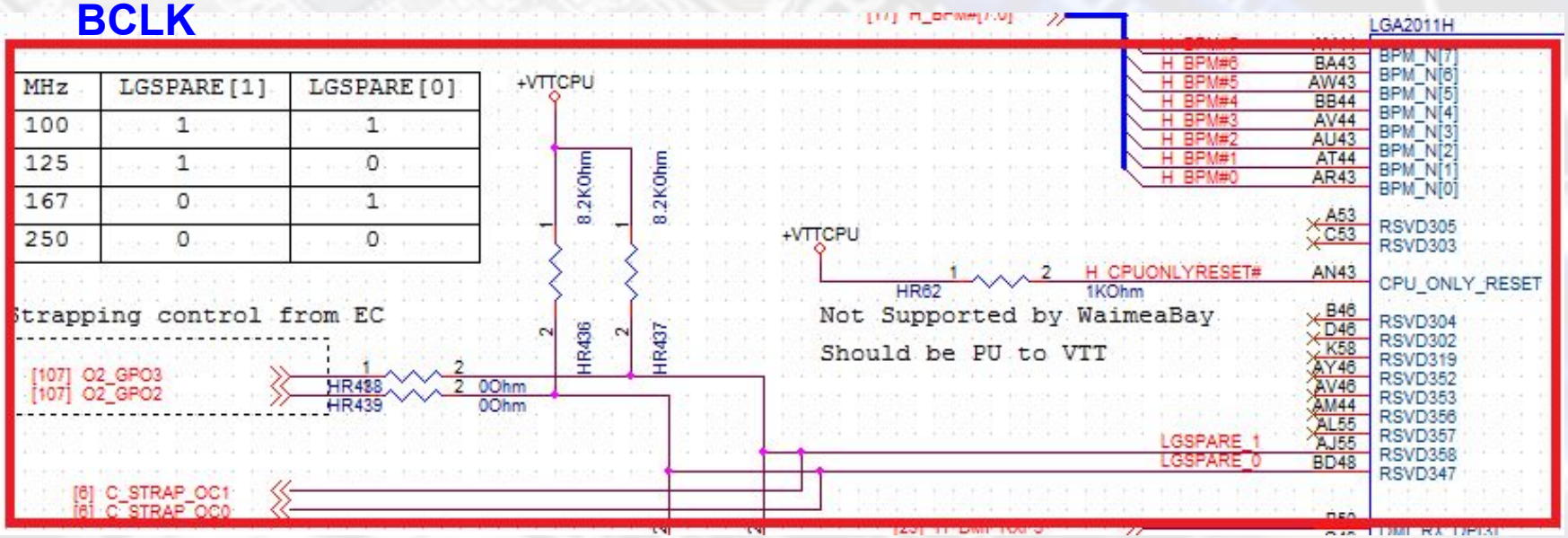
- **O2_GPO2~3:**

Load default -> check status : (1，1)

X79 series models use these two pins to control BLK frequency

BCLK

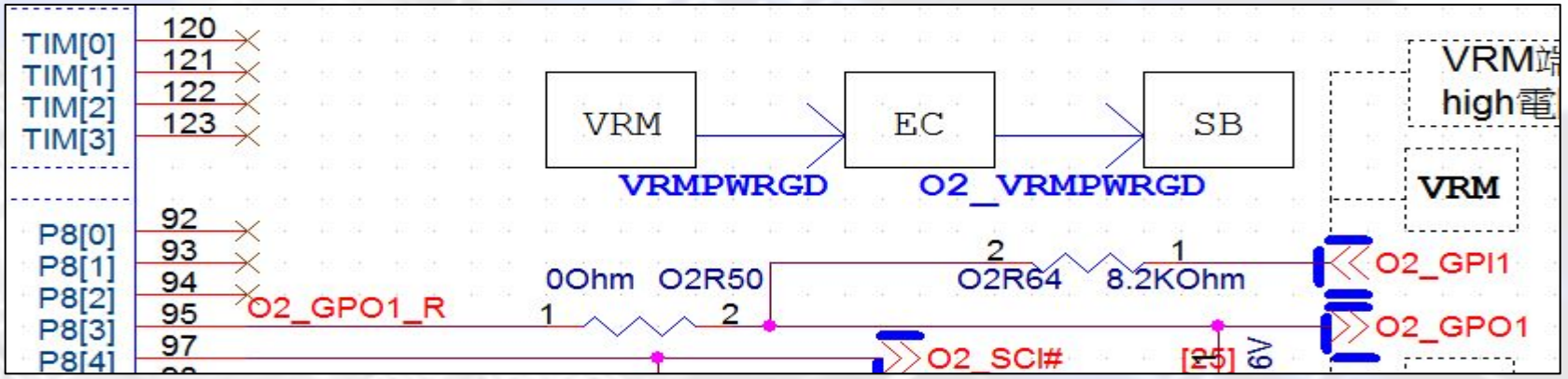
MHz	LGSPARE[1]	LGSPARE[0]
100	1	1
125	1	0
167	0	1
250	0	0



EC - Can’t Boot Status - 5

- **O2_GPI1 & O2_GPO1:**

  Correct: O2_GPI1:**H** & O2_GPO1:**H**



- **J_SILENT#(PROCHOT#):**

  If this pin of X79 series model is pulled low at S5, it can’t boot up.

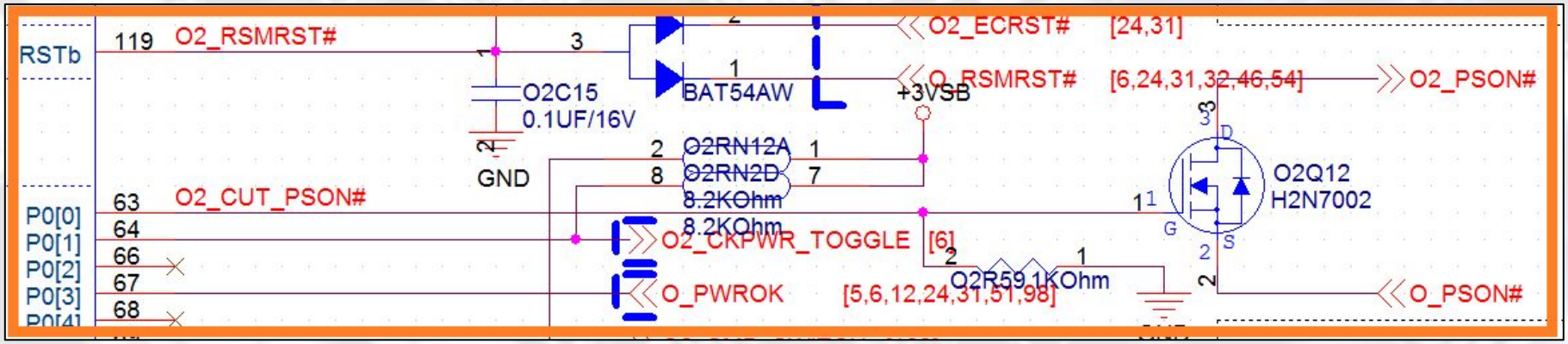
EC - Can’t Boot Status - 6

- **O_PWRBTN#IN_R& O_RSTCON#: Can’t Keep Low**

- **O2_CUT_PSON#: To keep PWRBTN motion**

  AC Power On -> PWM signal ready -> O2_CUT_PSON#: **H**

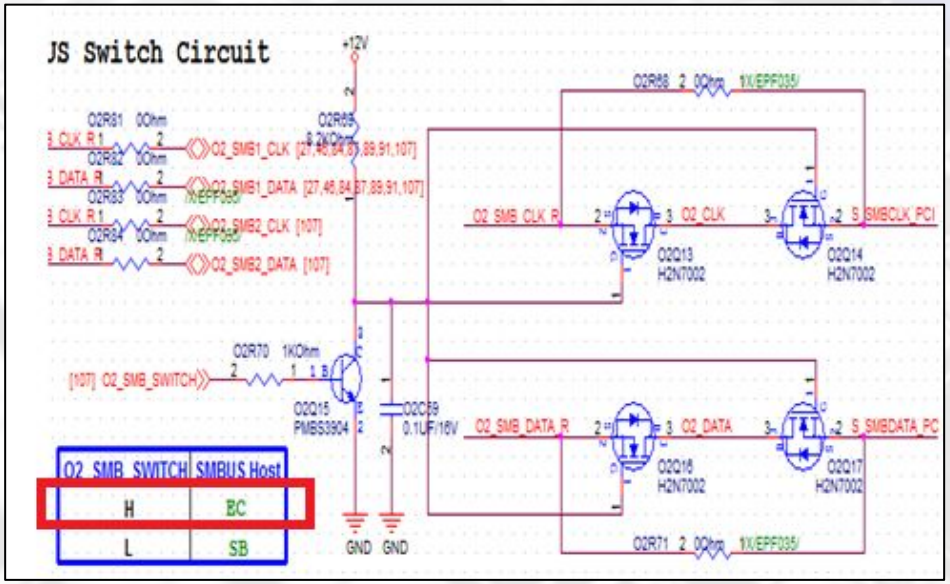
  When starting to USB BIOS flashback, this pin is also low.

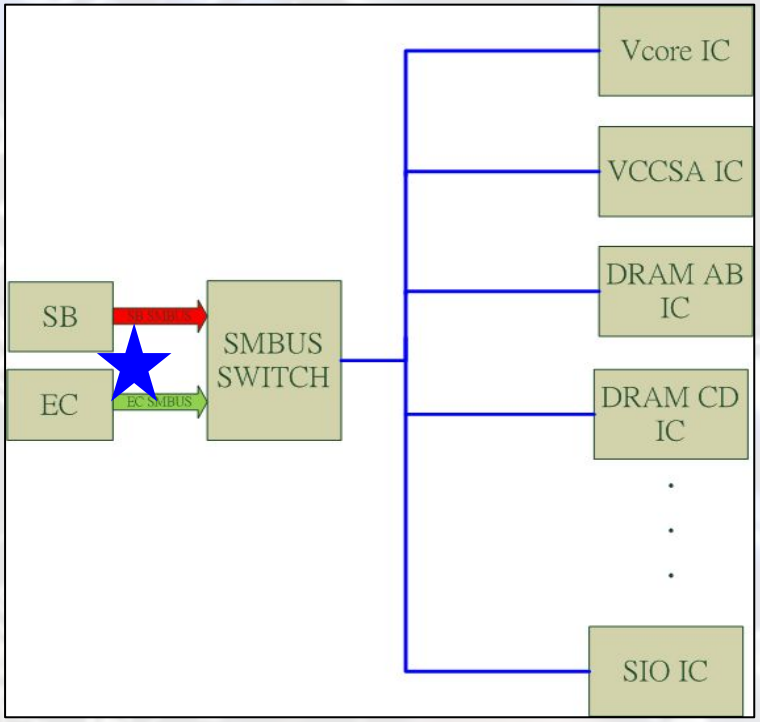


EC - Hang 0d0c Status

- **SMBUS & O2_SMB_SWITCH:**

Hang"**0d0c**" : EC check internal register setting of each DIGI+ Power Control.





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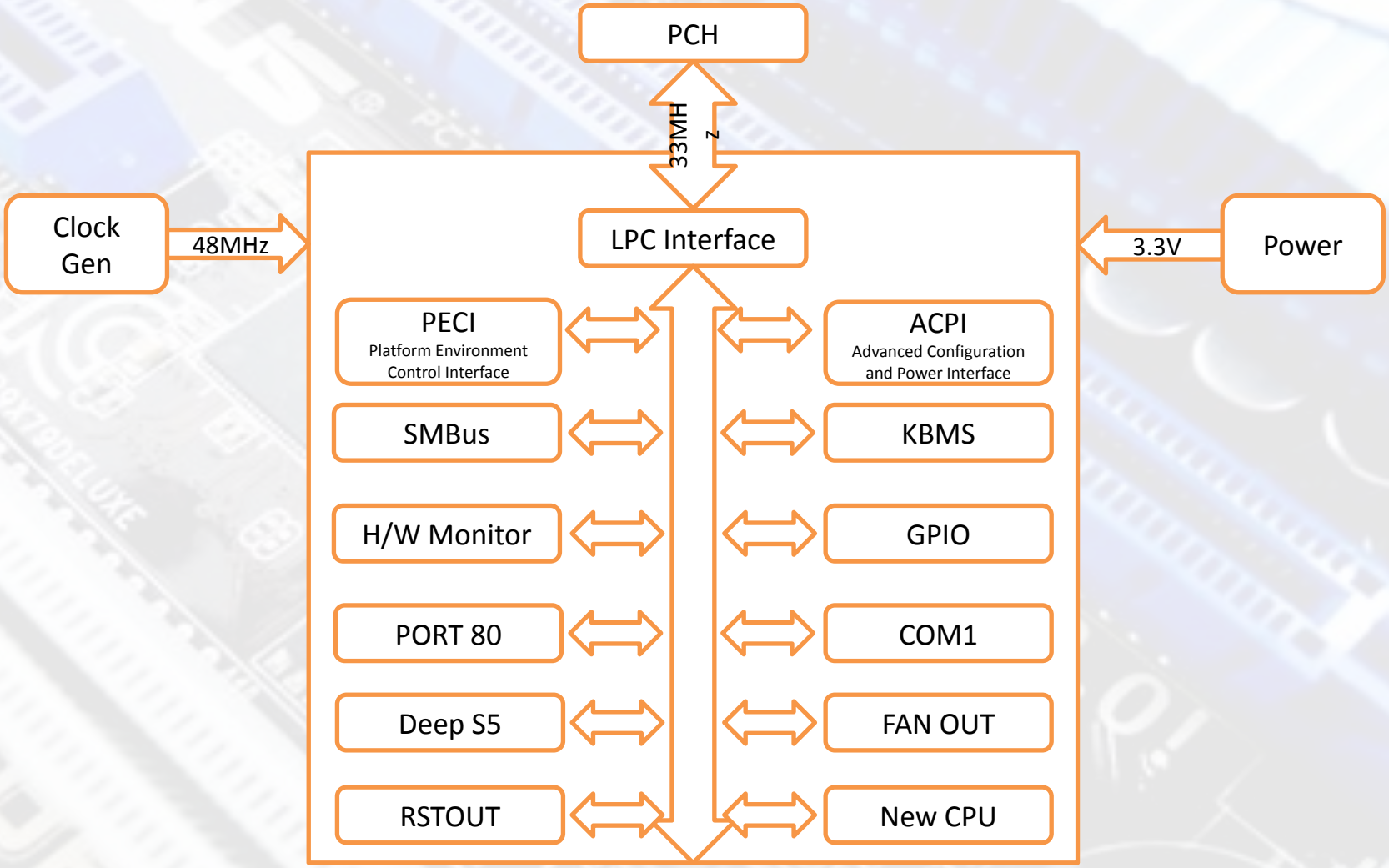
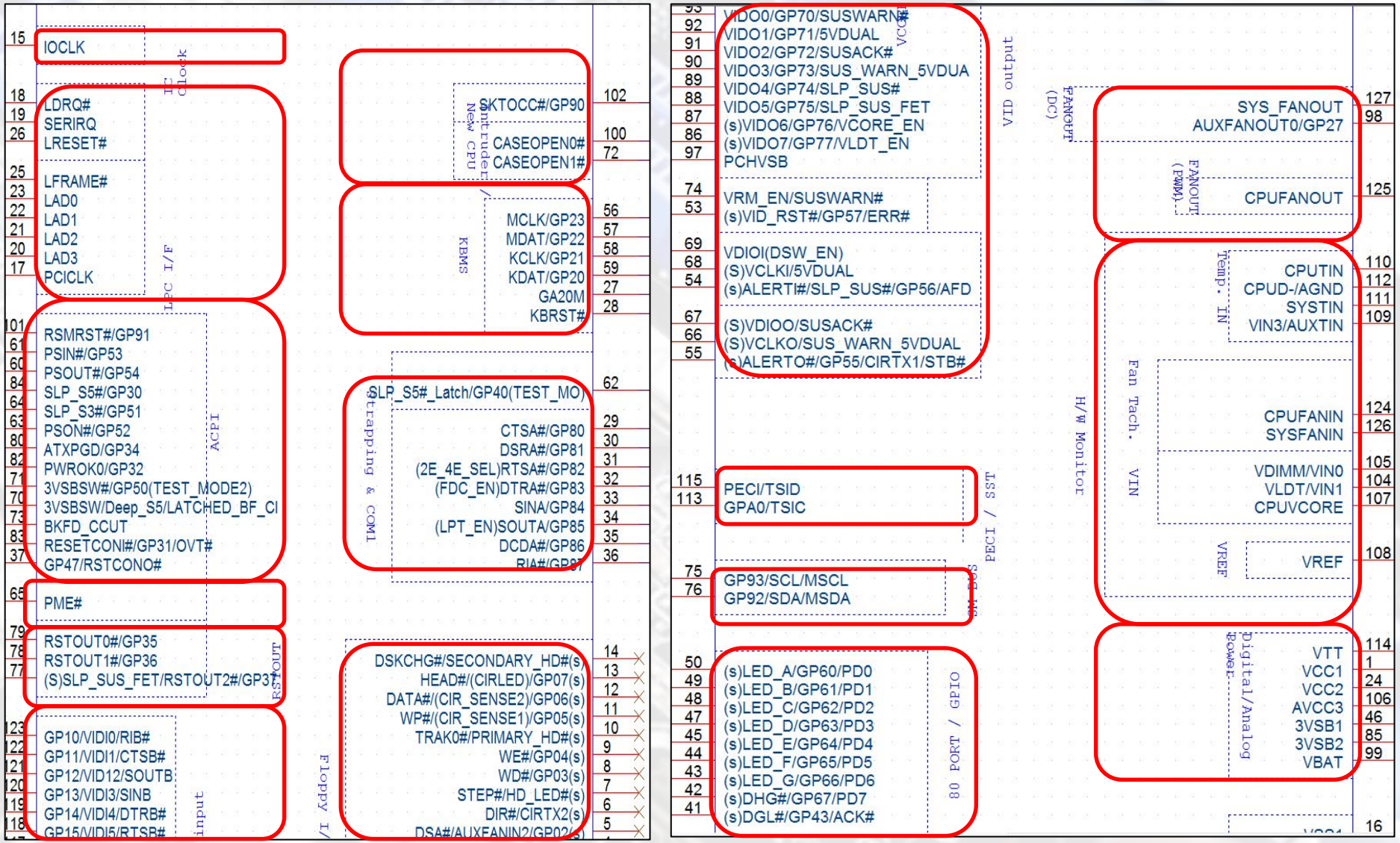
P9X79 SIO(6776F) – FEATURES

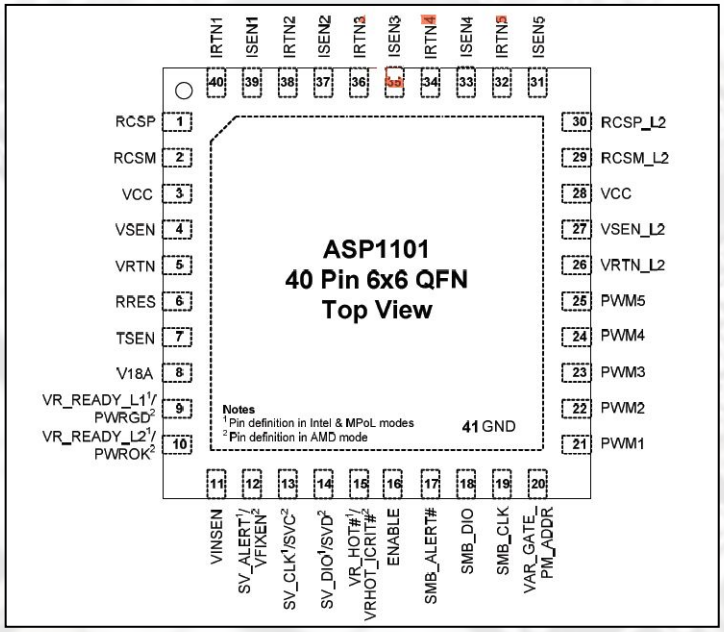


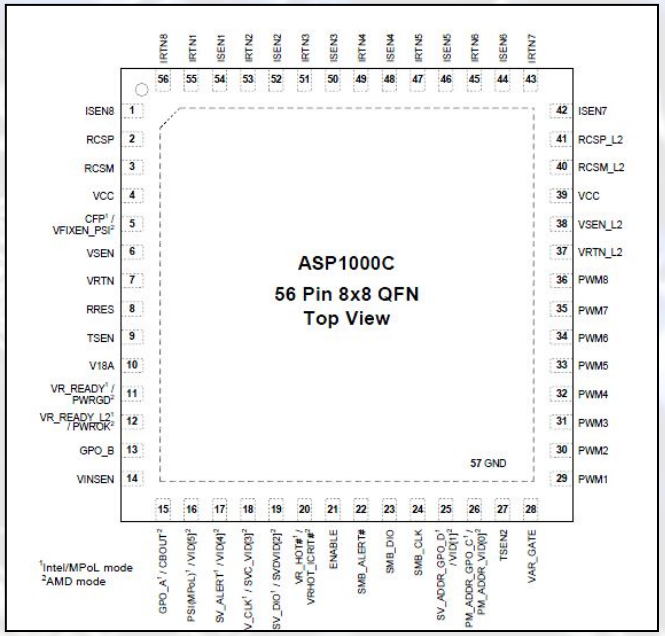
P9X79 SIO(6776F) Pin Description



DIGI VRM IC Introduction

- ASP1000 and ASP1101 are all DIGI power controller, all BIOS setting function can transmit signals through SMBUS to change or adjust IC internal value and in order to get all DIGI VRM function.





DIGI VRM IC Introduction - VCORE

- Vcc=3.3V
- Vinsen = 0.86V
- VRHot = Vcc
- EN=3.3V

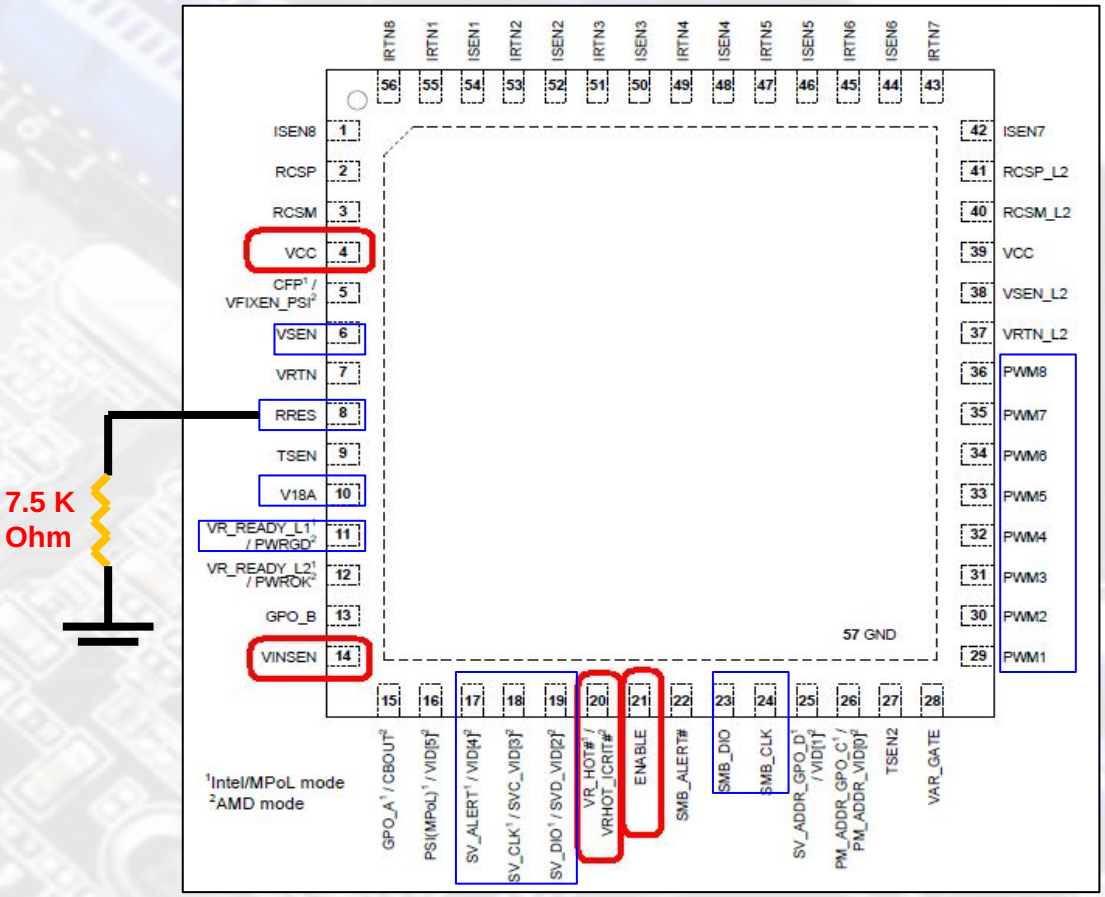
The Sequence:

VCC->Vinsen->VRHot->EN

Others Signals:

1. VSEN (FB+)
2. RRES
3. V18A
4. VR_READY
5. PIN17~19
6. SMBus
7. PWM signal

ASP1000



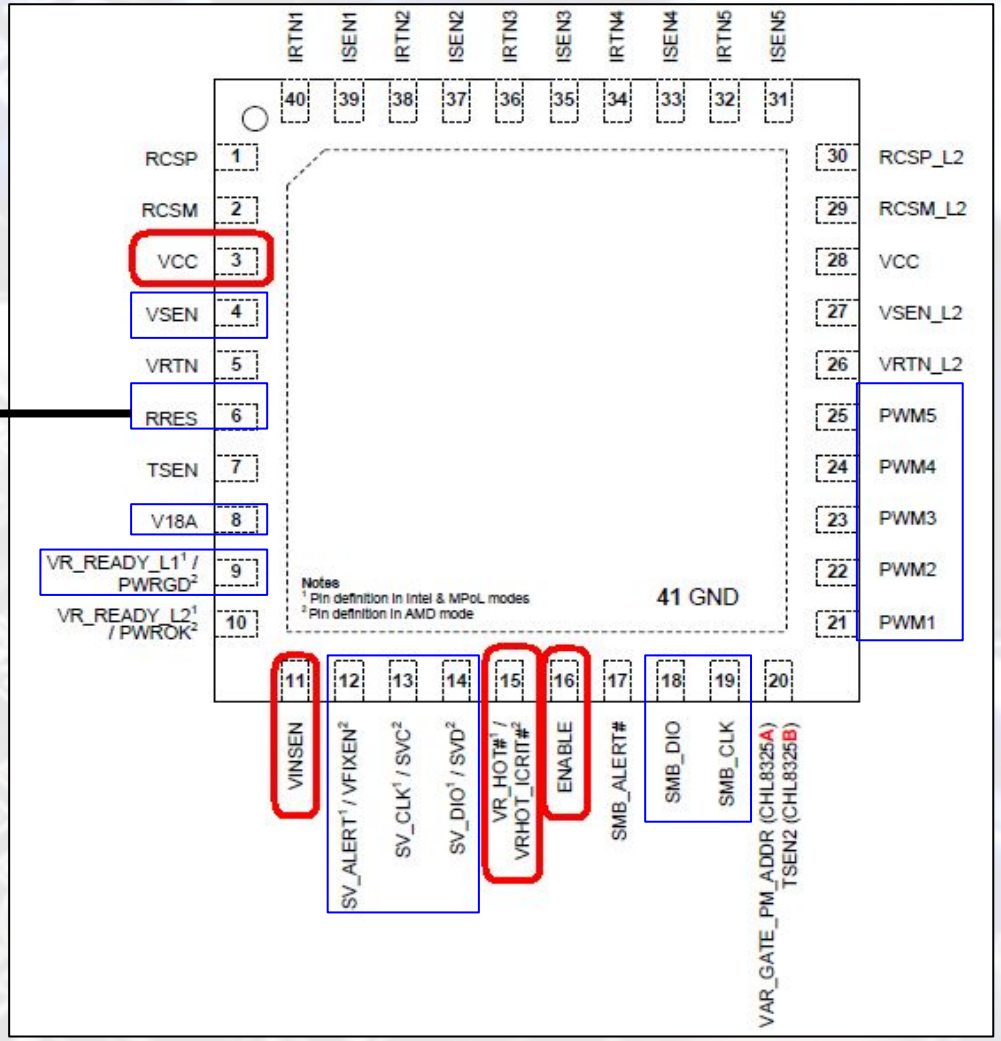
DIGI VRM IC Introduction - Vccsa

- Vcc=3.3V
- Vinsen = 0.86V
- VRHot = Vcc
- EN=3.3V

The Sequence:

VCC->Vinsen->VRHot->EN

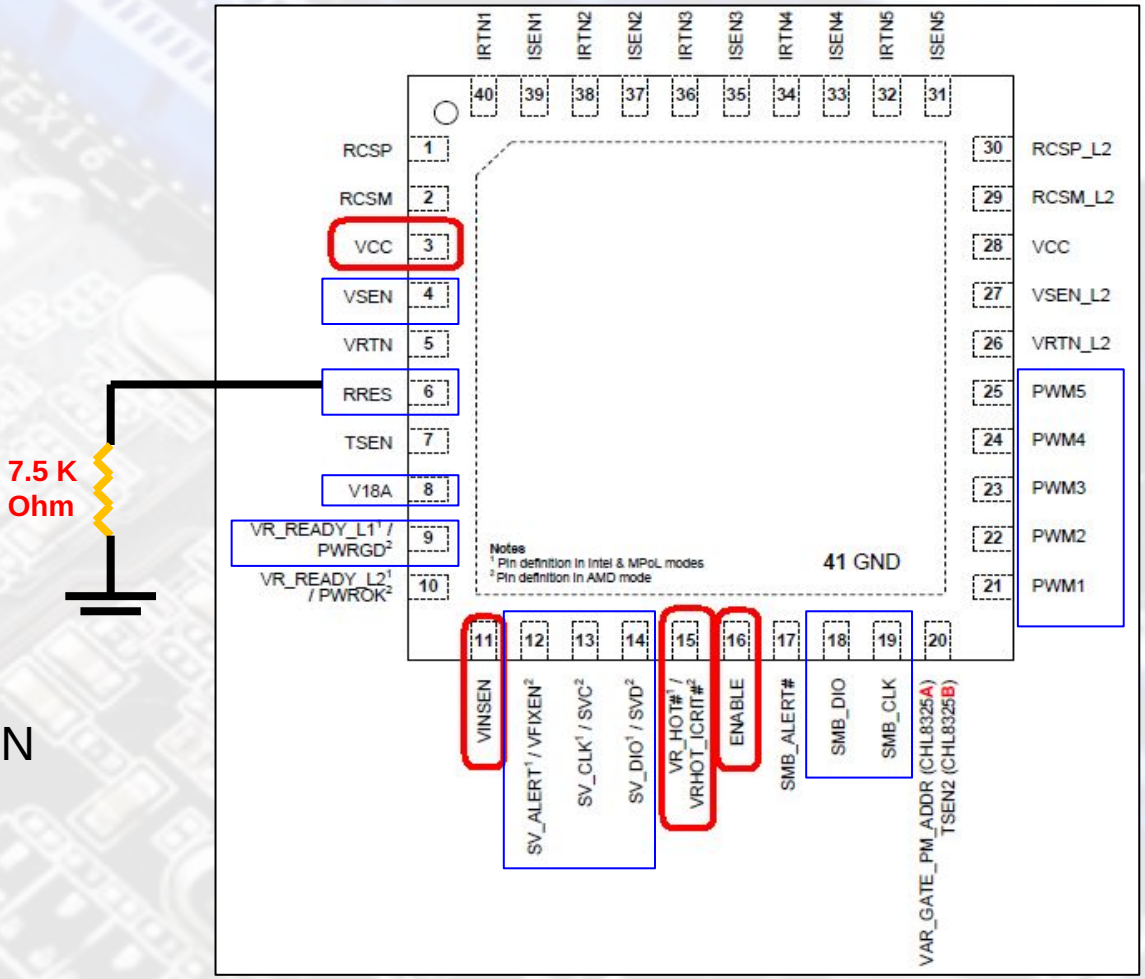
ASP1101



DIGI VRM IC Introduction – 1.5VDUAL

- Vcc=3.3V
- Vinsen = 0.38V
- VRHot = 3VSB
- EN=1V

ASP1101



The Sequence:

VCC->Vinsen->VRHot->EN

Repairing For NO VCORE

When the debug card shows 00, the CPU or sequence can't run completely.

(1) Visually inspect: (wrong parts, components missing …)

(2) Measure the impedance (component solder on the board)

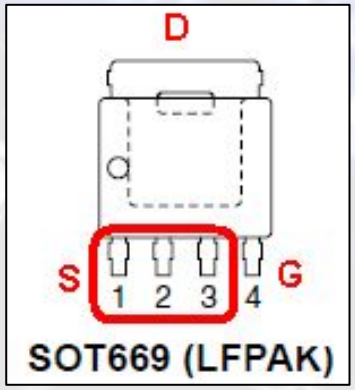
A. The impedance of each power circuit is short with GND or not.

B. Each MOS, the impedance of the H-S or L-S MOS GS side is K level,

C. the impedance of DS side can't be zero

D. Compare the difference with a golden compare .

(3) Power on and check each voltage



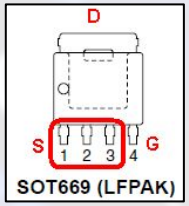
How To Identify MOS Is Normal

Step 1:

Multi-meter in Ω level : “+” side connects with Source, “-” side connects with Gate. Let MOSFET going into the cut-off state.

Step 2:

Multi-meter in diode level : “+” side connects with Source, “-” side connects with drain, measure Vf: 0.3V ~ 0.6V



Step 3:

Multi-meter in resistance level :

“+” side connects with drain, “-” side connects with source Value: xM Ω, ~ ∞ Ω,

“+” side connects with drain, “-” side connects with gate Value: xM Ω, ~ ∞ Ω

“+” side connects with source, “-” side connects with gate Value: xM Ω, ~ ∞ Ω

Step 4:

Multi-meter in resistance level :

“+” side connects with gate, “-” side connects with source ,to turn on MOSFET

“+” side connects with drain, “-” side connects with source Value: 0Ω ~~ 10 Ω

P9X79 – Agenda

- Intel X79 Platform Structure
- P9X79 Series Architecture
- New Feature
- Difference With P8 Series
- Clock Distribution
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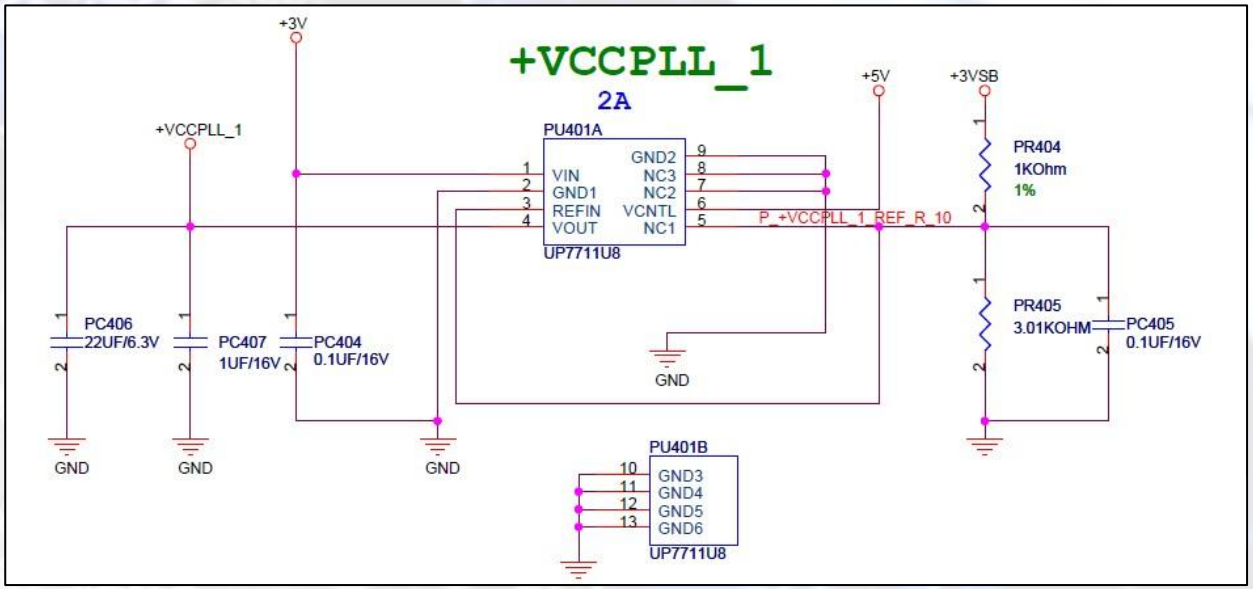
- Embedded Controller Introducing
- SIO and Other Power Chipset Introducing
- **Power theory and working condition**
- Communication BUS Introducing

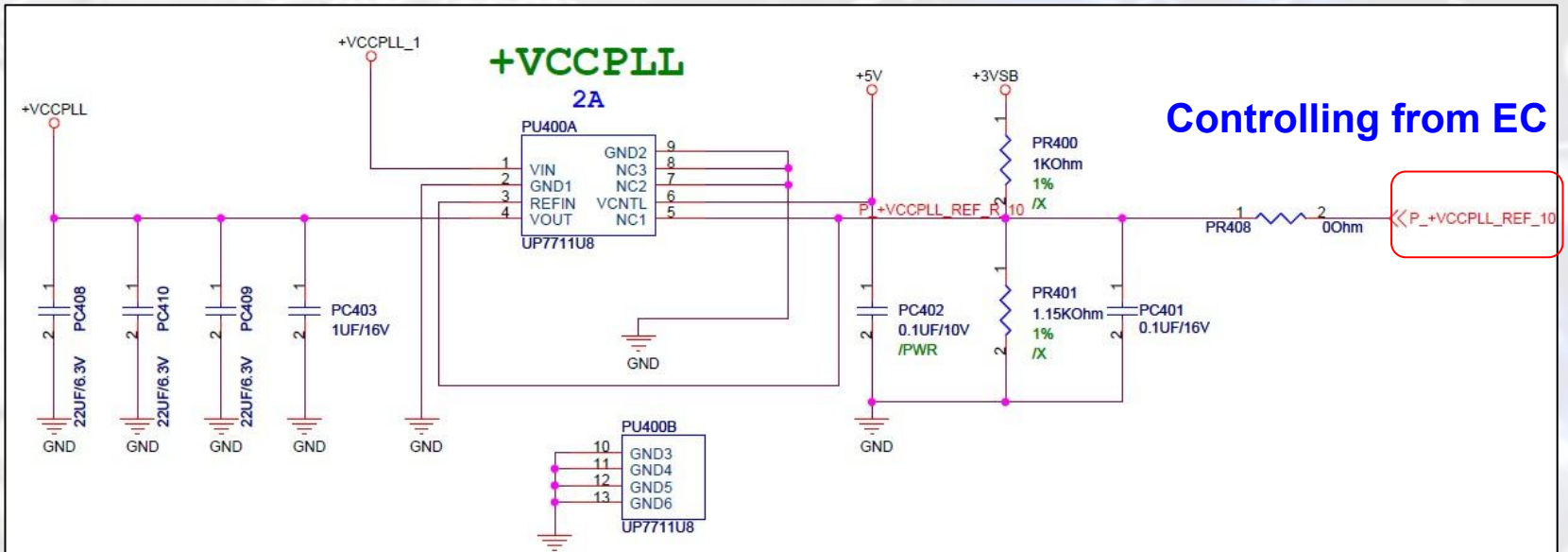
Power of VCCPLL

◆**Power:**

1. 3V
2. +VCCPLL_1
3. +VCCPLL

1. VIN
2. Control PIN
3. REF
4. VOUT

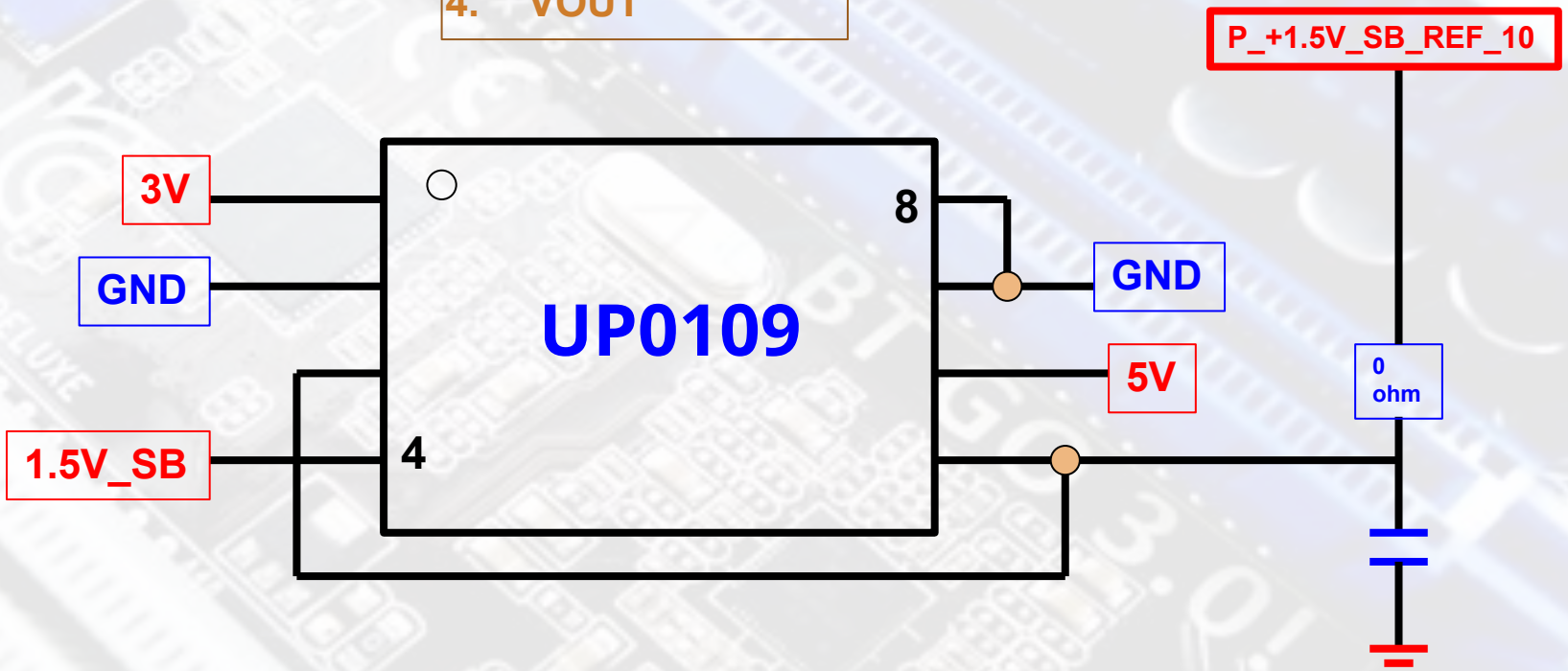




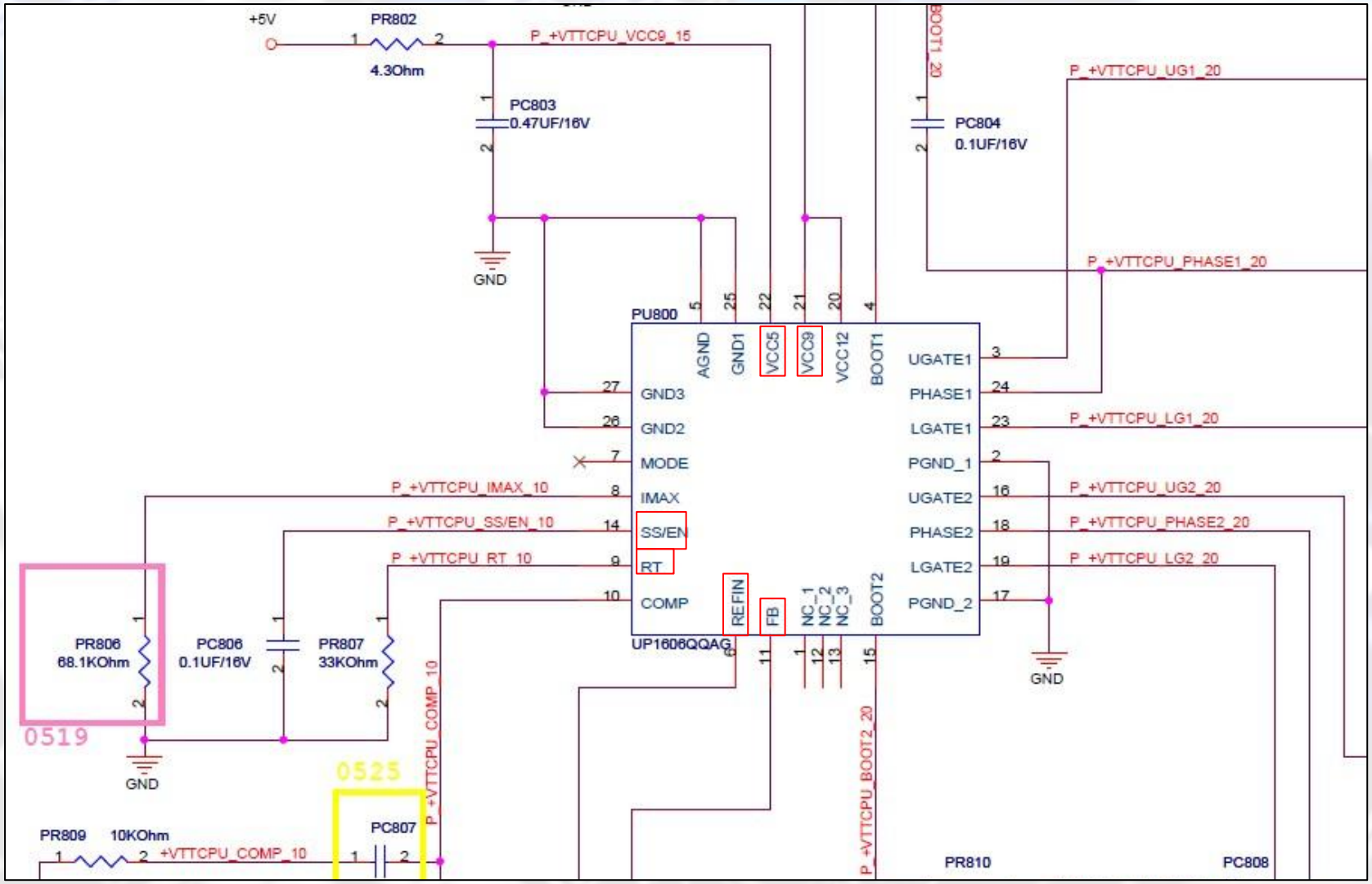
Power of 1.5V_SB

◆Power:
3V => +1.5V_SB

1. VIN
2. Control PIN
3. REF
4. VOUT



Power of VTTCPU eCircuit



Power of VTTCPU – Block Diagram

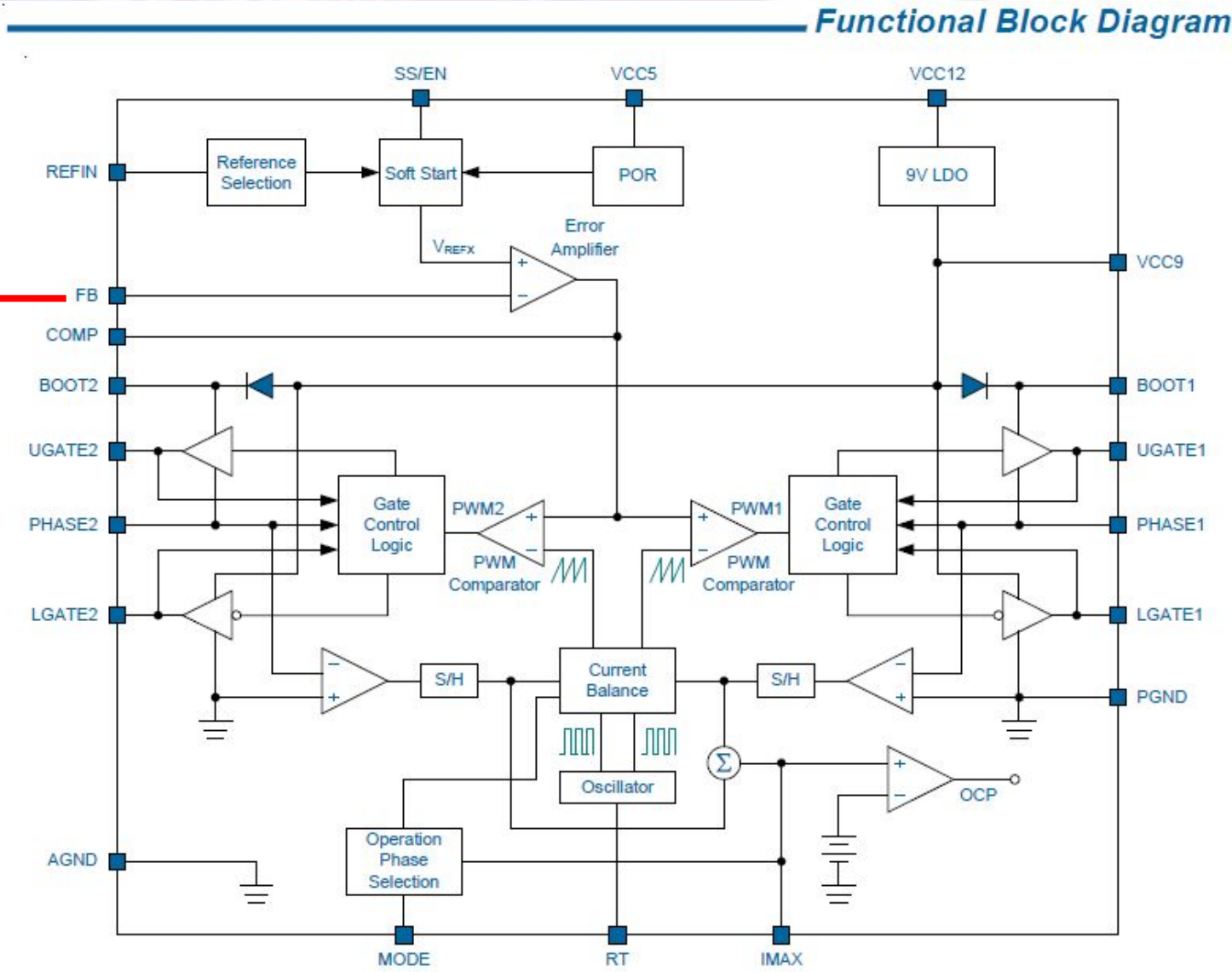
◆**Power:**
12V=>+VTTCPU

P_+VTTCPU_FB_R1_10

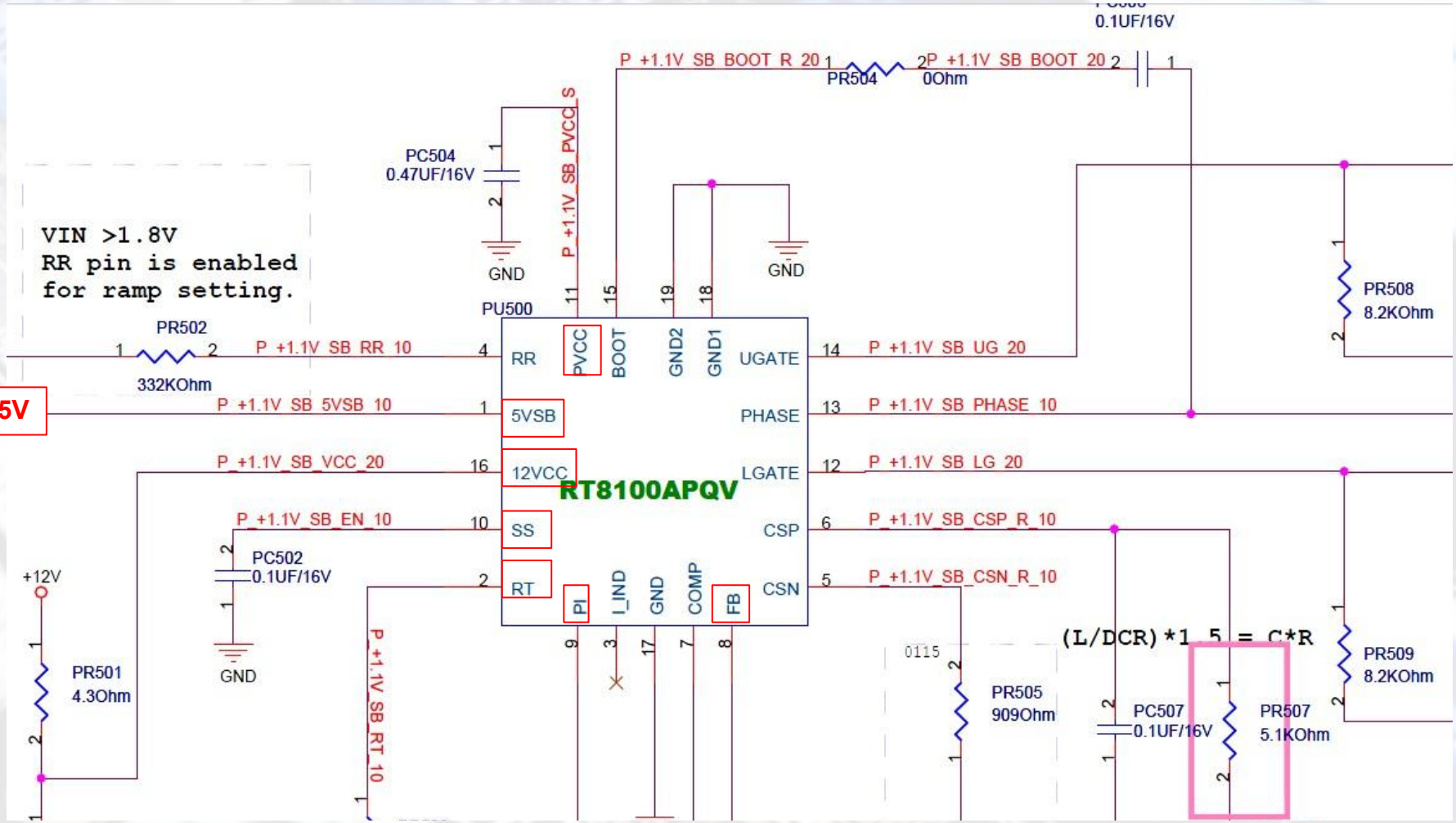
PR217

O_+VTTCPU_OV#

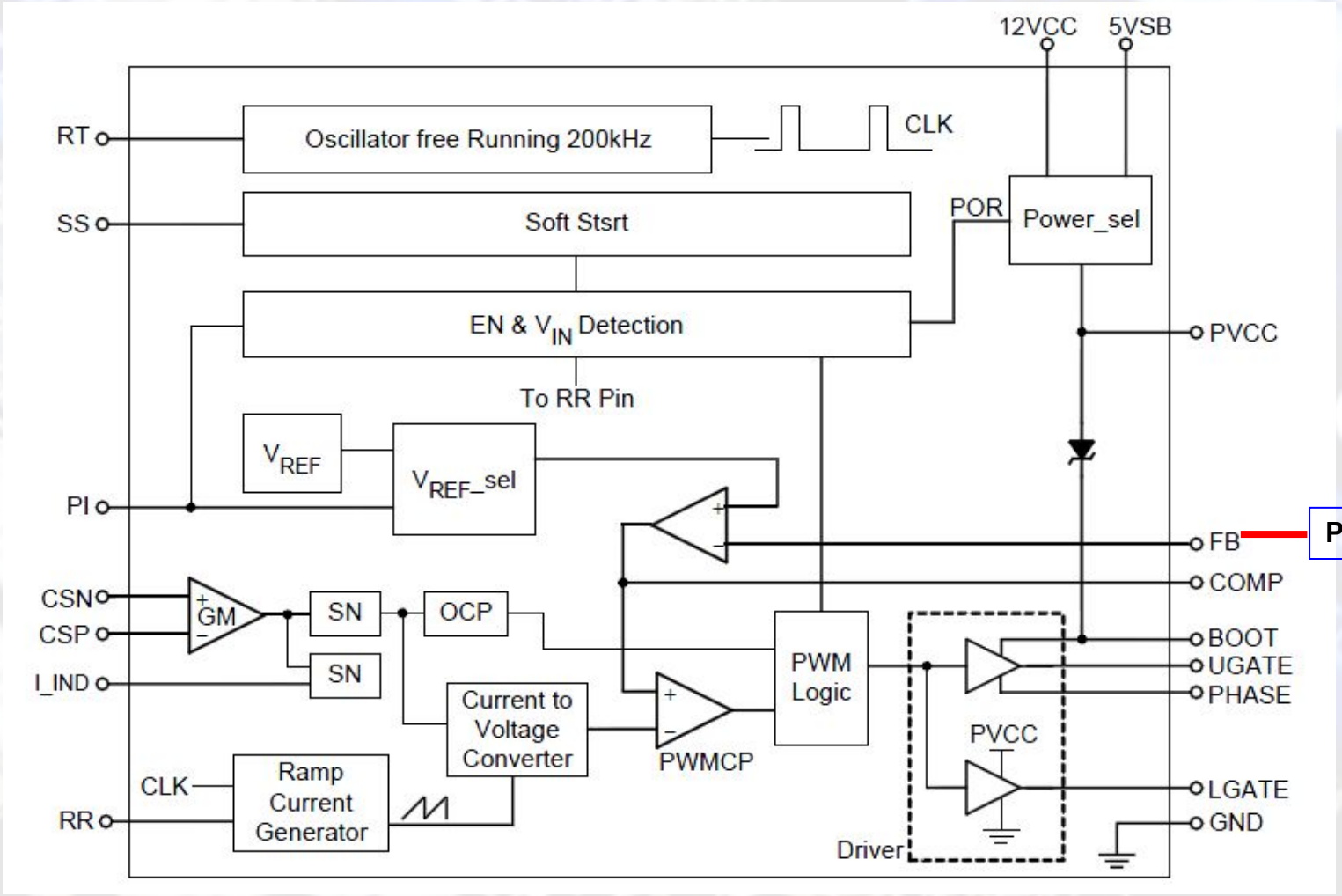
SIO



Power of 1.1V_SB eCircuit



Power of 1.1V_SB – Block Diagram



P_+1.1V_SB_FB_R1_10

PR527

O_+1.1V_SB_OV#

SIO

P9X79 – Agenda

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DMI

CPU

VCORE
VTTCPU
VSA_CPU
VCCPLL
1.5VDUAL_CD
1.5VDUAL_AB

C_CPU
C_CPU#
C_CPU_QPI
C_CPU_QPI#

H_CPUPWRGD
H_CPURST#

PCH

3V
3VSB
1.1V_SB
1.5V_SB
1.1V_SB_VCCDMIPLL

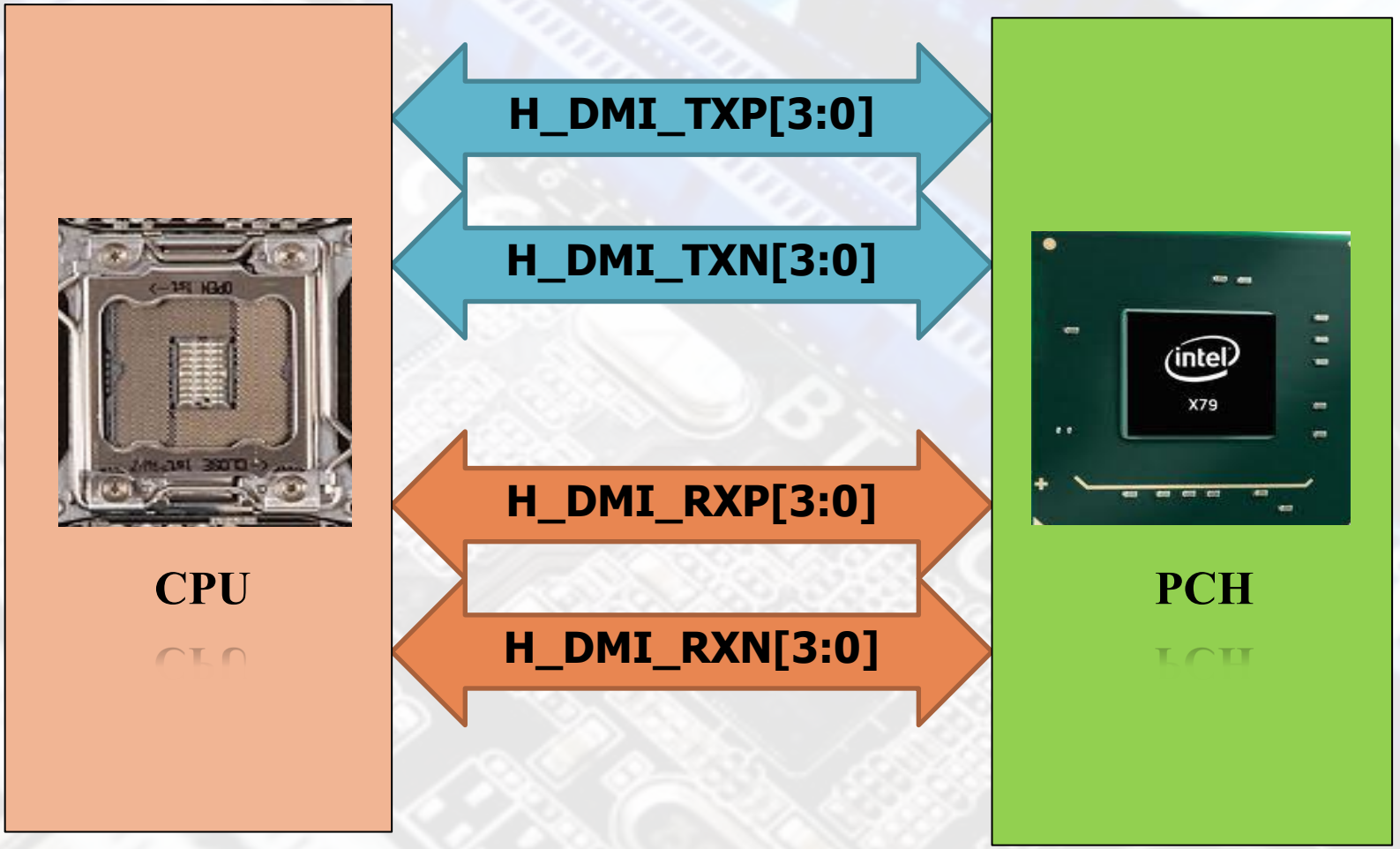
C_PCH_DMI
C_PCH_DMI#
32.768 Hz

O_PWROK
S_VRMPWRGD
S_PLTRST#

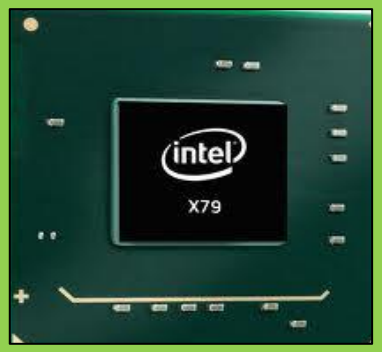
DMIRBIAS

DMI_ZCOMP

DMI


H_DMI_TXP[3:0]
H_DMI_TXN[3:0]
H_DMI_RXP[3:0]
H_DMI_RXN[3:0]
CPU
PCH
intel
X79

SPI



PCH

3V
3VSB
1.1V_SB
1.5V_SB

C_PCH_14M
32.768 Hz

O_PWROK
S_VRMPWRGD
S_PLTRST#

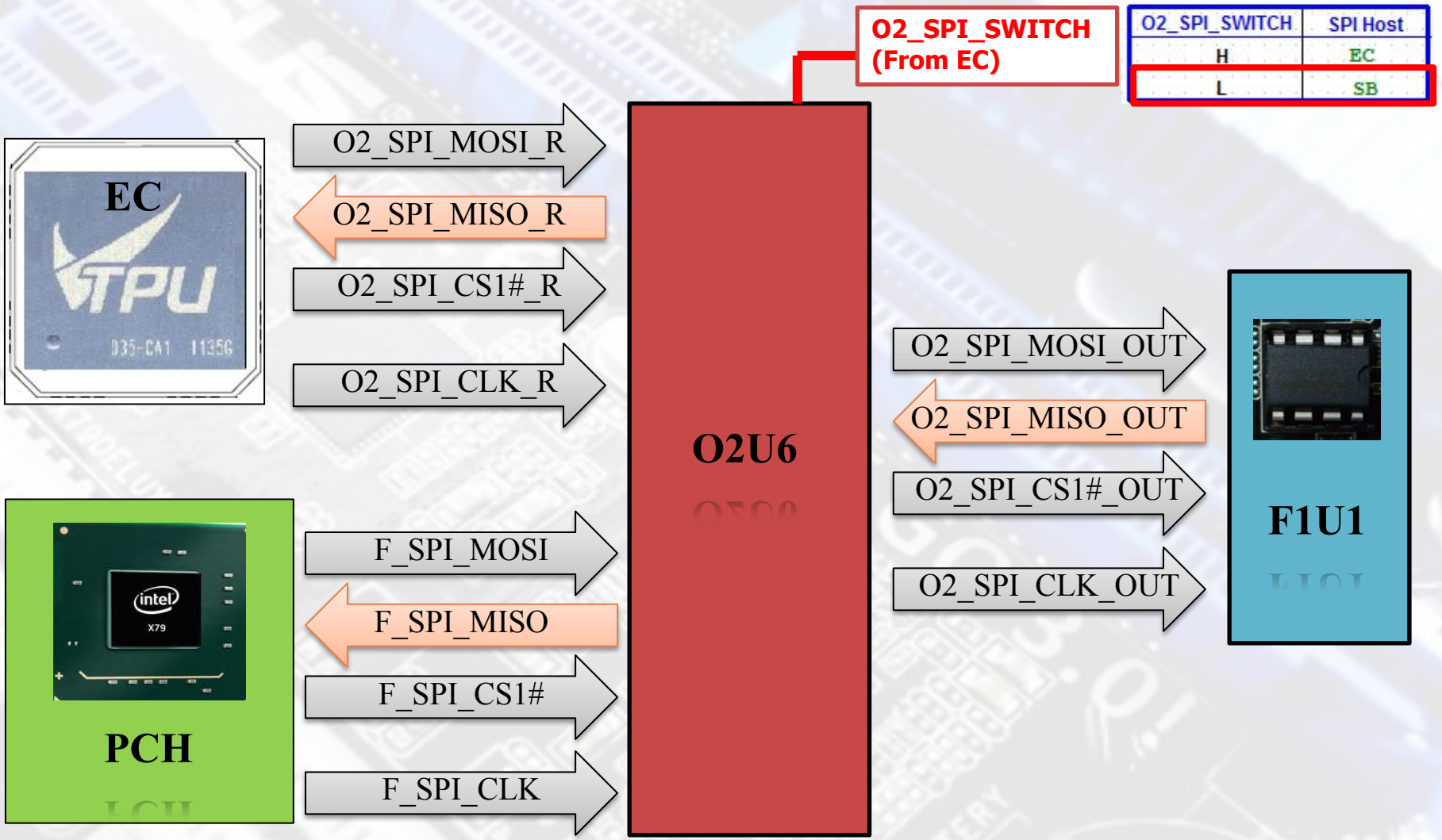
F1U1

3V_SPI (3VSB)
F1_SPI_HOLD#
O_BIOS_WP#

O2U6

5VSB
O2_SPI_SWITCH
(From EC)

SPI


O2_SPI_SWITCH
(From EC)
O2_SPI_SWITCH
SPI Host
H
EC
L
SB
EC
O2_SPI_MOSI_R
O2_SPI_MISO_R
O2_SPI_CS1#_R
O2_SPI_CLK_R
O2U6
O2_SPI_MOSI_OUT
O2_SPI_MISO_OUT
O2_SPI_CS1#_OUT
O2_SPI_CLK_OUT
F1U1
PCH
F_SPI_MOSI
F_SPI_MISO
F_SPI_CS1#
F_SPI_CLK

MEMORY

CPU

VCORE
VTTCPU
VSA_CPU
VCCPLL
1.5VDUAL_CD
1.5VDUAL_AB

H_DRAMVREFDQ_TX_CD
H_DRAMVREFDQ_TX_AB
H_DRAMVREFDQ_RX_CD
H_DRAMVREFDQ_RX_AB

H_DDR_CD_1V05_SDA
H_DDR_AB_1V05_SDA
H_DDR_CD_1V05_SCL
H_DDR_AB_1V05_SCL

H_DRAMPWROK_CD
H_DRAMPWROK_AB
D3_MEMHOT#_AB
D3_MEMHOT#_CD

MEMORY

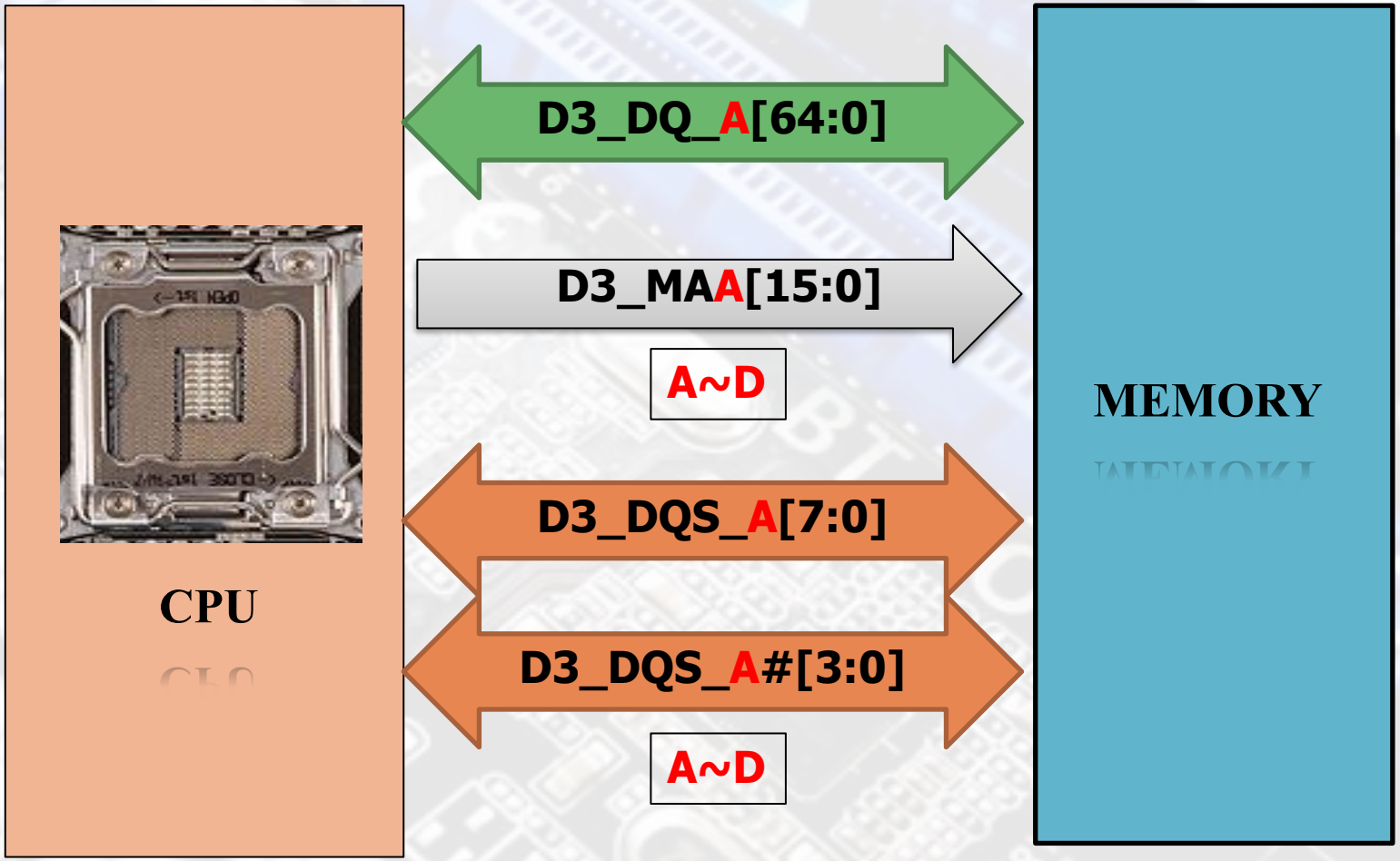
3V
1.5VDUAL_CD
1.5VDUAL_AB
+VTTDDR_AB
+VTTDDR_CD
D3_VREFDQ_A~D
D3_VREFCA_A~D

D3_M[A~D]_CLK[3:0]
D3_M[A~D]_CLK#[3:0]

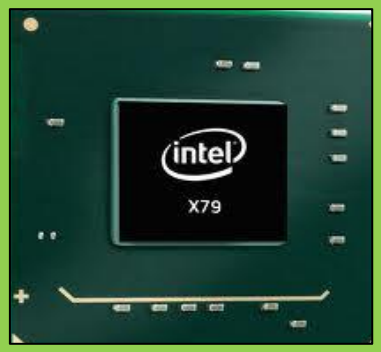
D3_RESET#AB
D3_RESET#CD

H_DDR_CD_3V3_SDA
H_DDR_AB_3V3_SCL
H_DDR_CD_3V3_SDA
H_DDR_AB_3V3_SCL

MEMORY



LPC



PCH

3V
3VSB
1.1V_SB
1.5V_SB

C_PCH_14M
C_PCI_PCH
32.768 Hz

O_PWROK
S_VRMPWRGD
S_PLTRST#

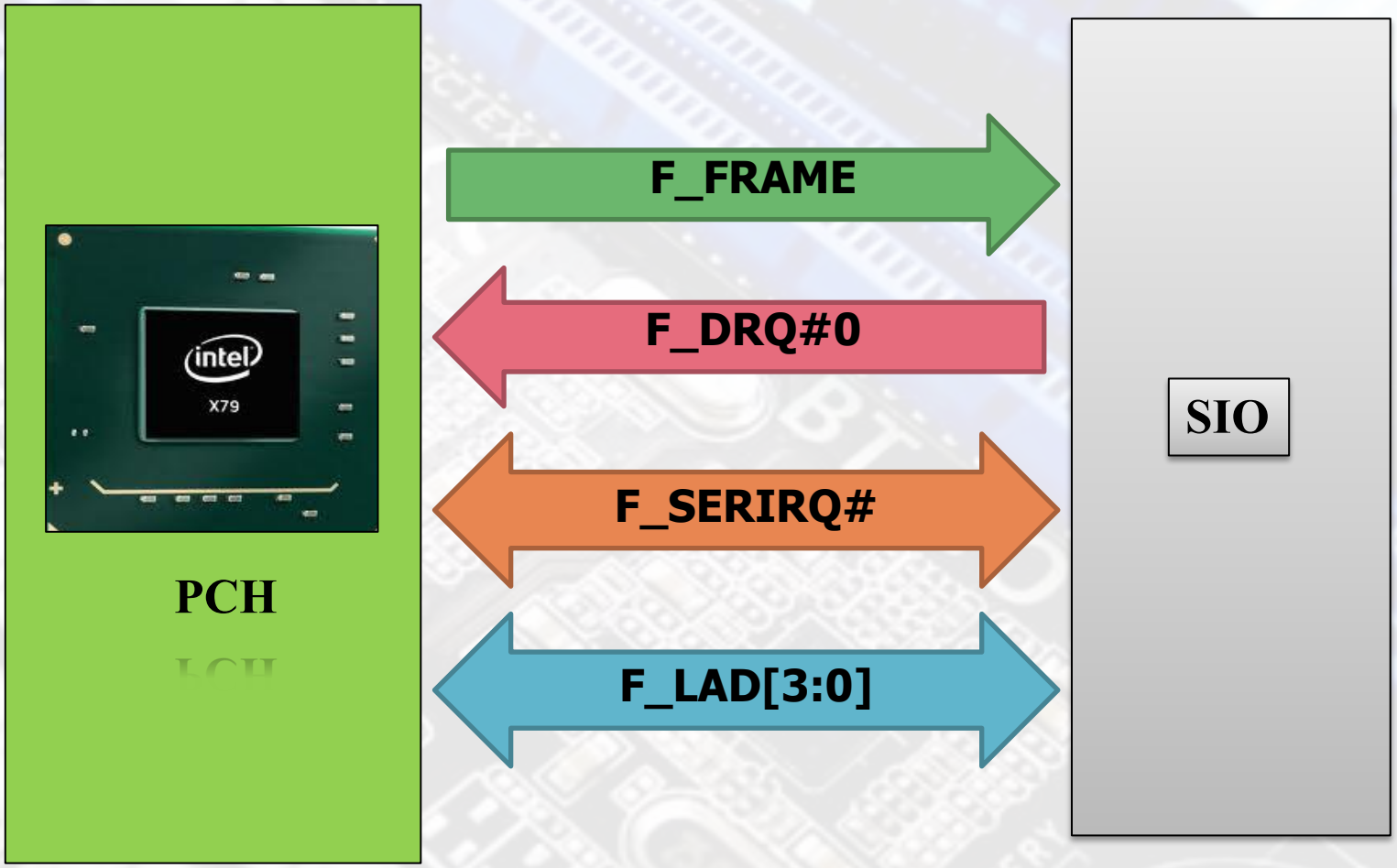
SIO

3V
3VSB_ATX
VTTCPU

C_48M_SIO
C_PCI_SIO

O_PWROK_SIO
S_PLTRST#

LPC



P9X79 Series – Q&A

~Q &A~

~THANK YOU~