

Мікропроцесорна техніка

(лекція 6)
Благітко Б.Я.
2019 р.

PSoC Creator 4.2
Designing with PSoC 3/5



Мікропроцесорн а техніка

ADC+LCD

PSoC Creator 4.2
Designing with PSoC 3/5



PSoC 3/5 включає в себе можливість обробки аналогових, цифрових і змішаних сигналів, а також можливість формування аналогових і цифрових сигналів, охоплюючи широкий спектр прикладних задач

- **Особливості PSoC 3/5:**
 - Реконфігуровувані Аналогові модулі:
 - Вбудовані АЦП і ЦАП, аналогові фільтри різних типів, підсилювачі аналогових сигналів, компаратори, аналогові модулятори і т. д.
 - Реконфігуровувані Цифрові модулі:
 - Вбудовані таймери, лічильники, PWM, UART, SPI, IrDA, I2C і т. д.
 - Flash від 4КВ до 32КВ для зберігання програми
 - SRAM от 256В до 2КВ для зберігання даних
 - Процесорне ядро - МК8051, CISC, 4MIPS

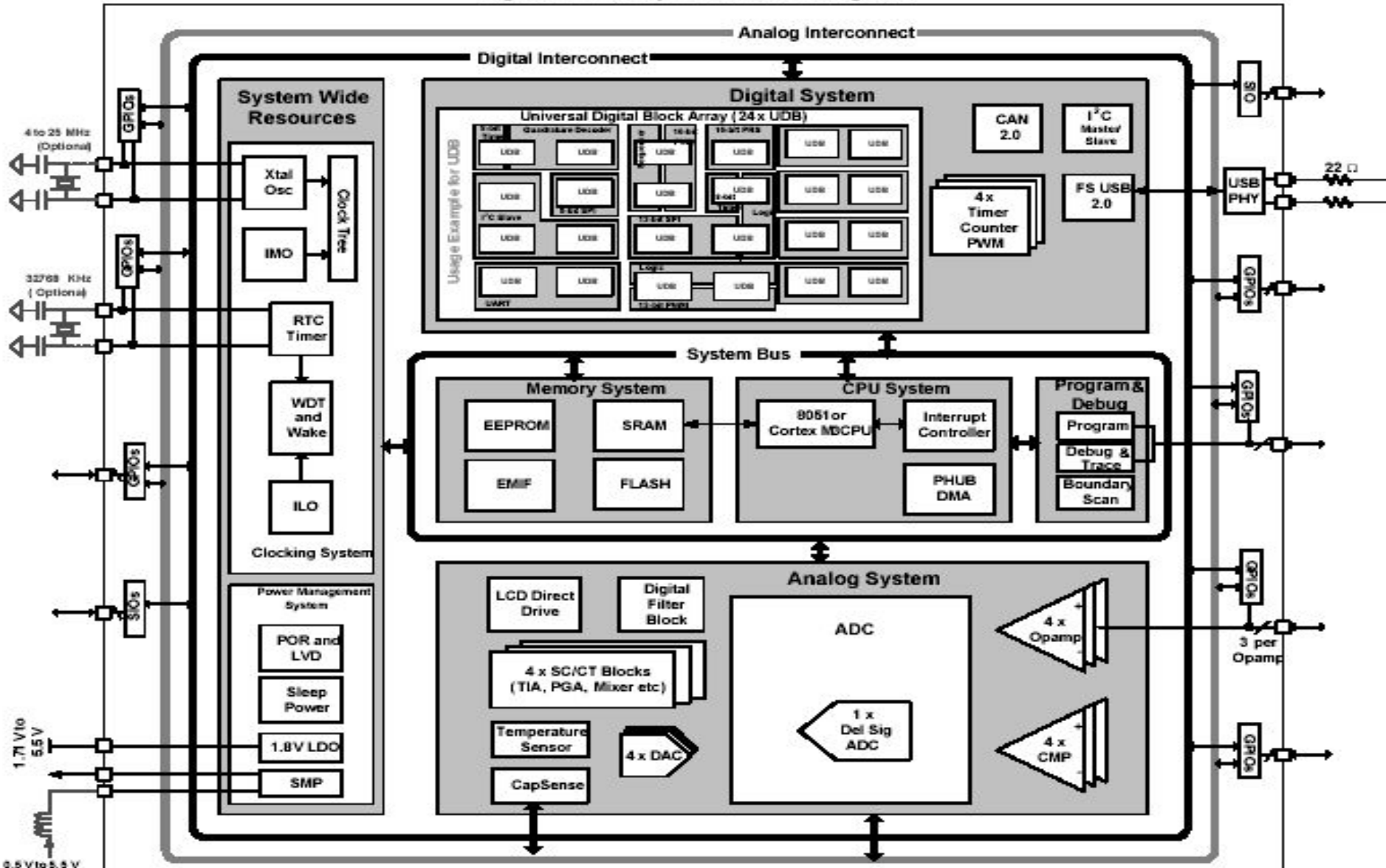
Оптимальними для PSoC являються задачі, коли необхідна обробка аналогових сигналів на апаратному рівні (підсилення, фільтрація, АМ/ФМ модуляція, демодуляція) із наступним перетворенням в цифрову форму в смузі аналогових сигналів до 100 кГц.

Виграш полягає в переносі зовнішніх дискретних компонентів у середину процесора.



Цифрові та аналогові модулі

Figure 1-1. Simplified Block Diagram



Принцип дії даного АЦП дещо більш складний, ніж у інших типів АЦП.

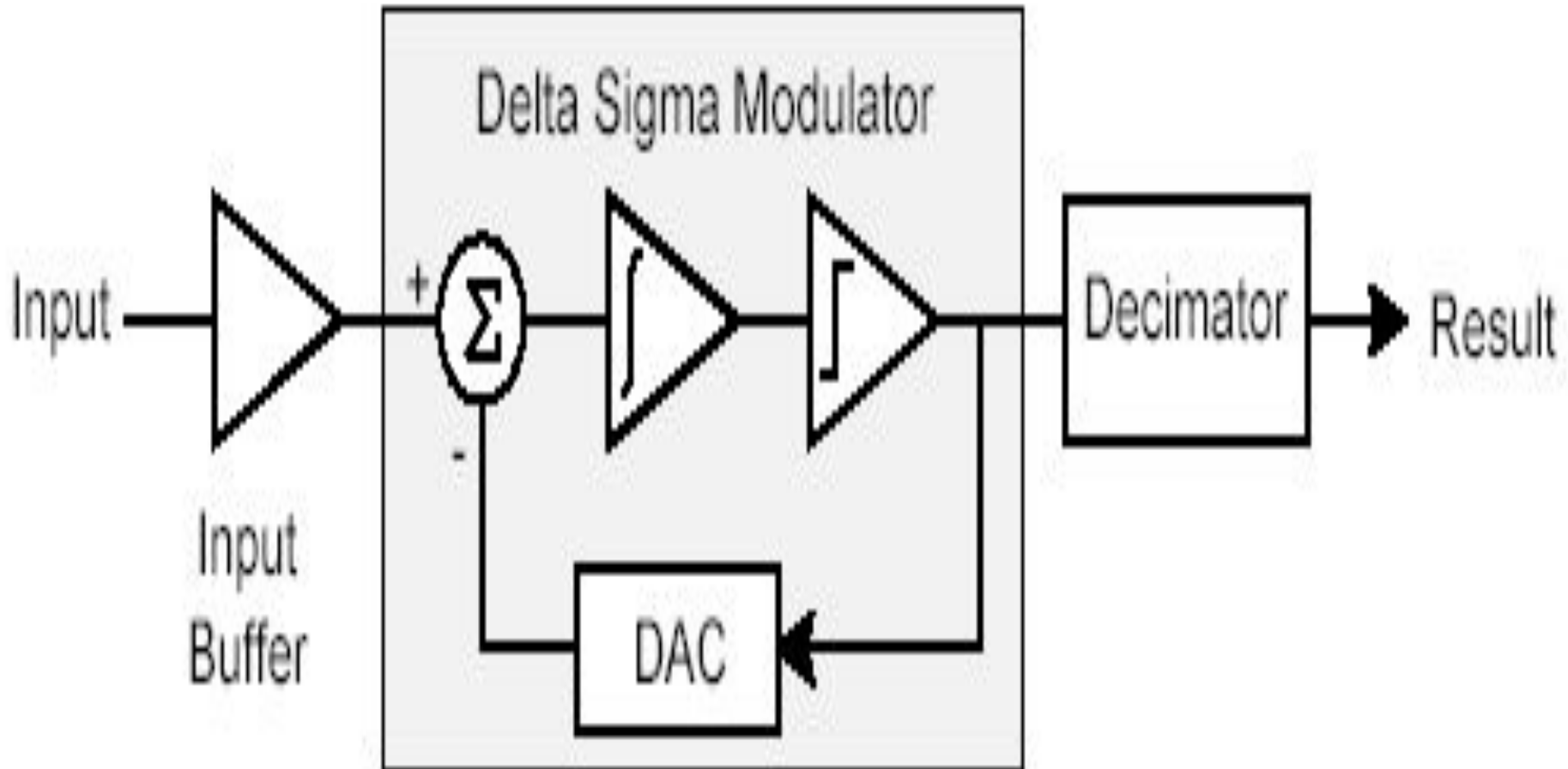
Його суть в тому, що вхідна напруга порівнюється зі значенням напруги, накопиченим інтегратором.

На вхід інтегратора подаються імпульси позитивної чи від'ємної полярності, в залежності від результату порівняння.

Таким чином, даний АЦП представляє собою просту слідкуючу систему: напруга на виході інтегратора «відслідковує» вхідну напругу (рис.).

Результатом роботи даної схеми являється потік нулів та одиниць на виході компаратора, який потім пропускається через цифровий ФНЧ, в результаті отримується N-бітний результат.

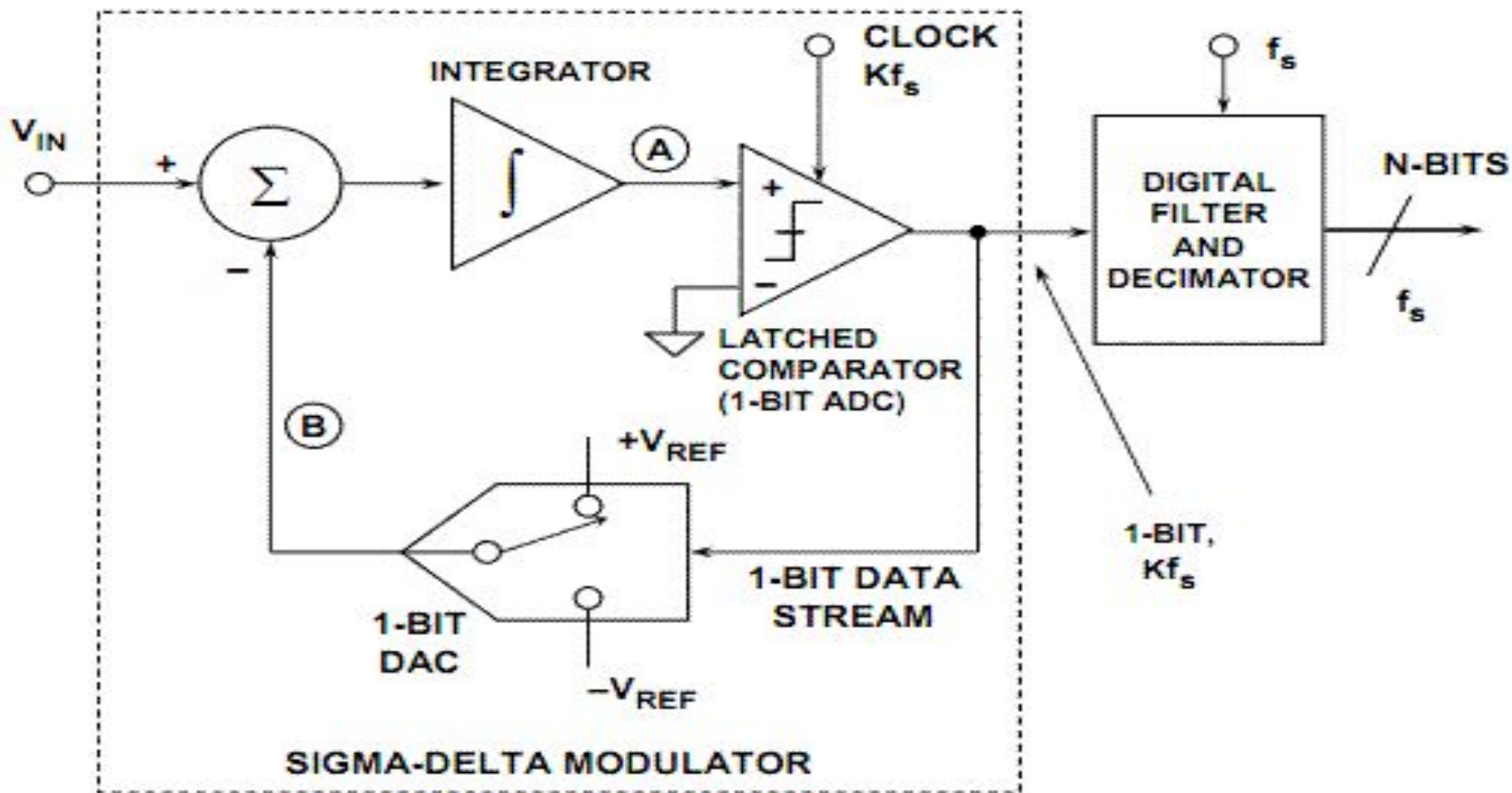
ФНЧ на рис. об'єднаний з «дециматором», пристроєм, який понижує частоту слідування відліків шляхом їх «проріджування».



ADC_DelSig Block Diagram



Delta Sigma Analog to Digital Converter (ADC_DelSig)

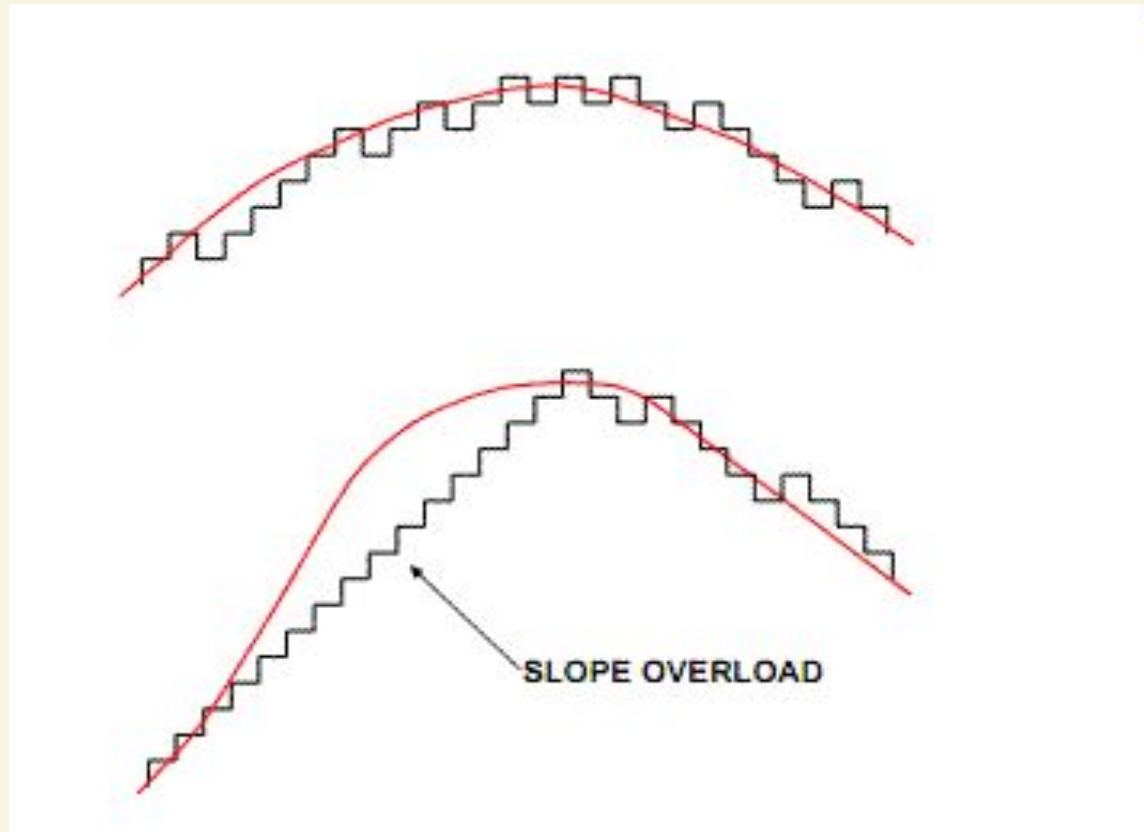


Структурна схема сигма-дельта АЦП.



CYPRUS

Delta Sigma Analog to Digital Converter (ADC_DelSig)



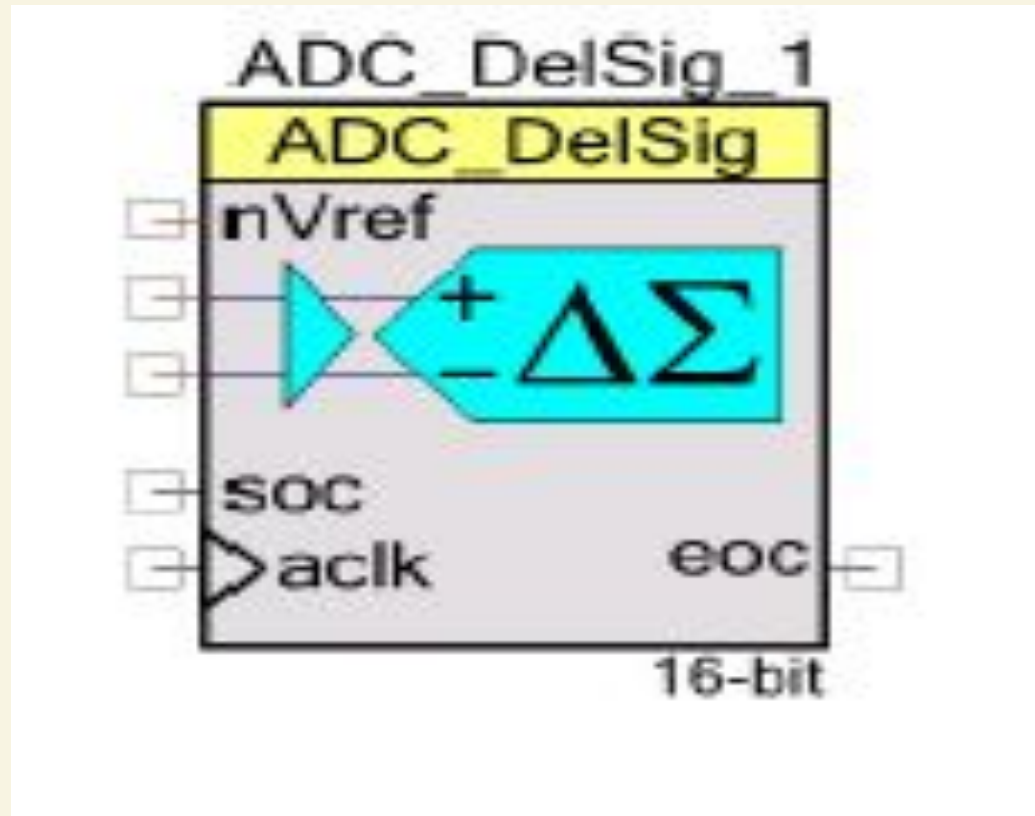
Сигма-дельта АЦП як слідкуюча система



Delta Sigma Analog to Digital Converter (ADC_DelSig)

- 1. When processing audio information, the ADC_DelSig is used in a continuous operation mode.**
- 2. When used for scanning multiple sensors, the ADC_DelSig is used in one of the multisample modes.**
- 3. When used for single-point high-resolution measurements, the ADC_DelSig is used in single-sample mode.**
- 4. Delta-sigma converters are good for both high-speed medium-resolution (8 to 16 bits) applications, and low-speed high-resolution (16 to 20 bits) applications. The sample rate can be adjusted between 10 and 384000 samples per second, depending on mode and resolution.**

Delta Sigma Analog to Digital Converter (ADC_DelSig)



It can produce 16-bit.



Delta Sigma Analog to Digital Converter (ADC_DelSig)

- 1. When used for single-point high-resolution measurements, the ADC_DelSig is used in single-sample mode.**
- 2. Delta-sigma converters are good for both high-speed medium-resolution (8 to 16 bits) applications.**
- 3. The sample rate can be adjusted between 2000 and 38400 samples per second, depending on mode and resolution.**

This example project shows how you can use **PSoC** to transfer data from one peripheral (**ADC**) to another (**LDC**),

Features

- Delta-Sigma ADC in single-ended mode
- LCD used to verify output

PSoC Creator 2.1


File Edit View Debug Project Build Tools Window Help

Workspace Explorer

Source Components Datasheets Results

Start Page

PSoC® Creator™



Recent Projects

- HelloWorld_Blinky01.cywrk
- CapSense_CSD_Design01...
- CapSense_CSD_Design01...
- CharLCD_CustomFont01.c...
- CharLCD_CustomFont01.c...

Create New Project...
Open Existing Project...

Getting Started

- PSoC Creator Start Page
- Quick Start Guide
- Intro to PSoC
- Intro to PSoC Creator
- PSoC Creator Training
- Help Tutorials
- Getting Started With PSoC 3
- Getting Started With PSoC 5

Examples and Kits

- Find Example Project...
- No Kit Packages Installed

简体中文 日本語 한국어 English


PSoC Creator News and Information

[Happy Lunar New Year!](#)
Posted on 02/11/2013

Gong Xi Fa Cai! As many of my friends and colleagues are celebrating the New Year and welcoming in the year of the water snake, I wanted to take a minute and wish you all well. May the New Year bring each of you prosperity, good luck and a new PSoC design.
[Read More](#)

[Tips + Tricks: Menu Customization](#)
Posted on 01/24/2013

Did you know you can create a customized menu in PSoC® Creator? Right click in a blank area of the top menu and select customize from the



Help

5% - Debug

Output

Show output from: All

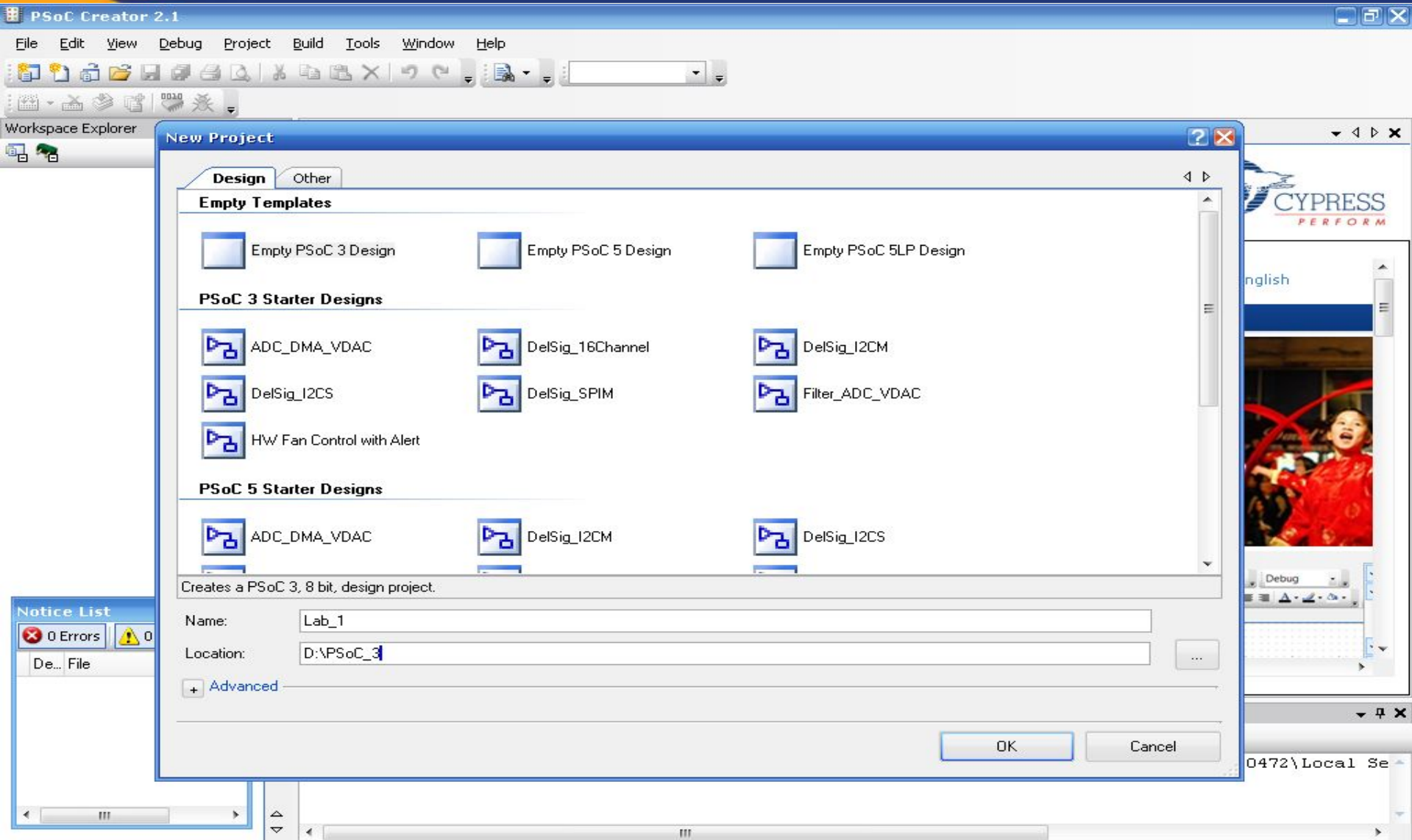
Log file for this session is located at: C:\Documents and Settings\Admin.MICROSOFT-7D0472\Local Se

Notice List

0 Errors 0 Warnings

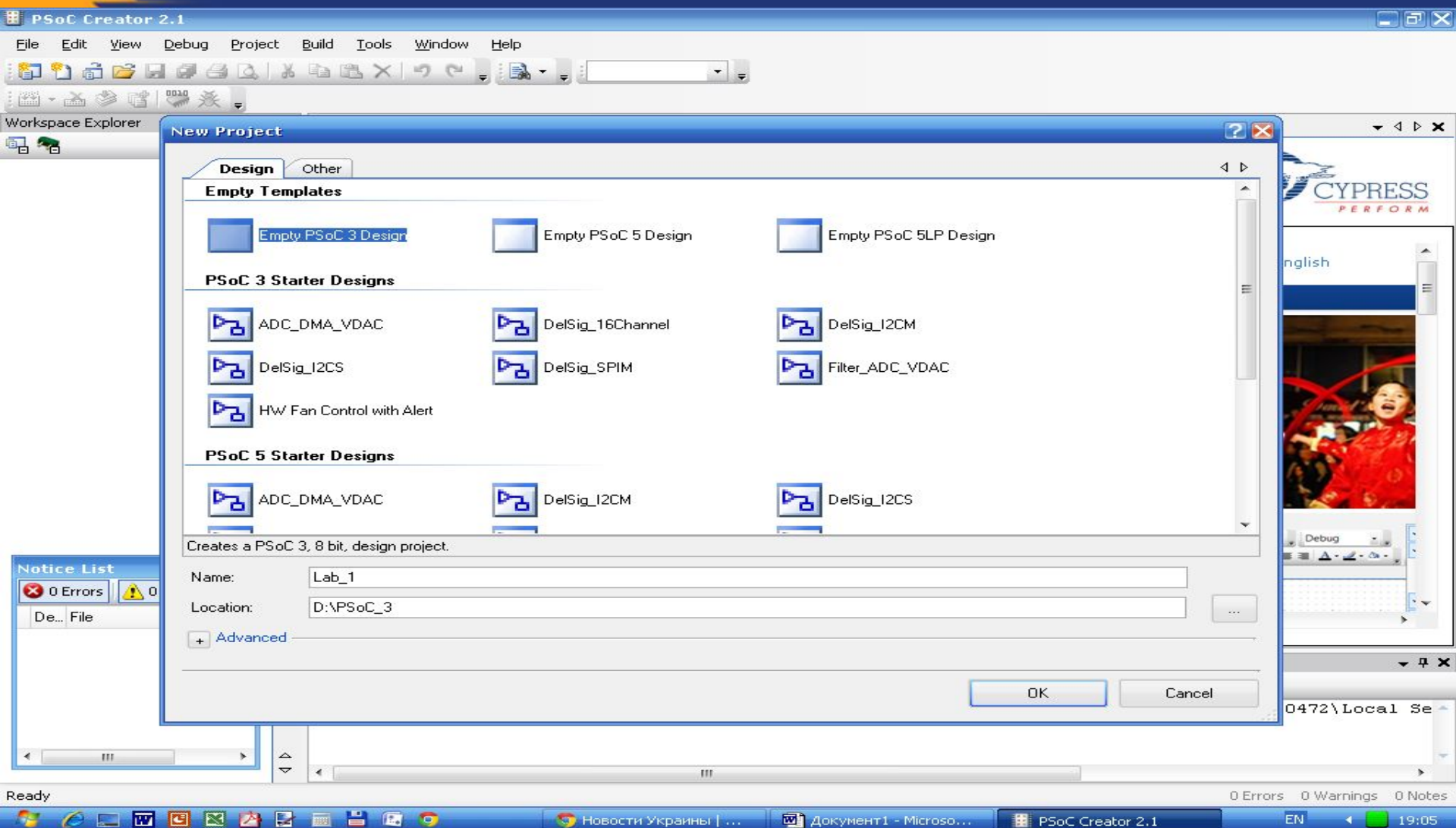
De...	File	Error L

File – New - Projekt



The screenshot shows the PSoC Creator 2.1 application window. The 'File' menu is open, and the 'New' option is selected, which has opened the 'New Project' dialog box. The dialog box has two tabs: 'Design' and 'Other'. Under the 'Design' tab, there are three sections: 'Empty Templates', 'PSoC 3 Starter Designs', and 'PSoC 5 Starter Designs'. The 'Empty Templates' section contains three options: 'Empty PSoC 3 Design', 'Empty PSoC 5 Design', and 'Empty PSoC 5LP Design'. The 'PSoC 3 Starter Designs' section contains six options: 'ADC_DMA_VDAC', 'DelSig_16Channel', 'DelSig_I2CM', 'DelSig_I2CS', 'DelSig_SPIM', and 'Filter_ADC_VDAC'. The 'PSoC 5 Starter Designs' section contains three options: 'ADC_DMA_VDAC', 'DelSig_I2CM', and 'DelSig_I2CS'. Below these sections, there is a description: 'Creates a PSoC 3, 8 bit, design project.' There are two input fields: 'Name:' with the value 'Lab_1' and 'Location:' with the value 'D:\PSoC_3'. There is also an 'Advanced' button with a plus sign. At the bottom right of the dialog box are 'OK' and 'Cancel' buttons. In the background, the main application window is visible, showing the 'Workspace Explorer' on the left and a 'Notice List' at the bottom left. The 'Notice List' shows '0 Errors' and '0 Warnings'. The taskbar at the bottom shows the Windows Start button, several application icons, and the system tray with the date and time '19:02'.

Empty PSoC 3/5 Design



PSoC Creator 2.1

File Edit View Debug Project Build Tools Window Help

Workspace Explorer

New Project

Design Other

Empty Templates

- Empty PSoC 3 Design
- Empty PSoC 5 Design
- Empty PSoC 5LP Design

PSoC 3 Starter Designs

- ADC_DMA_VDAC
- DelSig_I2CS
- HW Fan Control with Alert
- DelSig_16Channel
- DelSig_SPIM
- DelSig_I2CM
- Filter_ADC_VDAC

PSoC 5 Starter Designs

- ADC_DMA_VDAC
- DelSig_I2CM
- DelSig_I2CS

Creates a PSoC 3, 8 bit, design project.

Name: Lab_1

Location: D:\PSoC_3

+ Advanced

OK Cancel

Notice List

0 Errors 0 Warnings

0472\Local Se

Ready

0 Errors 0 Warnings 0 Notes

EN 19:05



Lab_6 ADC+LCD

CharLCD_CustomFont01 - PSoC Creator 2.1 [F:\...\CharLCD_CustomFont01.cydsn\TopDesign\TopDesign.cysch]

File Edit View Debug Project Build Tools Window Help

Microsoft Sans Serif 10 B I U

Workspace Explorer (1 project)

Project 'CharLCD_CustomFont01'

- TopDesign.cysch
- CharLCD_CustomFont01
 - Header Files
 - device.h
 - Source Files
 - main.c
 - Generated_Source
 - PSoC3
 - cy_boot
 - CyBootAsmk
 - CyDmac.c
 - CyDmac.h
 - CyFlash.c
 - CyFlash.h
 - CyLib.c
 - CyLib.h
 - cymem.a51
 - cypins.h

Component Catalog (174 components)

Cypress Component Catalog

- Display
 - Character LCD [v1.70]

Notice List

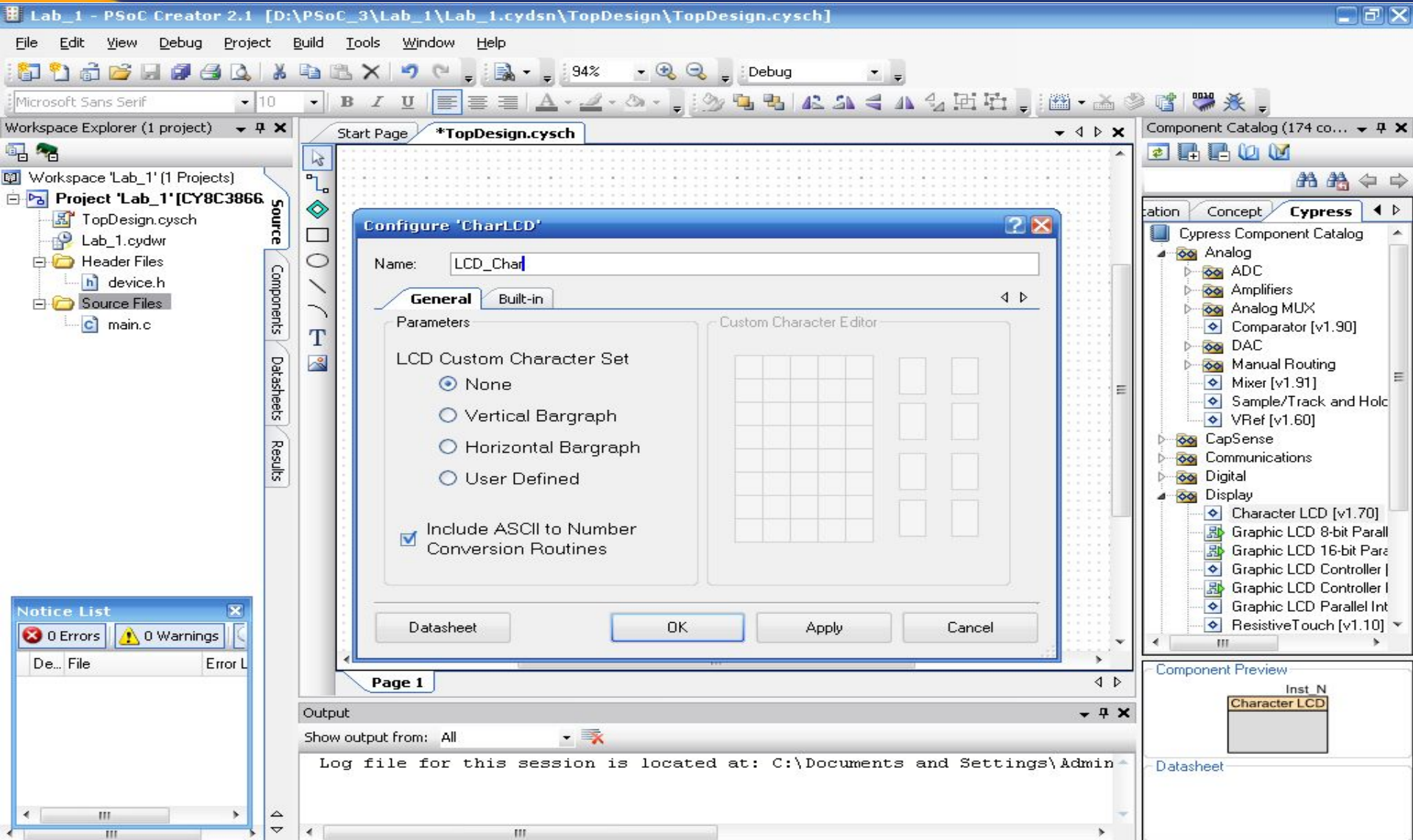
0 Errors 0 Warnings

Output

Show output from: All

Log file for this session is located at: C:\Documents and Settings\Admin...

Configure LCD



The screenshot shows the PSoC Creator 2.1 software interface. The main window displays the 'Configure CharLCD' dialog box for a component named 'LCD_Char'. The dialog has two tabs: 'General' and 'Built-in'. Under the 'General' tab, there are two sections: 'Parameters' and 'Custom Character Editor'. In the 'Parameters' section, the 'LCD Custom Character Set' is set to 'None'. Other options include 'Vertical Bargraph', 'Horizontal Bargraph', and 'User Defined'. The 'Include ASCII to Number Conversion Routines' checkbox is checked. The 'Custom Character Editor' section contains a grid for defining characters. At the bottom of the dialog are buttons for 'Datasheet', 'OK', 'Apply', and 'Cancel'. The background shows the workspace explorer with a project named 'Project Lab_1' and a component catalog on the right side listing various components like ADC, DAC, and Display. A 'Notice List' window is open in the bottom left corner, showing 0 errors and 0 warnings. The output window at the bottom shows a log message: 'Log file for this session is located at: C:\Documents and Settings\Admin...'

Lab_6 ADC+LCD

Lab_1 - PSoC Creator 2.1 [D:\PSoc_3\Lab_1\Lab_1.cydsn\Lab_1.cydw]

File Edit View Debug Project Build Tools Window Help

37% Debug

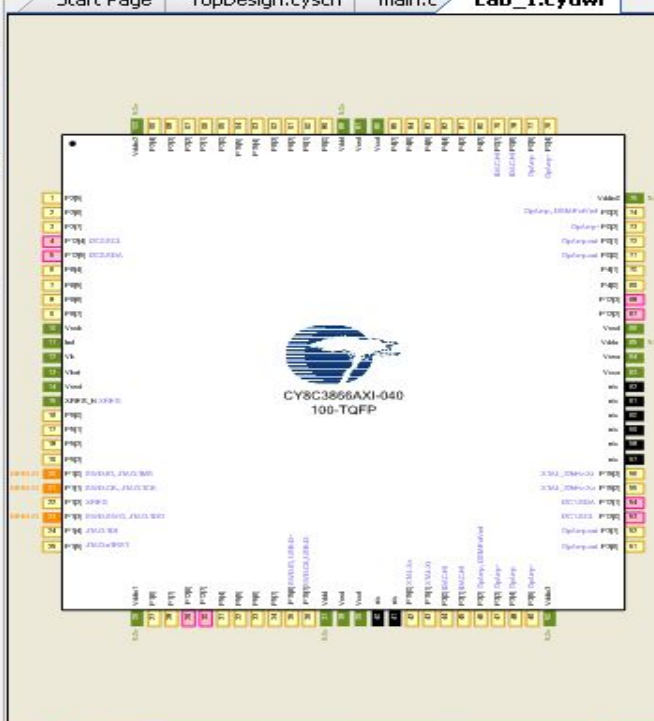
Workspace Explorer (1 project)

Workspace 'Lab_1' (1 Projects)

- Project 'Lab_1' [CY8C3866]
 - TopDesign.cysch
 - Lab_1.cydw
 - Header Files
 - device.h
 - Source Files
 - main.c

Source Components Datasheets Results

Start Page TopDesign.cysch main.c Lab_1.cydw



CY8C3866AXI-040
100-TQFP

Alias	Name	Port	Pin	Lock
	\LCD_Char:LCDPort[6:0]\			
	P0[6:0]	IDAC:HC		
	P0[7:1]	IDAC:HC		
	P2[6:0]			
	P2[7:1]			
	P3[6:0]	OpAmp:c		
	P3[7:1]	OpAmp:c		
	P4[6:0]			
	P4[7:1]			
	P5[6:0]			

LCD_Char_LCDPort_6 - Digital
LCD_Char_LCDPort_5 - Digital
LCD_Char_LCDPort_4 - Digital

Pins Analog Clocks Interrupts DMA System Directives Flash Security

Output

Show output from: All

Log file for this session is located at: C:\Documents and Settings\Admin.MICROSOFT-7D0472\Local Se

Notice List

0 Errors 0 Warnings

De... File Error L

Ready

0 Errors 0 Warnings 0 Notes

EN 19:33

Adding Components

To see how the ADC works we need an analog signal to convert. We're going to use a potentiometer to provide one analog signal. A basic potentiometer provides a great diagnostic tool for analog processing since you can slowly sweep the signal through the range of the potentiometer and observe the output. Char LCD to provide visual feedback.

- 1. Drag an Analog Pin component onto your design.**
- 2. Name it VR_Pin. This pin will be connected to the potentiometer on the DVK.**
- 3. The potentiometer output will send to the ADC.**

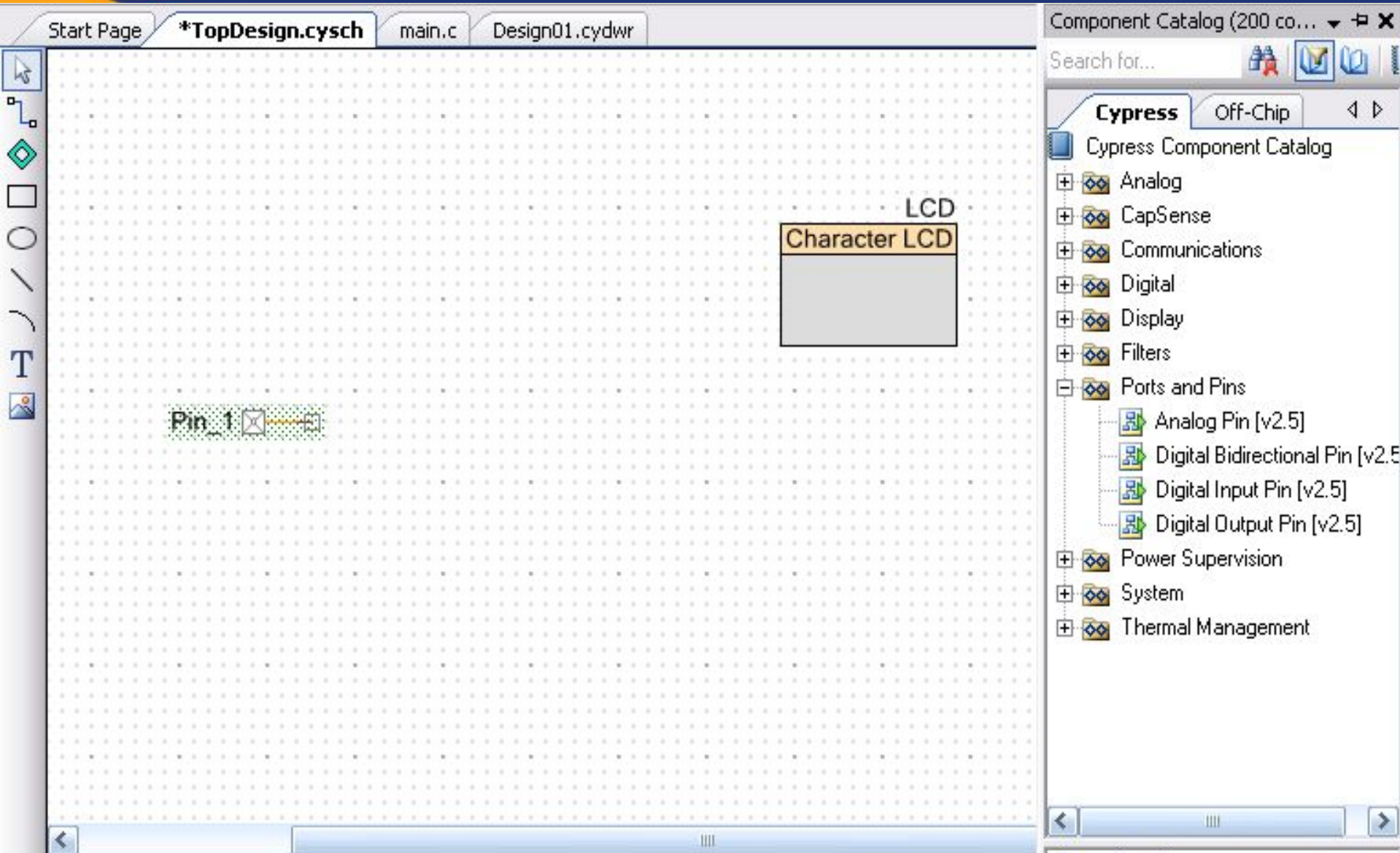
This design adds only one external pin for the potentiometer.

- **Open the design-wide resource file and assign the pins (Рис.1).**
- **Build the project.**
- **Add a wire to the DVK board connecting P0_7 to the VR.**
- **Make sure the VR_PWR jumper on the DVK is placed properly to provide power to the potentiometer.**

	\CharLCD:LCDPort\[6:0]	P2[6:0]	▼	☑
	VR_Pin	P0[7]	▼	☑

Рис.1

Lab_6 ADC+LCD



The screenshot shows the Cypress PSoC Designer IDE interface. The main workspace contains a schematic design on a grid. A component labeled "Character LCD" is placed on the right side, with the text "LCD" above it. A component labeled "Pin_1" is placed on the left side. The top of the window shows tabs for "Start Page", "*TopDesign.cysch", "main.c", and "Design01.cydwr". The right-hand side features a "Component Catalog" window with a search bar and a tree view of components. The tree view is expanded to show the "Ports and Pins" category, which includes "Analog Pin [v2.5]", "Digital Bidirectional Pin [v2.5]", "Digital Input Pin [v2.5]", and "Digital Output Pin [v2.5]".

Start Page *TopDesign.cysch main.c Design01.cydwr

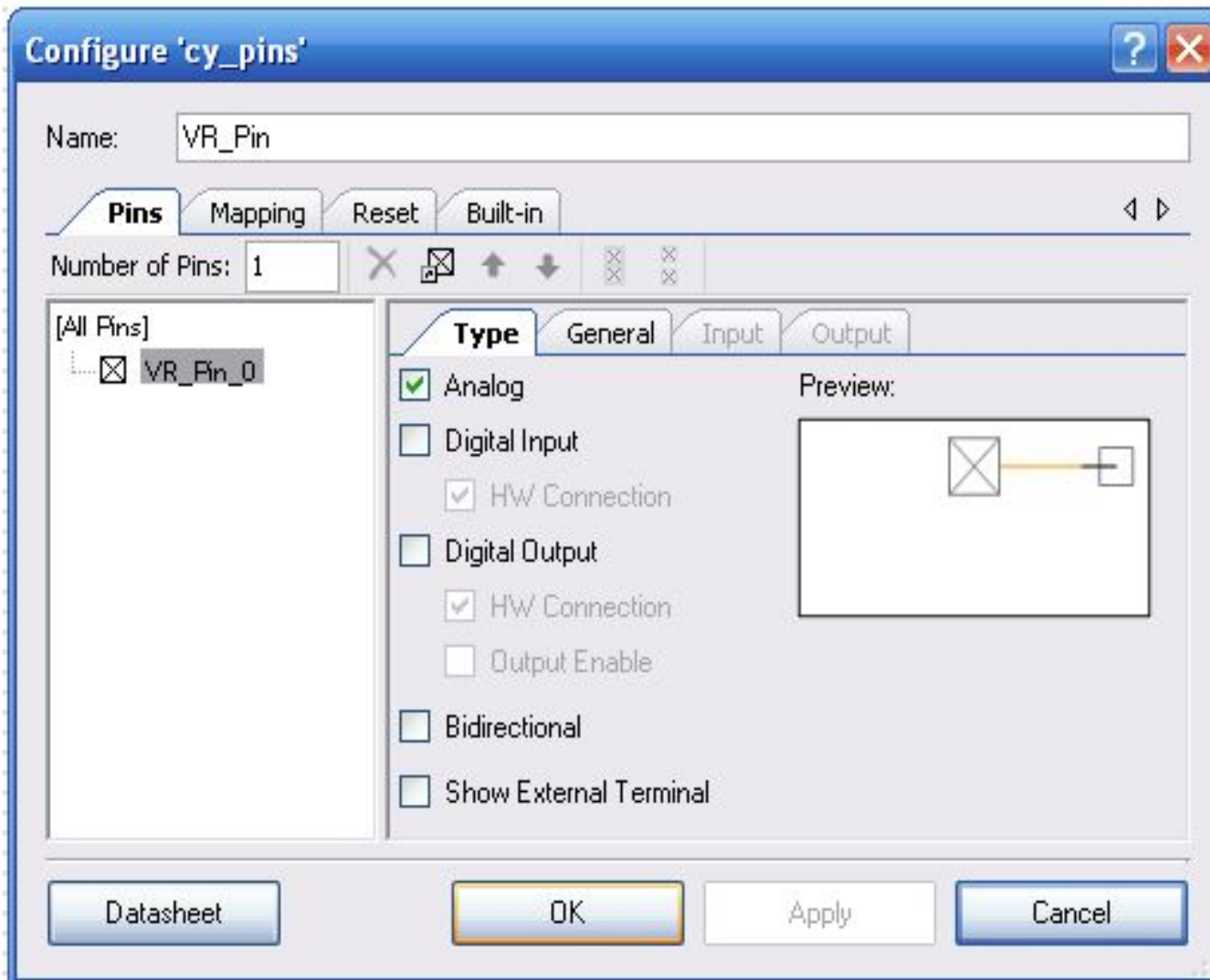
Component Catalog (200 co... X

Search for...

Cypress Off-Chip

Cypress Component Catalog

- + Analog
- + CapSense
- + Communications
- + Digital
- + Display
- + Filters
- Ports and Pins
 - Analog Pin [v2.5]
 - Digital Bidirectional Pin [v2.5]
 - Digital Input Pin [v2.5]
 - Digital Output Pin [v2.5]
- + Power Supervision
- + System
- + Thermal Management



Start Page *TopDesign.cysch main.c Design01.cydwr

Configure 'cy_pins'

Name: VR_Pin

Pins Mapping Reset Built-in

Number of Pins: 1

[All Pins]

VR_Pin_0

Type

General Input Output

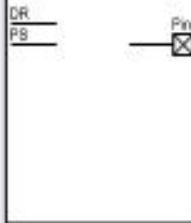
Drive Mode

High Impedance Analog

Initial State:

Low (0)

Minimum Supply Voltage:



Datasheet

OK

Apply

Cancel



Lab_6 Adding Components

- Drag an **Analog Pin** component onto your design
Name it **VR_Pin**.
This pin will be connected to the potentiometer on the DVK
- Add a **Delta Sigma ADC** component from the Component Catalog to your design
- Double Click the **ADC** to configure it.
Name the component **ADC**.
- Set the **Conversion Mode** to **Continuous**.
- Set the **Resolution** to be **14** bits and the **Conversion Rate** to be **5,000 SPS** (samples per second).
- Set the **Input Range** to be **Vssa to Vdda (Single Ended)**
- Set the **Input Buffer Gain** to **1**
- Select **Single Ended** Input mode

Lab_6 ADC+LCD

Start Page *TopDesign.cysch main.c Design01.cydwr

Component Catalog (200 co... Search for...

Cypress Off-Chip

- Cypress Component Catalog
 - Analog
 - ADC
 - Delta Sigma ADC [v...
 - Amplifiers
 - Analog MUX
 - Comparators
 - DAC
 - Manual Routing
 - Mixer [v2.0]
 - Sample/Track and Hold
 - VRef [v1.60]
 - CapSense
 - Communications
 - Digital
 - Display
 - Filters
 - Ports and Pins
 - Power Supervision
 - System

VR_Pin [07] []

ADC_DelSig_1
ADC_DelSig

+

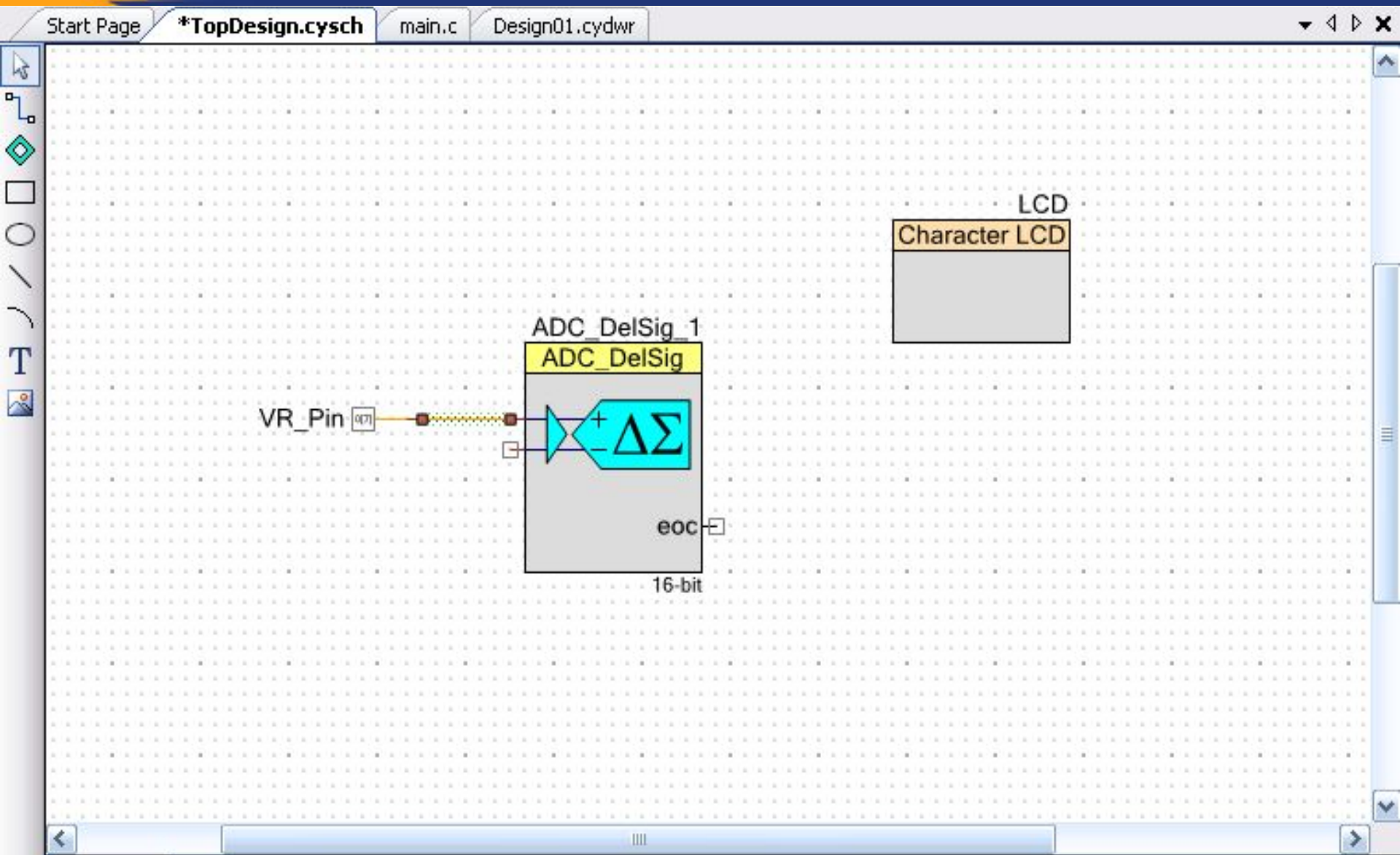
$\Delta\Sigma$

eoc []

16-bit

LCD
Character LCD

Lab_6 ADC+LCD



Configure 'ADC_DeISig'

Name:

Config1 | Config2 | Config3 | Config4 | Common | Built-in

Comment:

Configuration name: ADC_DeISig_1_CFG1

Modes

Conversion mode:

Resolution (bits):

Conversion rate (SPS): Range: 2000 - 48000 SPS

Actual conv. rate (SPS):

Clock frequency (kHz):

Input options - Differential mode

Input range:

Buffer gain:

Buffer mode:

Reference

Reference:

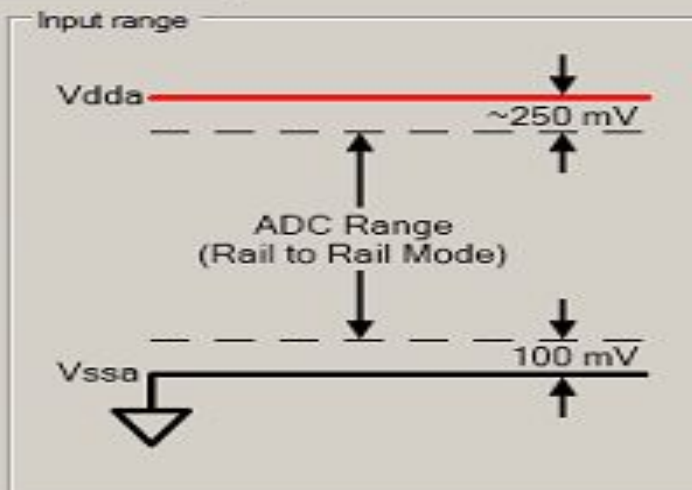
Vref (V):

Alignment

Right Coherency = LOW

Left

Input range



The diagram shows the input range between Vdda and Vssa. The ADC Range (Rail to Rail Mode) is indicated as approximately 250 mV. A 100 mV range is also shown below the Vssa rail.

Datasheet OK Apply Cancel

Configure 'ADC_DeISig'

Name: ADC

Config1 Config2 Config3 Config4 Common Built-in

Comment: Default Config

Configuration name: CFG1 ADC_CFG1

Modes

Conversion mode: 2 - Continuous

Resolution (bits): 14

Conversion rate (SPS): 5000 Range: 2783 - 133565 SPS

Actual conv. rate (SPS): 5017

Clock frequency (kHz): 230.000

Input options - Differential mode

Input range: +/-2.048V [-Input +/- 2*Vref]

Buffer gain: 1

Buffer mode: Rail to Rail

Input range



Reference

Datasheet

OK

Apply

Cancel

Start Page | TopDesign.cysch | main.c | Design01.cydwr

Configure 'ADC_DeISig'

Name: ADC

Config1 | Config2 | Config3 | Config4 | Common | Built-in

Actual conv. rate (SPS): 5017

Clock frequency (kHz): 230.000

Input options - Differential mode

Input range: $\pm 2.048V$ (-Input $\pm 2 \cdot V_{ref}$)

Buffer gain: 1

Buffer mode: Rail to Rail

Reference

Reference: Internal 1.024 Volts

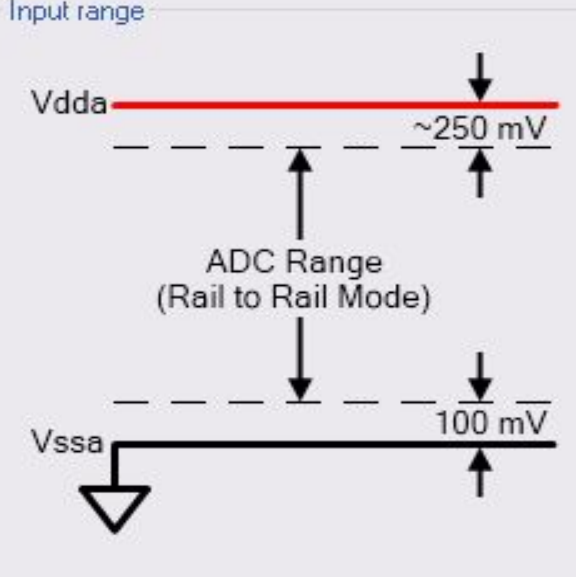
Vref (V): 1.024

Alignment

Right Coherency = LOW

Left 16 bits (DVF Protected)

Input range diagram:



Vdda

$\sim 250\text{ mV}$

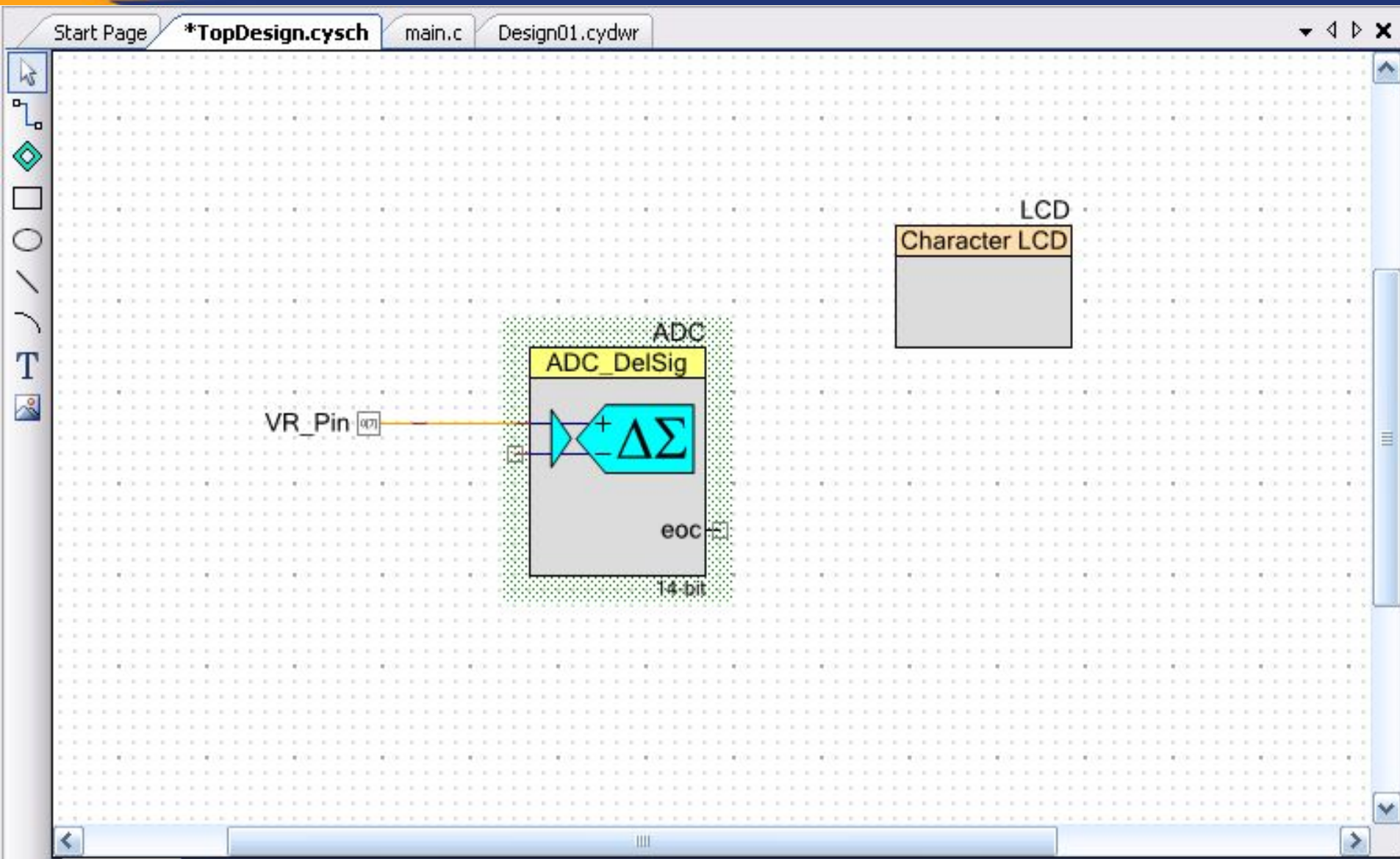
ADC Range (Rail to Rail Mode)

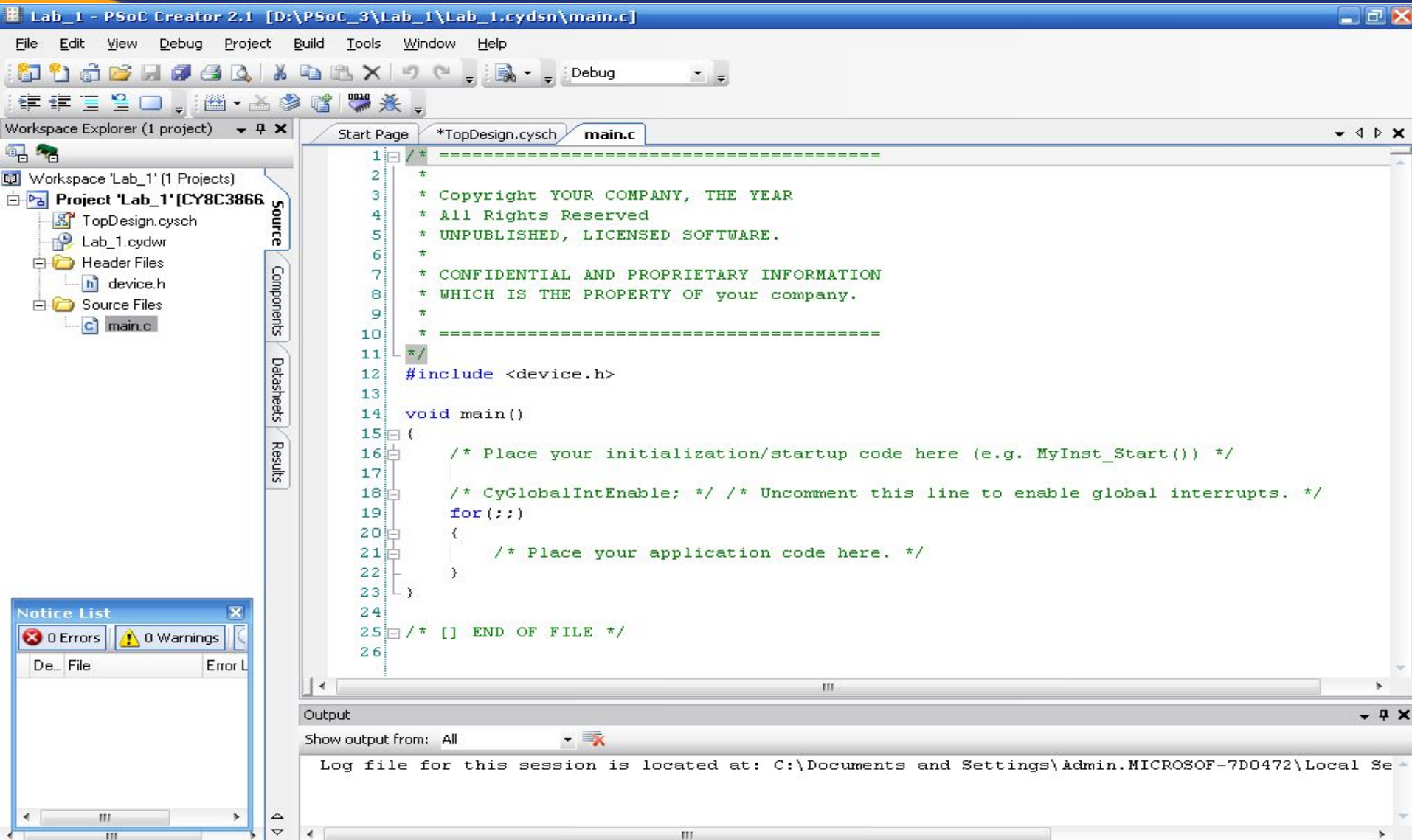
100 mV

Vssa

Datasheet OK Apply Cancel

Lab_6 ADC+LCD





Lab_1 - PSoC Creator 2.1 [D:\PSoC_3\Lab_1\Lab_1.cydsn\main.c]

File Edit View Debug Project Build Tools Window Help

Debug

Workspace Explorer (1 project)

Project 'Lab_1' [CY8C3866]

- TopDesign.cysch
- Lab_1.cydwr
- Header Files
- device.h
- Source Files
- main.c

```
1  /* -----  
2  *  
3  * Copyright YOUR COMPANY, THE YEAR  
4  * All Rights Reserved  
5  * UNPUBLISHED, LICENSED SOFTWARE.  
6  *  
7  * CONFIDENTIAL AND PROPRIETARY INFORMATION  
8  * WHICH IS THE PROPERTY OF your company.  
9  *  
10 * -----  
11 */  
12 #include <device.h>  
13  
14 void main()  
15 {  
16     /* Place your initialization/startup code here (e.g. MyInst_Start()) */  
17  
18     /* CyGlobalIntEnable; */ /* Uncomment this line to enable global interrupts. */  
19     for (;;)   
20     {  
21         /* Place your application code here. */  
22     }  
23 }  
24  
25 /* [] END OF FILE */  
26
```

Notice List

0 Errors 0 Warnings

De...	File	Error L
-------	------	---------

Output

Show output from: All

Log file for this session is located at: C:\Documents and Settings\Admin.MICROSOFT-7D0472\Local Se

Ln 1 Col 1 INS 0 Errors 0 Warnings 0 Notes

Make the following changes to the beginning of *main.c*.

```
#include "myADC.h"
```

```
.....
```

```
void main()
```

```
{
```

```
/* Components should be initialized in the following order:
```

```
* 1. interrupts
```

```
* 2. sources of interrupts (clocks are auto-initialized)
```

```
* 3. global interrupt enable
```

```
*/
```

```
InitAdc(); /* source of interrupt */
```

```
CYGlobalIntEnable /* macro */
```

```
/* Initialize other components, not associated with interrupts */
```

```
CharLCD_Start();
```

Create a file called *myADC.c*.

Add the following code to the *myADC.c* file.

```
#include <device.h>
#include "myADC.h"
/*****
* Global Functions
*****/
/*****
* Function Name: InitAdc()
*****/
void InitAdc(void)
{
ADC_Start();
ADC_StartConvert(); /* Starts a continuous conversion process */
} /* end of InitAdc() */
```



```
/* **** */
* Function Name: UpdateAdc()
* **** */
void UpdateAdc(void)
{
if(ADC_IsEndConversion(ADC_RETURN_STATUS))
{
uint8 adcval8;
/* Get 14-bit conversion reported in a signed 16-bit result, and limit
* negative and positive overflow. */
int16 adcval16 = ADC_GetResult16();
if(adcval16 < 0)
{
adcval16 = 0;
}
else if(adcval16 > 0x3FFF)
{
adcval16 = 0x3FFF;
}
else {} /* value is in range, do nothing */
```



```
/* Convert to an 8-bit result; grab the 8 MS bits. */  
adcval8 = (uint8)(((uint16)adcval16 >> 6) & 0xFFU);  
if(source != 0U)  
{  
    adcval8 *= 3U;  
}  
/* display the result on the char LCD */  
CharLCD_Position(1U, 6U); /* row, column */  
CharLCD_PrintHexUint8(adcval8);  
* Print (val / 4) (with rounding, add half the divisor) 'X' characters,  
* which creates a horizontal line whose length is proportional to the  
* ADC value.  
*/  
adcval8 = (uint8)(((uint16)adcval8 + 2U) / 4U);  
if (adcval8 == 0U) /* make sure that at least one 'X' is printed */  
{  
    adcval8 = 1U;  
}  
} /* end of if (ADC_IsEndConversion(ADC_RETURN_STATUS)) */  
} /* end of UpdateAdc() */
```

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