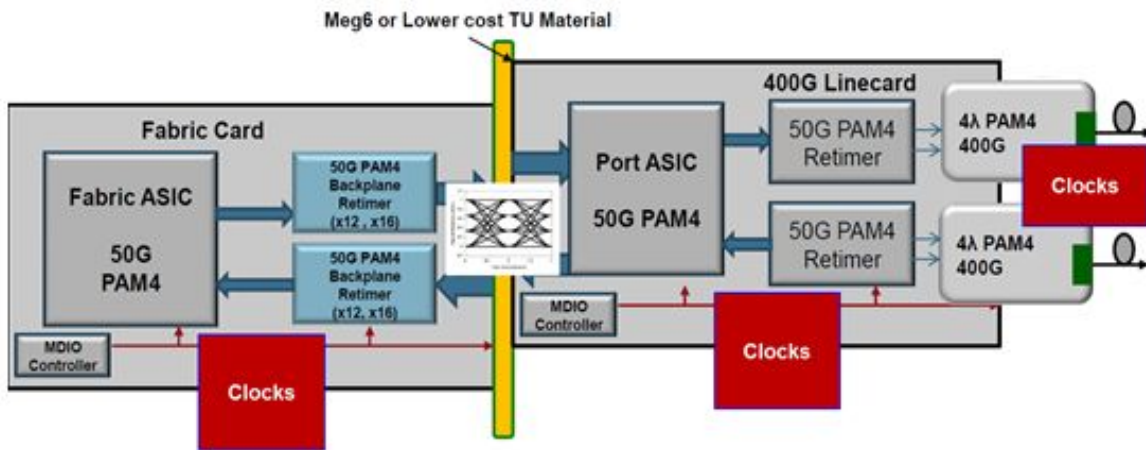


Clocking for Telecom Infrastructure & Data Center Applications

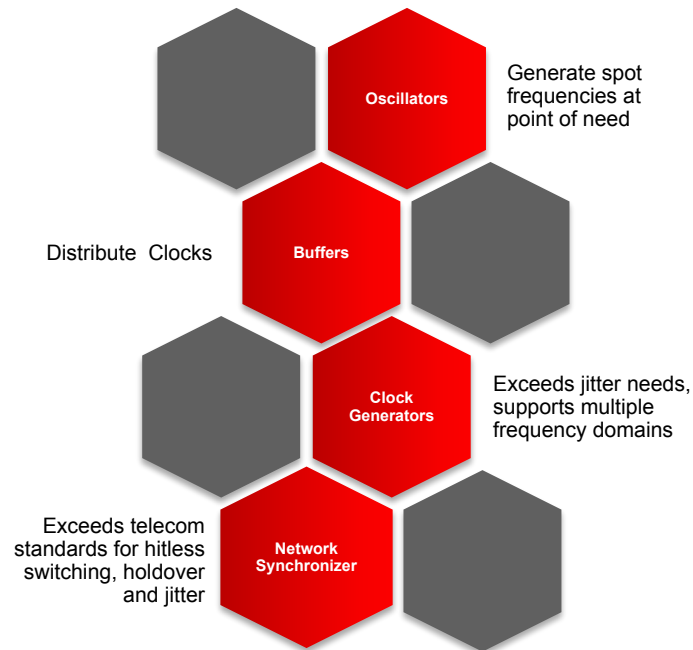
Clock and Timing Solutions

TI clocks for Telecom Infrastructure & Data Center

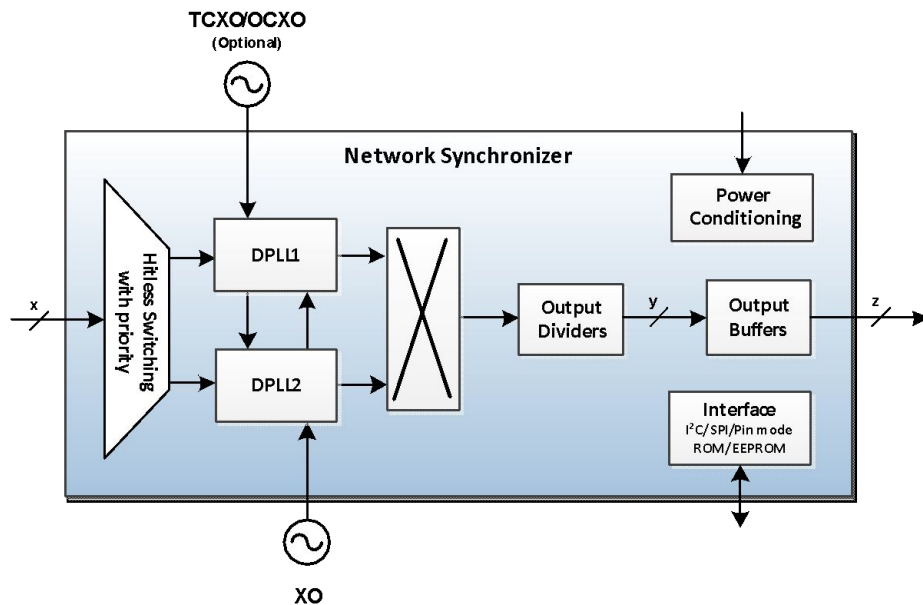
- One of few suppliers offering end to end solutions
- High Performance, cost optimized solutions for all telecom standards



TI Information – Selective Disclosure

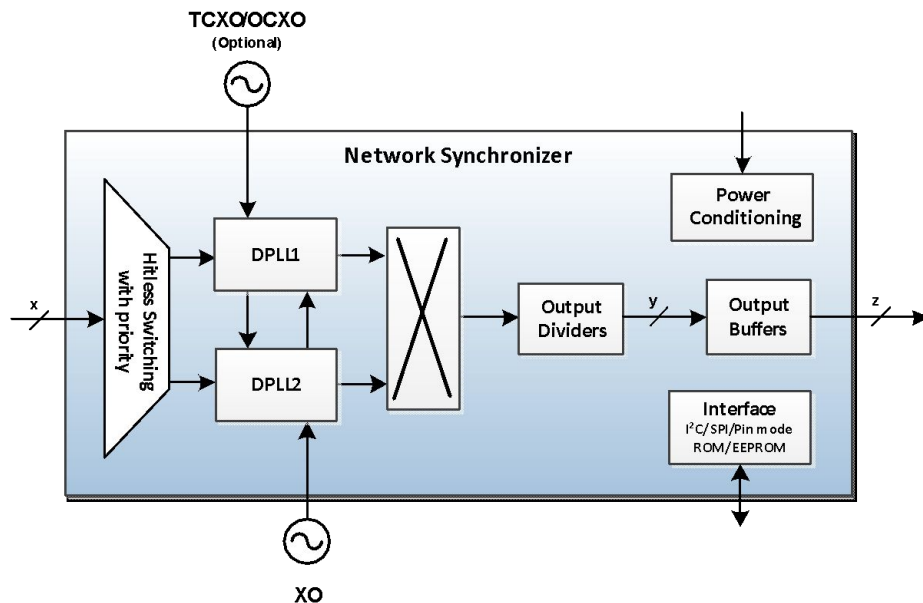


Why use TI Network Synchronizers



- Exceeds jitter requirements on reference clocks for current and next generation serial links
- Industry leading performance on hitless switching and holdover
- Robust operation with high level of immunity to system level noises on power supply with superior PSRR
- High level of flexibility (multiple frequency domains derived from single device) and easy to use (integrated EEPROM, tools)

Popular Network Synchronizer product



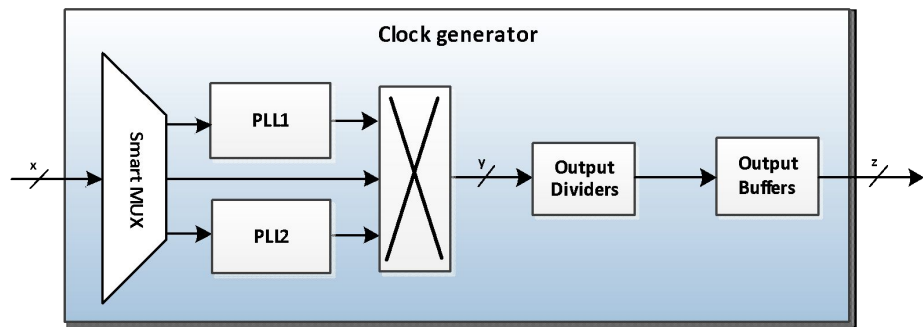
- 2 independent synchronizers with 4 inputs and 8 outputs
- Industry leading hitless switching and holdover performance
- Supports 10MHz OCXO while still exceeding 100G jitter requirements
- Superior PSRR on all supplies
- Flexible and easy to use with integrated NVM

LMK05028 competitive analysis

FEATURES	LMK05028	SI5346	AD9559	ZL30612
Input frequency Range [MHz]				
Differential	2 kHz – 750 MHz	8 kHz - 750 MHz	2 kHz - 1250 MHz	1 kHz - 900 MHz
Single-Ended	2 kHz – 750MHz	8 kHz - 250 MHz	2 kHz - 300 MHz	1 kHz - 180 MHz
Output frequency range [MHz]				
Differential	2 kHz – 750MHz	8 kHz - 800 MHz	262 kHz - 1250 MHz	0.5Hz - 900 MHz
Single-Ended	2 kHz – 200MHz	8 kHz - 250 MHz	262 kHz - 250 MHz	0.5Hz - 180 MHz
No of Unique Outputs (Non-VCO related)	2	3	2	4
Supply Voltage [V]	3.3 and 1.8	3.3 and 1.8	3.3 and 1.8	3.3 and 1.8
Power Dissipation [W]	2W (Max)	1.25W (Max, scaled for same config)	1.25W (Max, scaled for same config)	TBD
PSRR with PCB filter (dBc)	< -95	< -80	TBD	TBD
RMS Jitter Performance (12 kHz - 20 MHz)	200fs max with 10MHz OCXO	500fs rms with 10MHz OCXO	331fs rms (typ)	180fs rms (typ, P) 17ps rms (GP)
Max phase transient during hitless switch (synchronous inputs)	< 10ps	2.8ns	TBD	100ps
Phase transient behavior with switching between async inputs	Smooth	Ringing	TBD	TBD
Supported standards	G.8262	G.8262	G.8262	G.8262

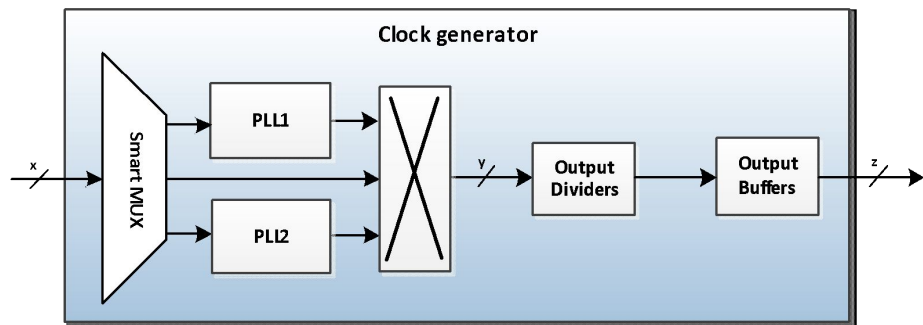
TI Inform

Why use TI Clock Generators



- Exceeds jitter requirements on reference clocks for current and next generation serial links
- Robust operation with high level of immunity to system level noises on power supply with superior PSRR
- High level of flexibility (multiple frequency domains derived from single device) and easy to use (integrated EEPROM, tools)

Popular Clock Generator product

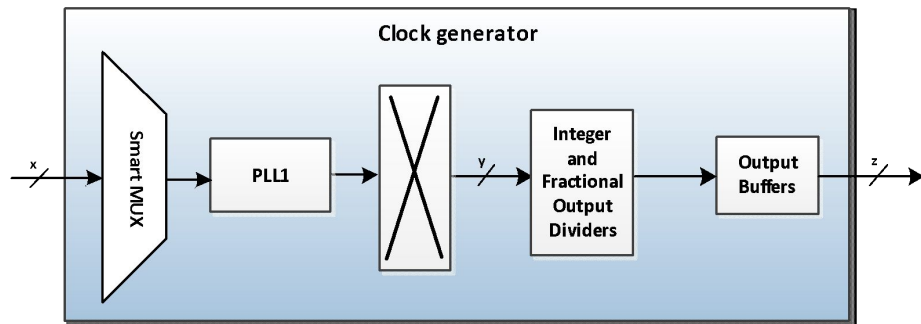


- **2 independent synthesizers with 4 inputs and 8 outputs**
- **Exceeds 100G serial link jitter requirements**
- **Superior PSRR on all supplies**
- **Flexible and easy to use with integrated NVM**

LMK03328 Competitive Analysis

Parameter/Feature	TI LMK03328	SI5341	IDT 8T49NS010
Device control	I2C, EPROM Pin mode	I2C, SPI	I2C, Pin mode
NVM	Y, 100 writes	Y, 2 writes	N
Pin mode settings	Y, 64 states	N/A	Y, 8 states
Flexibility	High	High	Low Limited divider settings
Frequency Margining	Fine and Coarse	Coarse	N/A
RMS Jitter @156.25 LVPECL fs 25MHz input	120	160	120
Output Types	LVPECL, LVDS, HCSL, LVCMOS		LVPECL, LVDS
PSRR (dBc)	-92	-80	TBD
Number of Outputs	8 outputs (Differential or 2x LVCMOS)	10 outputs (Differential or 2x LVCMOS)	10 outputs (Differential)
Operating Conditions °C	-40 to 85	-40 to 85	-40 to 85
Power supply Analog V	3.3	3.3	3.3
Power supply Digital V	1.8/2.5/3.3	1.8/2.5/3.3	3.3
Power Dissipation W	2.25	1.14	2.57
Package Type	7mm x 7mm QFN-48	9mm x 9mm QFN-64	8mm x 8mm QFN-56

Popular Clock Generator product

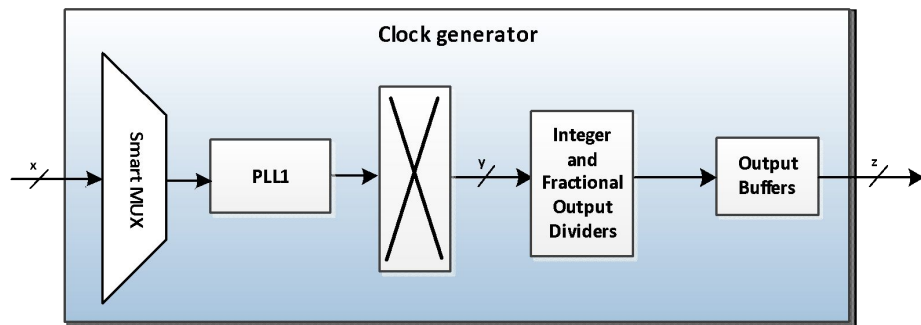


- 1 synthesizer with 2 inputs, 8 outputs and 4 fractional dividers
- Exceeds 40G serial link and PCI Express Gen 4 jitter requirements
- Superior PSRR on all supplies
- Flexible and easy to use with integrated NVM

CDCM6208 Competitive Analysis

Parameter/Feature	TI CDCM6208	ADI AD9522	IDT 8T49N8018
Device control	I2C, SPI, Pin mode	SPI	I2C
Pin mode settings	Y, 32 states	N/A	N/A
Flexibility	High	Low	High
RMS Jitter @156.25 LVPECL fs 25MHz input	265	400	350
Output Types	LVPECL, LVDS, HCSL, LVCMOS		
PSRR (dBc)	-70	TBD	TBD
Number of Outputs	8 outputs (Differential or 2x LVCMOS)	10 outputs (Differential or 2x LVCMOS)	8 outputs (Differential or 2x LVCMOS)
Operating Conditions °C	-40 to 85	-40 to 85	-40 to 85
Power supply Analog V	1.8/2.5/3.3	3.3	2.5/3.3
Power supply Digital V	1.8/2.5/3.3	3.3	2.5/3.3
Power Dissipation W	0.45	1.2	1.2
Package Type	7mm x 7mm QFN-48	9mm x 9mm QFN-64	8mm x 8mm QFN-56

Popular Clock Generator product

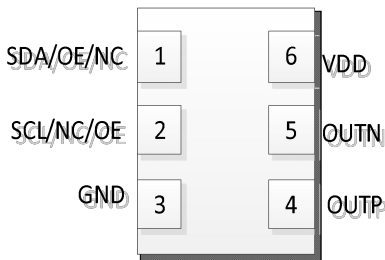
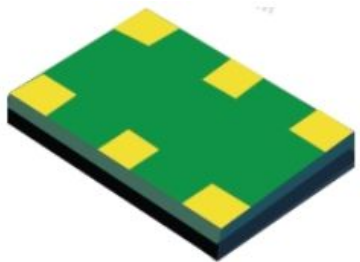


- 1 synthesizer with 2 inputs, 4 outputs and 4 fractional dividers
- Exceeds Express Gen 4 jitter requirements
- Superior PSRR on all supplies
- Flexible and easy to use with integrated NVM

CDCI6214 Competitive Analysis

Parameter/Feature	IDT Versaclock 5	SiLabs 5338	CDCI6214
Number of Outputs	4	4	4+1
Power consumption in PCIe config	256mW	225mW	<200mW
Power consumptio 10GbE config	170mW	139mW	<150mW
Programming	OTP	OTP	EEPROM
RMS jitter	800fs	700fs	500fs
Package	24 QFN	24QFN	24QFN

Oscillator family key highlights



- Available in standard footprint 7x5 and 5x3.2
- Frequency independent lead times
- LMK61K2-322M26 and LMK62K2-156M25 qualified with Intel
- Programmable LMK61E0 supported by Broadcom firmware
- Total stability of 25 and 50 ppm

LMK60xx, LMK62xx Competitive Analysis

Electrical Specs	Units	LMK60xx, 62xx	EG-2102CB	SI513	MX55
Typical Output Jitter	fs, rms	150	169	800	175
Maximum Total Frequency Stability	ppm	± 25 ± 50	± 50 ±100	± 30 ± 50 ± 100	± 50
Output Frequency Range	MHz	10 - 800 (LVPECL) 10 - 800 (LVDS) 10-400 (HCSL)	100 - 700 (Diff)	0.1 - 250 (Diff)	156.25 (LVPECL)
Typical PSRR, 50mV ripple	dBc	-65	TBD	-60	tbd
Maximum Startup Time	ms	10	10	10	20
Power supply	V	3.3	2.5/3.3	1.8/2.5/3.3	2.5/3.3
Max Icc	mA	120	60	43	120

TI Buffer Portfolio

Device	Outputs	Format	Freq	Add. Jitter RMS	PN Floor	VDD	Package	Extra Features
CDCLVDxxxx	1:4 to 1:16	LVDS	800 MHz	171fs @100MHz 65fs @737MHz	-156dBc/Hz @100MHz -146.5dBc/Hz @ 737MHz	2.5	16QFN (3x3) to 48QFN (7x7)	
CDCLVPxxxx	1:2 to 1:16	LVPECL	2GHz	57fs@122.88MHz 48fs@156.25MHz 30fs@312.5MHz	-161dbc/Hz @156.25MHz	2.5V/3.3V	16QFN (3x3) 48QFN (7x7)	
CDCLVCxxxx	1:2 to 1:12	LVC MOS	250MHz	100fs@250MHz	-161dBc/Hz @100MHz	2.5V/3.3V	8-24 TSSOP	
LMK0030x	3:4 3:8	LVPECL LVDS HCSL	3.1 GHz	55fs@156.25MHz	-162 dBc/Hz @100MHz -158 dBc/Hz@156.25MHz 154dBc/Hz@625MHz	2.5V/3.3V	32QFN (5x5) 40QFN (6x6)	XO Stage PSRR <-70dB LDOs
LMK0033x PCIe Gen4	1:4 1:8	HCSL	400 MHz	30fs@100MHz (PCIe mask)	-161dBc/Hz@100MHz	2.5V/3.3V	32QFN (5x5) 40QFN (6x6)	XO Stage PSRR <-70dB LDOs
LMK0x1xxx	1:8	LVDS LVPECL	1.6GHz	80fs@200MHz 30fs@800MHz 25fs@1.6GHz	-156dBc/Hz @200Mz -153dBc/Hz @800MHz -148dBc/Hz @1.6GHz	3.3V	48QFN (7x7)	Dividers + Delay SPI Interface
CDCLVC1310	1:10	LVC MOS	200 MHz	25fs@125MHz	-164dBc/Hz @125MHz	3.3V/2.5V/ 1.8V/1.5V	32QFN (5x5)	XO stage LDOs
LMK01801	2:14	LVDS LVPECL LVC MOS	3.1GHZ	50fs@800MHz	-163dBc/Hz @100MHz -154dBc/Hz @1GHz -148dBc/Hz @3GHz	3.3V	48QFN (7x7)	Dividers + Delay SPI Interface LDOs
CDC3S04	1:4	SINE	52MHz	100fs@38.4MHz	-150dBc/Hz @38.4MHz	1.8V	20WCSP (1.6x2)	I2C, LDOs