ACT – AURIX[™] Configuration Tool ATV MC July 2015





ACT – Intention

- The ACT was developed to:
 - □ Simplify pin mapping
 - Provides an overview over used/configured pins
 - Shows possible module connections and signal paths to the single pins/balls
 - Support PCB-design
 - Provide an interface to easily configure the iLLD
 - □ Have a single core OS



AURIX[™] Configuration Tool – ACT

ACT will be provided as a plugin for Tasking VX Toolset for Tricore from Altium

Free of charge!



Pin-Mapper



New Pin-Mapper project

TASKING Pin Mapper					
File Edit Navigate Search Project New Open File	ct Debug Windo Alt+Shift+N ▶	v Help [™] TASKING Pin Mapper Project [™] Project	L		TASKING Pin
Close Close All	Ctrl+W Ctrl+Shift+W	TASKING Pin Mapper Document	tive editor.		
Save Save As Save All	Ctrl+S Ctrl+Shift+S	T Other Ctrl+N	l		
Revert Move Rename Refresh Convert Line Delimiters To	F5	ve			
🖹 Print	C41+P				
Switch Workspace Restart	•				
i≥g Import i≥g Export					
Properties	Alt+Enter	ve			
1 mcs_sieve.src [gtm_mcs03_siev 2 TC29x.pincfg [TC29x] 3 TC275.pincfg [TC275] 4 TC267.pincfg [TC267]	e]				
Exit		∇			
] ∎≎		Wri	table Smart Insert	1:1	



Select TASKING Pin Mapper Project





Give the project a name

7 New TASKING Pin Mapper Pro	ject				<u>_ 🗆 ×</u>
Pin Mapper Project					
Project name must be specified					
Project name:					
Use default location					
Location: C:\eclipse_workspaces\	Tasking_VX-	toolset			Browse
		1			1
	< Back	Next >	Fir	nish	Cancel



Select the derivate and the package

77 New TASKING Pin Mapper	Project			
Device and Package Select device and package for t	he new pin mapp	er project		1
 □ Infineon □ AURIX Family □ TC26x8 □ BGA292 □ QFP144 □ QFP176 □ TC27xC □ BGA292 □ QFP176 □ TC29x8 □ BGA292 ○ TC29x8 □ BGA416 □ BGA516 				
?	< Back	Next >	Finish	Cancel



Open the pin-mapper

- Select the project in the project explorer on the left side
- Right click on the project



Overview

Search Project Debug Pin Mapper Window Help

Ports



Configuraiton

Package and Overview

C29x.pincfg 🛛				Package 🖾										📲 🕶 Ab
selection	Pin configuration			11121314	5 6 7	8 9 10 1	1 12 13	14 15	16 13	7 18 19	20 21	22 23	24 25 26	27 28 29 30
e filter text			Use tan: type new tag	A NO VECT NO. NO	P10 15P10 13P10 11	C N.C. N.C. P13	15P13 13P13 1	1 P13 9 P13	7 P13 5 N	P14 15P14 1	3P14 11 N.C.	P15 15P15 1	P15 11 N.C. N.C.	NC. NC. VDDP3 VSS
													-	
Ports	Module name:	ETH0		B N.C. VSS VEXT NO	_ P10_14 N.C. P10_10 P1	0_9 N.C. N.C. P13	_14P13_12P13_1	0 N.C. P13_	6 P13_4	P14_14P14_1	Z N.C. N.C.	P15_14P15_1	2P15_10 N.C. N.C.	N.C. VDDP3 VSS VSS
E - Analog	Description:	Ethernet module 0		C N.C. N.C.										
H-P01	Input			D N.C. N.C.										NC NC.
±-P02	MDI:	None		E NC NC										NC: NC
₽ 10														
+-P11 	1N2:	None	52	F PUZ_13PUZ_12	N.C. VEXT PI	0_7 P10_6 P10_2 P10	L_1 P10_0 P11_1	1 11 9 11	2 013 2.50	1 PI43 PI43	0 P14_1 P15_0	P15_4 P15_1	VD0P3 V35	
±-P13	CRS:	None	\Rightarrow	G P02_15P02_14	P02_0 VSS V	DKT P10_8 P10_5 P10	L4 P10_1 P11_1	2P11_10 P11_	3 P13_2 P13	LO P14_6 P14_	P14_4 P14_0	P15_3 VDDP3	VSS P15_0	N.C. N.C.
±-P14	COL:	None	0	H N.C. N.C.	P02_2 P02_1								P15_2 P20_14	VSS VSS
₽15				3 N.C. P01_0	P02_4 P02_3	VSS VFLEX P11	15P11_14 P11_	5 P11_6 P11_	4 P14_10 P14	0 P14,7 P15	P15_7 VDDFL	VSS	P20_12P20_13	VEBU VEBU
±-P20 = P21	1N5:	None	52				12 011 0 011 7		0 012 1 012	0.014.2.015	3		000 40000 44	P24 14724 41
₽ P22	RXER:	None	\Rightarrow	K MULI MULZ	P02,6 P02,5	P02_9 V55 P11	13 111 8 111	(P11_1 P11_	0 121 12	C0 P14_2 P15_	S VDDPL VSS	P20_9	P20_10P20_11	P24_14P24_15
₽23	RXD0:	None		L P01_8 P01_9	P02_8 P02_7	P02_11P02_10		-			ESRO	P20_6	P20_7 P20_8	P24_12P24_13
₽24	and the second se			M P01_11 P01_10	P00_0 P00_1	P01_4 P01_3	VDDV	D V <u>SS</u> _ V <u>SS</u>	VS5_ VS	S_ VDD	ESR1	PORST	P20_1 P20_3	P24_10 P24_11
± P25	RXD1:	None	52	N P01_13 P01_12	P00_2 P00_3	P01_6 P01_5	VDDVD	VSS_ VSS		s_ voo	P21_7	P21_6	P20_2 P20_0	P24_8 P24_5
±-P30	RXD2:	None						26 26	26 20	6				
±-P31	PXD3	None	-5	P POI_15POI_14	P00_4 P00_5	10005 1012/	*******	· ***	- V3-	V3- V3-	ICK	P21_1	P23 P23	Parts Part
<u>■</u> -P32	10051		~	R N.C. NC.	P00_7 P00_9	P00_8 P00_10	V <u>SS</u> 3024	VSS_ VSS 24 24	- V <u>SS</u> - V <u>S</u> 24 24	5 VSS N.C.	TMS	P21_0	P21_2 P21_4	P24_4 P24_5
H-P33	TXCLK:	None		T N.C. P00_13	P00_11P00_12	AN43 AN42	V55- V55-	V55- V55	- V <u>Ş</u> - V <u>Ş</u>	<u>s_ vss_ vss</u>	P22_10	P22_11	TRST VSS	P24_2 P24_3
₽40	Output			u P00_15P00_14	AN46 AN47	ANHI ANHO	VSS_ VSS_	VSS	VS5	VS5_ VS5_	P22_8	P22_9	XTAL2XTAL1	P24_0 P24_1
Peripherals	MDO0:	None			ANI44 ANI45		22 22	22	22	22 22 c voo			NOD 010002	NC NC
È ADC				V (11.2	CPINA PPINA	HAUTO HAUTO	000	21 21	- 21 2	1 100	P22_0	¥22_)	13	NG_ NG_
E ASCLINU	MDO 1:	None	52	w P40_13 P40_14	P40_9 P40_7	P40_4 AN34	VDD	VSS_ VSS 21 27	- V <u>SS</u> - VS 28 2	SVDD	P22_4	P22_5	P22_1 P22_0	P25_6 N.C.
E-ASCLIN2	MDO2:	None		Y P40_11 P40_12	P40_5 AN35	AN31 AN23					P23_7	P23_6	P22_3 P22_2	P25_14P25_15
E-ASCLIN3	MDO3:	None	0	AA P40_10 AN66	VAREFVAGND	AN30 AN22 AN	15 AN12 AN5	AN4 AN	VEVRSI P34	2 934 4 933	4 P32_5 VSS	P23_5	P23_3 P23_4	P25_12P25_17
E-CANO				ANES ANES	2 2	N.C. AN17 AN	14 4340 4347	4417 441	024 1 024	2 024 5 022 4	E 022 6 022 7	1/05	012 4 012 2	DOE 1000E 11
E CLIED	MDC:	None		HOMA COMA GA	A1125 A1120		14 MIG MIG	AND AND		0,00,000	5 1323 132	V33		
E-CCU61	TXER:	None 💌	\Rightarrow	AC AN53 AN52	P40_3 P40_2								VEXT P23_0	P25_8 P25_9
⊕- CIF	TXD0:	None	-	AD AN50 AN51	P40_1 P40_0 A	N19 AN18 AN16 AN	13 AN11 AN8	AN2 P33_	0 933_2 933	8_4 P33_6 P33_	9 933_10 933_12	VGATE P32_4	VSS VEXT	P25_7 P25_5
E Cerberus	TADOI	- Terre		AE AN59 AN58	N.C. ANZI A	N20 VSSM VDDM VAR	EF VAGND AN10	AN5 P33_	1 P33_3 P33	5 P33_7 P33_	P33_11P33_13	P32_0 P32_2	P32_3 VSS	P25_4 P25_3
E-E-Bay0	TXD1:	None		ANES ANET			1							D2E 2 02E 1
E-Ray1	TXD2:	None		AF AIO AIO										PO_2 PO_1
	TYD3.	None	-	AG N.C. N.C.										P26_0 P25_0
ETH	1403.			AH N.C. N.C.										VEXT VEBU
EIHO E- CPT	TXEN:	None	(D)	AJ N.C. N.C. N.C. AN	54 AN52 AN50 AN49 V	ISM VOOM VSS VFL	EXE P31_0 P31_2	2 P31_4 P31_	6 P31_8 P31	10P31_12P31_1	AVGATE P30_0	P30_2 P30_4	P30_6 P30_8 P30_10	P30_12P30_14 VSS VEXT
⊕ GTM				AN NO NO NO AN		TH NOON NOT NE	EVE 021 1 021 3	021 5 021	7 021 0 021	11021 12021 1	3P	2 020 2 020 2	020 7 020 0 020 11	1020 12020 15VE EVE VCC
					5 6 7	SM VOUM VSS VFL		14 15	15 1	7 18 19	20 21	73U 73U 73U 73	24 25 26	77 28 29 30
HSSL	-						TC		EIG (Tee	March				
±-12C0				Course the second			102	caxe - RG	4010 (10p	view)				
Conflicts S? E Consola			✓ □ A	Connection status:	Warning	ОК								
				-										
iption A	e Pin Location	Resource												
Modu	- Cocodoli													

O Infinos



If package is not shown

Open the right perspective





Package Overview – Different States

- Can display:
 - Module names
 - Symbolic names
 - Connection status
 - Pad classes
 - Power domains
 - Reset state

_				\searrow						
	<u> </u>	<u> </u>	_							
		<u> </u>	<u> </u>	_	0,	() ()	~*		Ab	
20	21	22	23	24	Q. 25	(±)		22	Ab	30
20	21 1 NC	22 P15.15	23 P15.13	24 P15.11	 ○ 25 № 	25 NC	27 NC	28 NC	29 VDDP3	30 VSS
20 14.1 NC	21 1 NC	22 P15.15 P15.14	23 P15.13 P15.12	24 P15.11 P15.10	0, 15 N N	25 NC	NC NC	28 NC VDDP3	29 VDDP3 VSS	
20 14.1 NC	21 1 NC	22 P15.15 P15.14	23 P15.13 P15.12	24 P15.11 P15.10	0 25 NC NC	25 NC NC	27 NC NC	28 NC VDDP3	29 VDDP3 VSS NC	30 VSS VSS NC



Configuration

Easily assign symbolic names to pins

Easily mark connections between modules and pins as Use-tags

Module/Pin selection Modul	e/Pin configuration		30 29 28 27 26	5 25 24 23 2
type filter text		Use tag: qspi0	AK VSS VFLEXE P30_ P30_ P30 15 13 11	0_ P30_9 P30_7 P30_5 P30
type filter text P13 P14 P14 P15 P20_0 P20_1 P20_2 P20_3 P20_6 P20_9 P20_10 P20_11 P20_11 P20_10 P20_11 P20_12 P20_13 P20_14 P40 P131 P25 P26 OUT: P31 P32 P33 P34 P40 AN1 AN1 AN1 AN1 AN2 AN3 	le name: P20_11 Jass: MP t state: PU1 r domain: VEXT olic name: Clock_QSPI0 nent: Clock_Output_QSPI0 tion: Output evel: CMOS/Automotive evel: CMOS/Automotive etrength: Speed grade 4 input :: Pull-up None ▼ output :: Push-pull : QSPI0_CLK ▼	Use tag: qspi0	N VSS VFLEX P30 P30 <td>1 P30.9 P30.7 P30.2 P30.2 P30.4 P30</td>	1 P30.9 P30.7 P30.2 P30.2 P30.4 P30

Copyright

Infind



Configuration

- Select the pin you want to use for the signal
- If two pins are selected for an uniqe signal, a warning is





After configuration

Generate .c and .h files if needed



And select the folder in the project where the files should be



Config-file itself

The configuration is stored in xml-like-format



Can be used for further processing

Next time open the file with Pin Configuration Editor again



ACT – Pin Mapper

- Shows all configured pins with possible errors and warnings
- Can display:
 - Module names
 - Symbolic names
 - Connection status
 - Pad classes
 - Power domains
 - Reset state

	30	29	28	77	26	25	24	23	22	21	20	19	18	17	16	15	14	13	17		10	9	8	7	6	5	4		2	1		
-			23	030	0.20	030.0	830 7	23	0.00 7	830.1	VER	19	18		16	15	14	13			10	VDDM	VEEN		-	-						
	135	TLEA	15	13	11		-30	- 30,3	1730,5	r su L	VILLEA	15	13	11	1369	rs.	r sL s		-34	VILLEA		VUUN	¥33M	AITHO	Andi	Anas	Anas		18.5	- m.c.	AL	
•	EXT	VSS	P30_ 14	P30_ 12	P30_ 10	P30_8	P30_6	P30_4	P30_2	P30_0	VGATE	P31_ 14	P31_ 12	P31_ 10	P31_8	P31_6	P31_4	P31_2	P31_0	VFLEX	e vss	VDDM	VSSM	AN49	ANSO	AN52	AN54	N.C.	N.C.	N.C.	LA	
	EBU	VEXT																											N.C.	N.C.	AH	
	25_0	P 26_0																											N.C.	N.C.	AG	
	25_1	P 25_2																											AN57	AN56	AF	
	25_3	P25_4				VSS	P32_3	P32_2	P32_0	P33_ 13	P33_	P33_9	P33_7	P33_5	P33_3	P33_1	ANS	AN10	VAGNE 1	VAREF	VDDM	VSSM	AN20	AN21	N.C.				AN58	AN59	AE	
	25_5	P25_7				VEXT	V55	P32_4	VGATE	P33_ 12	P33_ 10	P33_8	P33_6	P33_4	P33_2	P33_0	ANZ	ANS	AN11	AN13	AN16	ANIS	AN19	P40_0/	P40_1	1			AN61	ANGO	AD	
	25_9	P 25_8				P23_0	VEXT																	P40_2/	P40_3 AN27				AN62	AN63	AC	
	25_	P25_				P23_2	P23_1		VSS	P32_7	P32_6	P33_	P34_5	P34_3	P34_1	ANI	AN3	AN7	AN9	AN14	AN17	N.C.		ANZE	AN29				AN64	ANGS	AB	
	25	P 25_				P23_4	P23_3		P23_5	V55	P32_5	P33_	P34_4	P34_2	VEVRS	AND	AN4	ANG	AN12	AN15	AN22	AN30		VAGNO	VAREF				ANGG	P40_10	AA	
	25_	P 25_ 14				P 22_2	P22_3		P 23_6	P23_7											AN23	AN31		AN35	P40_5				P40_13 AN69	2P40_11 AN68	Y	
	K.C.	P 25_6					P22_1		P22_5	P 22_4			VDD	V55_	V55_	V55_	V55_	VDD			AN34	P40_4	-	P40_7/	P40_9				P40_14	P40_13	w	
	ч.с.	n.c.				VDDP3	VDD_9		0.22.7	P22_6		VDD		V55_	V55_	V55_	V55_		VDD		P40_8	P40_6		AN45	AN44				N.C.	N.C.	v	
	24_1	P 24_0				XTAL	XTALZ		P22_9	P 22_8		V55_	V55_		V55_	V55_		V55_	V55_		AN40	AN41		AN47	AN46				P00_	P00_	U	
	24.3	P24_2				VSS	TRST_		P22_	P22_10		V55_	V55_	155	V55_	V55_	V55_	V55_	V55_		AN42	AN43		P00_	P00_				P00_	N.C.	т	
	24_5	P24_4				P21_4	P21_2		P21_0	TMS		N.C.	V55_	V55_	V55_	V-1	V55_	V55_	V55_		P00_	P00_8		P00_9	P00_7				N.C.	N.C.	R	
	24.7	P24_6				P21_5	P21_3		P21_1	тск		V55_	V55_		V55_	V55_		V55_	25		P01_7	P00_6		P00_5	P00_4				P01_	P01_	p	
	24_9	P 24_8				P 20_0	P 20_2		P21_6	P21_7		VDD		V55_	V55_	V55_	V55_		VDDVD		P01_	P.01_6		P					P01_	P01_	N	
	24_	P24_				P20_3	P 20_1		PORST	ESR1_			VDD	V55_	V55_	V55_	V55_	VDDVD			P01_3	P01_4		- 0.1	100_0				P01_	P01_	м	
	24_	P24_				P20_8	P 20_7		P 20_6	ESRO_											P02_	P02_		-	-				P01_9	P01_8	L	
	24_	P24_				P20_	P 20_		P 20_9	V55	VDDFL	P15_5	P14_2	P12_0	P12_1	P11_0	P11_1	P11_7	P11_8	P11_	VSS	P02_9		P02_5	P02_6				P01_2	P01_1	к	
	EBU	VEBU				P20_	P20_		VSS	VDDFL	P15_7	P15_8	P14_7	P14_9	P14_	P11_4	P11_6	P11_5	P11_	P11_	VFLEX	vss		P02_3	P02_4				P01_0	N.C.	3	
	/55	VSS				P 20_	P15_2																	P02_1	P02_2				N.C.	N.C.	н	
	1.C.	N.C.				P15_0	V55	VDDP.	3 P15_3	P14_0	P14_4	P14_3	P14_6	P13_0	P13_2	P11_3	P11_	P11_	P10_1	P10_4	P10_5	P10_8	VEXT	VSS	P02_0				P02_	P02_	G	
	UC.	N.C.				VSS	VDDP	P15_1	P15_4	P15_6	P14_1	P14_5	P14_8	P13_1	P13_3	P11_2	P11_9	P11_	P10_0	P10_3	P10_2	P10_6	P10_7	VEXT	N.C.				P02_	P02_	F	
	I.C.	n.c.				9																							N.C.	N.C.	Ε	
	9.C.	N.C.																											N.C.	N.C.	D	
	9.C.	N.C.																											N.C.	H.C.	с	
	/55	VSS	VDDP3	N.C.	N.C.	N.C.	P15_	P15_	P15_	n.c.	H.C.	P14_	P14_	N.C.	P13_4	P13_6	N.C.	P13_	P13_	P13_	N.C.	N.C.	P10_9	P10_	N.C.	P10_	N.C.	VEXT	VSS	N.C.	8	
	/55	VDDP3	N.C.	N.C.	N.C.	N.C.	P15_	P15_	P15_	N.C.	P14_	P14_	P14_	N.C.	P13_5	P13_7	P13_9	P13_	P13_	P13_	N.C.	N.C.	N.C.	P10_	P10_	P10_	N.C.	N.C.	VEXT	N.C.	A	
	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1		
	onne	ection	status			Error				Info			1																			



ACT – Pin Mapper

Connection Status



Power Domain

| VSS
R.C.
R.C. | | <pre></pre> | VS5 | VDDP3 | P15_3 | 3
P14_0
P15_6 | P14_4
¥ | P14,3
P14,5 | P14_6 | 913,0
913,1 | P13_2
P13_3

 | РЦ 3
РЦ 2

 | P11_
10
P11_9
 | P11_
12
P11_
11

 | P10_1
P10_0 | P10_4
P10_3 | P10_5
P10_2 | P10_8
P10_6
 | VEXT
P10_7 | P02_1
VSS
VEXT | P02_2
P02_0
N.C. |
 | | | N.C.
P02_
14
P02_
12
N.C. | N.C.
P02
15
P02
13
N.C. |
|-------------------------------|-----------------------|----------------------------|------------|--|---|--|---|---|---|--
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---|---|--|
| VSS
N.C. | | P20_
14
P15_0
V55 | VDDP3 | VDDP3 | P15_3 | 3
P14_0
P15_6 | P14_4
¥14_1 | P14,3
P14,5 | P14_6
P14_8 | P13_0
P13_1 | P13_2
P13_3

 | P11_3
P11_2

 | P11_
10
P11_9
 | P11_
12
P11_
11

 | P10_1
P10_0 | P10_4
P10_3 | P10_5
P10_2 | P10_8
P10_6
 | VEXT
P10_7 | VSS
VEXT | P02_2
P02_0
N.C. |
 | | | N.C.
P02_
14
P02_
12 | P02
15
P02
13 |
| V55 | | P20_
14
P15_0 | P15_2 | VDDP3 | P15_3 | 3
P14_0 | P14_4 | P14_3 | P14_6 | P13_0 | P13_2

 | P11_3

 | P11_
10
 | P11_
12

 | P10_1 | P10_4 | P10_5 | P10_8
 | VEXT | P02_1 | P02_2 | | | | | | | | |
 | | | N.C.
P02_
14 | P02 |
| vss | | P20_14 | P15_2 | | | - | | | | |

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 | | | | | | | | | | | |
 | | P02_1 | P02_2 |
 | | | N.C. | 16.1 |
| | | | | | | 3 | | | | |

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 |

 | | | | |
 | | | |
 | | | | |
| VERU | | P20_ | P20_ | | VSS | VDDFL | P15_7 | P15_8 | P14,7 | P14_9 | P14_
10

 | P11_4

 | P11_6
 | P11_5

 | P11_
14 | P11_
15 | VFLEX | VSS
 | | P02_3 | P02_4 |
 | | | P01_0 | (11) |
| P24_
14 | | P 20_ | P20_
10 | | P 20_9 | VSS | VDDFL
3 | P15_5 | P14_2 | P12_0 | P12_1

 | P11_0

 | P11_1
 | P11,7

 | P11_8 | P11_
13 | V55 | P02_9
 | | P02_5 | P02_6 |
 | | | P01_2 | POI |
| 10
P24_ | | ¥ | ¥20_7 | | n
P20_6 | n
ESRO_ | | | | 26 | 26

 | 26

 | 26
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 | | | P02_ | P02_
 | | P02_7 | P02_8 |
 | | | 10
P01_9 | PO |
| P24_ | | P 20_3 | P20_1 | | PORST | ESR1_ | | | VDD | VSS_ | VSS_

 | VS5_

 | VSS_
 | VDDVD

 | | | P01_3 | P01_4
 | | P00_1 | P00_0 | | | | | | | | | | | | | | | | | | | | | | | | |
 | | | P01_ | PC |
| P24
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P24
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P24 | 2
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L P20_1 P20_1
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1 10 | P 20, 3 P 20, 1
P 20, 3 P 20, 1
P 20, 8 P 20, 7
P 20, 9 20, 1
P 20, 9 20, 1
10 | L P20,3 P20,1 P005
P20,3 P20,1 P005
P20,8 P20,7 P20,6
P20,8 P20,7 P20,6
P20,9 P20,9 P20,9
L P20, P20, P20,9
10 P20,9 P20,9
P20,9 P20,1 P20,9
P20,9 P20,1 P20,9
P20,9 P20,1 P20,9
P20,9 P20,1 P20,1 P20,9
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P20,9 P20,9 P20, | A Fall Fa | A Fails Fails Fails Fails Fails Fails L Fails Fails Fails Fails Fails L Fails Fails Fails Fails Fails L Fails Fai | S FALL FA | FALL FALL FALL FALL VOID L FALL FALL FALL VOID | FALL FALL FALL FALL FALL FALL FALL FALL FALL VOO VIE L FALL FALL FALL FALL VIE VIE <t< td=""><td>FALL FALL <th< td=""><td>FALL FALL <th< td=""><td>FALL FALL <th< td=""><td>FALL FALL FALL FALL VIO VIO</td><td>FALL FALL FALL FALL VIO Table Table VIO L FALL FALL VIO V</td><td>FALL FALL FALL FALL VID Table Table Table Tube L FALL FALL VID VID Table Table Table VID VID <</td><td>FALL FALL FALL FALL VID Table <thtable< th=""> <thtable< th=""> <thtable< t<="" td=""><td>x x</td><td>S FALL FALL FALL VID Table <thtable< th=""> <thtable< th=""> <thtable< th=""></thtable<></thtable<></thtable<></td><td>Company Pack Pack</td><td>Company Company <t< td=""><td>S FAD FAD FAD FAD F</td><td>S FALL FA</td><td>x x</td><td>C PRO_PRO_PRO_PRO_PRO_PRO_PRO_PRO_PRO_PRO_</td></t<></td></thtable<></thtable<></thtable<></td></th<></td></th<></td></th<></td></t<> | FALL FALL <th< td=""><td>FALL FALL <th< td=""><td>FALL FALL <th< td=""><td>FALL FALL FALL FALL VIO VIO</td><td>FALL FALL FALL FALL VIO Table Table VIO L FALL FALL VIO V</td><td>FALL FALL FALL FALL VID Table Table Table Tube L FALL FALL VID VID Table Table Table VID VID <</td><td>FALL FALL FALL FALL VID Table <thtable< th=""> <thtable< th=""> <thtable< t<="" td=""><td>x x</td><td>S FALL FALL FALL VID Table <thtable< th=""> <thtable< th=""> <thtable< th=""></thtable<></thtable<></thtable<></td><td>Company Pack Pack</td><td>Company Company <t< td=""><td>S FAD FAD FAD FAD F</td><td>S FALL FA</td><td>x x</td><td>C PRO_PRO_PRO_PRO_PRO_PRO_PRO_PRO_PRO_PRO_</td></t<></td></thtable<></thtable<></thtable<></td></th<></td></th<></td></th<> | FALL FALL <th< td=""><td>FALL FALL <th< td=""><td>FALL FALL FALL FALL VIO VIO</td><td>FALL FALL FALL FALL VIO Table Table VIO L FALL FALL VIO V</td><td>FALL FALL FALL FALL VID Table Table Table Tube L FALL FALL VID VID Table Table Table VID VID <</td><td>FALL FALL FALL FALL VID Table <thtable< th=""> <thtable< th=""> <thtable< t<="" td=""><td>x x</td><td>S FALL FALL FALL VID Table <thtable< th=""> <thtable< th=""> <thtable< th=""></thtable<></thtable<></thtable<></td><td>Company Pack Pack</td><td>Company Company <t< td=""><td>S FAD FAD FAD FAD F</td><td>S FALL FA</td><td>x x</td><td>C PRO_PRO_PRO_PRO_PRO_PRO_PRO_PRO_PRO_PRO_</td></t<></td></thtable<></thtable<></thtable<></td></th<></td></th<> | FALL FALL <th< td=""><td>FALL FALL FALL FALL VIO VIO</td><td>FALL FALL FALL FALL VIO Table Table VIO L FALL FALL VIO V</td><td>FALL FALL FALL FALL VID Table Table Table Tube L FALL FALL VID VID Table Table Table VID VID <</td><td>FALL FALL FALL FALL VID Table <thtable< th=""> <thtable< th=""> <thtable< t<="" td=""><td>x x</td><td>S FALL FALL FALL VID Table <thtable< th=""> <thtable< th=""> <thtable< th=""></thtable<></thtable<></thtable<></td><td>Company Pack Pack</td><td>Company Company <t< td=""><td>S FAD FAD FAD FAD F</td><td>S FALL FA</td><td>x x</td><td>C PRO_PRO_PRO_PRO_PRO_PRO_PRO_PRO_PRO_PRO_</td></t<></td></thtable<></thtable<></thtable<></td></th<> | FALL FALL FALL FALL VIO VIO | FALL FALL FALL FALL VIO Table Table VIO L FALL FALL VIO V | FALL FALL FALL FALL VID Table Table Table Tube L FALL FALL VID VID Table Table Table VID VID < | FALL FALL FALL FALL VID Table Table <thtable< th=""> <thtable< th=""> <thtable< t<="" td=""><td>x x</td><td>S FALL FALL FALL VID Table <thtable< th=""> <thtable< th=""> <thtable< th=""></thtable<></thtable<></thtable<></td><td>Company Pack Pack</td><td>Company Company <t< td=""><td>S FAD FAD FAD FAD F</td><td>S FALL FA</td><td>x x</td><td>C PRO_PRO_PRO_PRO_PRO_PRO_PRO_PRO_PRO_PRO_</td></t<></td></thtable<></thtable<></thtable<> | x x | S FALL FALL FALL VID Table Table <thtable< th=""> <thtable< th=""> <thtable< th=""></thtable<></thtable<></thtable<> | Company Pack Pack | Company Company <t< td=""><td>S FAD FAD FAD FAD F</td><td>S FALL FA</td><td>x x</td><td>C PRO_PRO_PRO_PRO_PRO_PRO_PRO_PRO_PRO_PRO_</td></t<> | S FAD FAD FAD FAD F | S FALL FA | x x | C PRO_PRO_PRO_PRO_PRO_PRO_PRO_PRO_PRO_PRO_ |

Pad Class



Reset State

neset	sudte:				HighZ				PU				1.4																
30 Reset	25	28	27	26	25	24	23	22	21	20	19	18	17 PX	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
VSS	VDDP3	N.C.	N.C.	N.C.	N.C.	P15_ 11	P15_ 13	P15_ 15	74.C.	P14_ 11	P14_ 13	P14_ 15	N.C.	P13_5	P13_7	P13_9	P13_ 11	P13_ 13	P13_ 15	N.C.	N.C.	N.C.	P10_ 11	P10_ 13	P10_ 15	N.C.	N.C.	VEXT	N.C.
VSS	VSS	VDDP3	N.C.	R.C.	N.C.	P15_ 10	P15_ 12	P15_ 14	N.C.	N.C.	P14_ 12	P14_ 14	N.C.	P13_4	P13_6	N.C.	P13_ 10	P13_ 12	P13_ 14	n.c.	N.C.	P10_9	P10_ 10	N.C.	P10_ 14	N.C.	VEXT	V55	N.C.
N.C.	N.C.																											N.C.	N.C.
N.C.	n.c.																											N.C.	N.C.
N.C.	N.C.																											N.C.	N.C.
N.C.	n.c.				VSS	VDDP:	P15_1	P15_4	P15_6	P14_1	P14_5	P14_8	P13_1	P13_3	P11_2	P11_9	P11_ 11	P10_0	P10_3	P10_2	P10_6	P10_7	VEXT	N.C.				P02_ 12	P02_ 13
N.C.	H.C.				P15_0	VSS	VDDP	3 P 15_3	P14_0	P14_4	P14_3	P14_6	P13_0	P13_2	P11_3	P11_ 10	P11_ 12	P10_1	P10_4	P10_5	P10_8	VEXT	VSS	P02_0				P02_ 14	P02_ 15
V55	VSS				P20_ 14	P15,3																	P02_1	P02_2				N.C.	N.C.
VEBU	VEBU				P20_	P20_		VSS	VDDFL 3	P15_7	P15_8	P14_7	P14_9	P14_ 10	P11_4	P11_6	P11_5	P11_ 14	P11_ 15	VFLEX	VSS		P02_3	P02_4				P01_0	N.C.
P24_ 15	P24_ 14				P20_ 11	P 20_ 10		P 20_9	V55	VDDFL 3	P15_5	P14_2	P12_0	P12_1	P11_0	P11_1	P11,7	P11_8	P11_ 13	VSS	P02_9		P02_5	P02_6				P01_2	P01_1
P24_ 13	P24_ 12				P20_8	P20_7		P 20_6	ESRO_											P02_ 10	P02_		P02_7	P02_8				P01_9	P01_8
P24_ 11	P24_ 10				P20_3	P 20_3		PORST	ESR1_			VDD	V55_ 26	V55_ 26	V55_ 26	V55_ 26	VDDVD	•		P01_3	P01_4		P00_1	P00_0				P01_ 10	P01_ 11
P24_9	P24_8				P 20_0	P 20_2		P21_6	P21_7		VDD		V55_ 26	26	V55_ 26	VS5_ 26		VDDVD		P01_5	P01_6		P00_3	P00_2				P01_ 12	P01_ 13



ACT – Pin Mapper

- After the configuration the target project for the setting has to be chosen
- The configuration is stored in xml-like-format

	₽	
	fptrap	-
	fssdemo	
	helloc	
-	hellocpp	
-	iLLD_software_platform	
	profiling	
	queens	
	sieve	
	squares	
	stack	
	tcpip	
	time	
	tsk_demo_tc27x	
±	tsk_demo_tc27x_with_ACT	
±	tsk_demo_tc29x_ACT_PinMapper	
·····	whets	





- iLLD come from tests and application used by several teams at infineon ATV
- iLLD are basic function low level drivers for use and demonstration for almost every module
- All drivers have the same code styling -> common look and feel
- Already tested in pre-silicone with a virtual prototype or in RTL-simulations
- Each derivate (TC2YX) has its own set of drivers
- No dependency between the peripheral drivers
- The strict iLLD coding guidelines allow layering of drivers for multi-dimensional system scenarios
- Available in the beta ACT-release (estimated Q2/15)







- Multifunctional drivers: Add a new peripheral and choose the iLLD for this module
 Application Software /
 - Right click in the
 window and add a
 new service or
 driver
 - Then you can choose the iLLD for the module





7/

ACT – Driver Configuration

Select the iLLD from a module and configure your parameters

Infinos

oftware Services	Device Stacks							
Software Platform Builder								
	ASCLIN ASC Interface IFX_ASCLIN_ASC_1	MULTICAN CAN Interface IFX_MULTICAN_CAN MULTICAN Peripheral MULTICAN	QSPI Master Interface IFX_QSPI_MASTER QSPI Peripheral	QSPI Sla Interfac IFX_QSPI QSPI Pe	ve e _SLAVE_1	STM Comparator IFX_STM_COMPARAT STM Peripheral		
	ASCLIN_0	MOLTICAN	Q3P1_0	Q3P1_2		51M_0		
n Conflicts 📮 Console 🔲 Properties 🔀	Call Hierarchy	Search						
PI Master Interface								
erty	Value		Type	Range	Prototype			
				i sunge /	1. ococype			
stack Item Options				(drige /	(indec)pe			
ID ID	IFX QSPI MA	STER 1		ixange /	in other pe			
ID ID SPI Interface	IFX_QSPI_MA	STER_1	STRUCT	indinge /	rototype			
ID SPI Interface Receive Interrupt Priority	IFX_QSPI_MA	STER_1	STRUCT UINT16	i kunge /	Auto	matically		
ID SPI Interface Receive Interrupt Priority Transmit Interrupt Priority	IFX_QSPI_MA 2 1	STER_1	STRUCT UINT16 UINT16	i kange y	Auto	matically	y cal	culat
ID SPI Interface Receive Interrupt Priority Transmit Interrupt Priority Error Interrupt Priority	IFX_QSPI_MA 2 1 0x30	STER_1	STRUCT UINT16 UINT16 UINT16	i tenge /	Auto	matically	y cal	culat
Stack Item Options ID SPI Interface Receive Interrupt Priority Transmit Interrupt Priority Error Interrupt Priority Type of Interrupt Priority	IFX_QSPI_MA 2 1 0x30 5xx0	STER_1	STRUCT UINT16 UINT16 UINT16	(reinge)	Auto	matically uency an	y calo nd pro	culat escal
ID ID SPI Interface Receive Interrupt Priority Transmit Interrupt Priority Error Interrupt Priority Type of Interrupt Service Maximum Channel Baudrate	IFX_QSPI_MA 2 1 0x30 Cpr0 10000000	STER_1	STRUCT UINT 16 UINT 16 UINT 16 SNUM UINT 32		Auto frequ	omatically uency an	y calo nd pro	culat escal
tack Item Options ID SPI Interface Receive Interrupt Priority Transmit Interrupt Priority Error Interrupt Priority Type of Interrupt Service Maximum Channel Baudrate	IFX_QSPI_MA 2 1 0x30 0x90 10000000 faise	STER_1	STRUCT UINT 16 UINT 16 UINT 16 EN M UINT 32 OCOLLAIN		Auto frequ for t	matically uency an he clock	y calo Id pro	culat escal ces
stack Item Options ID SPI Interface Receive Interrupt Priority Transmit Interrupt Priority Type of Interrupt Course Maximum Channel Baudrate Craoles Jelep Mode Pause On Baudrate Spike Errors	IFX_QSPI_MA 2 1 0x30 Crv0 10000000 false	STER_1	STRUCT UINT 16 UINT 16 UINT 16 UINT 16 ENUM UINT 32 BOOLEAN BOOLEAN		Auto frequ for t	matically uency an he clock	y calo Id pro -sour	culat escal ces
tack Item Options ID ID SPI Interface Receive Interrupt Priority Transmit Interrupt Priority Error Interrupt Priority Type of Interrupt Course Maximum Channel Baudrate Criabic Siecep Mode Pause On Baudrate Spike Errors Run or Pause Mode	IFX_QSPI_MA 2 1 0x30 Cove 1000000 Vaise false Pause	STER_1	STRUCT UINT16 UINT16 UINT16 ENUM UINT32 BOOLEAN ENUM		Auto frequ for t	matically uency an he clock	y calo Id pro -sour	culat escal ces
tack Item Options ID SPI Interface Receive Interrupt Priority Transmit Interrupt Priority Error Interrupt Priority Error Interrupt Priority Aximum Channel Baudrate Criate: Sietep Mode Pause On Baudrate Spike Errors Run or Pause Mode TX FIFO Interrupt Threshold	IFX_QSPI_MA 2 1 0x30 Cpv0 10000000 false False Pause 1	STER_1	STRUCT UINT 16 UINT 16 UINT 16 ENUM UINT 32 BOOLEAN BOOLEAN ENUM ENUM		Auto frequ for t	matically uency an he clock	y calo Id pro -sour	culat escal ces
tack Item Options ID SPI Interface SPI Interface rransmit Interrupt Priority Transmit Interrupt Priority Error Interrupt Priority Type of Interrupt Service Maximum Channel Baudrate Chable Sleep Mode Pause On Baudrate Spike Errors Run or Pause Mode TX FIFO Interrupt Threshold RX FIFO Interrupt Threshold RX FIFO Interrupt Threshold	IFX_QSPI_MA 2 1 0x30 Cru0 10000000 faise faise Pause 1 1 0	STER_1	STRUCT UINT 16 UINT 16 UINT 16 ENUM UINT 32 BOOLEAN BOOLEAN ENUM ENUM		Auto frequ for t	matically uency an he clock	y calo Id pro -sour	culat escal ces
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stack Item Options ID ID SPI Interface Receive Interrupt Priority Transmit Interrupt Priority Error Interrupt Priority Type of Interrupt Censics Maximum Channel Baudrate Chalors Sietep Mode Pause On Baudrate Spike Errors Run or Pause Mode TX FIFO Interrupt Threshold RX FIFO Interrupt Threshold Enabled Interrupts TX Interrupt RX Interrupt PX Interrupt PT I Interrupt	IFX_QSPI_MA 2 1 0x30 Cpu0 10000000 Taise false Pause 1 0 0 true true false	STER_1	STRUCT UINT 16 UINT 16 UINT 16 ENUM BOOLEAN ENUM ENUM ENUM STRUCT BOOLEAN BOOLEAN BOOLEAN BOOLEAN BOOLEAN		Auto frequ for t	omatically uency an he clock	y calo id pro -sour	culat escal ces
tack Item Options ID ID SPI Interface Receive Interrupt Priority Transmit Interrupt Priority Error Interrupt Priority Type of Interrupt Priority Maximum Channel Baudrate Chable Sleep Mode Pause On Baudrate Spike Errors Run or Pause Mode TX FIFO Interrupt Threshold RX FIFO Interrupt Threshold RX FIFO Interrupt Threshold Enabled Interrupts TX Interrupt RX Interrupt RX Interrupt PT1 Interrupt PT2 Interrupt PT2 Interrupt	IFX_QSPI_MA 2 1 0x30 cpu0 10000000 raise false Pause 1 1 0 true true false false false	STER_1	STRUCT UINT 16 UINT 16 EN M UINT 32 BOOLEAN BOOLEAN ENUM ENUM ENUM ENUM ENUM STRUCT BOOLEAN BOOLEAN BOOLEAN BOOLEAN BOOLEAN		Auto frequ for t	omatically uency an he clock- setup	y calo id pro -sour	culat escal ces
stack Item Options ID SPI Interface Receive Interrupt Priority Transmit Interrupt Priority Error Interrupt Priority Error Interrupt Priority Maximum Channel Baudrate Drable Sleep Mode Pause On Baudrate Spike Errors Run or Pause Mode TK FIFO Interrupt Threshold RX FIFO Interrupt Threshold Enabled Interrupt TX Interrupt PT1 Interrupt PT1 Interrupt PT2 Interrupt UPD Interrupt	IFX_QSPI_MA 2 1 0x30 cpu0 10000000 taise faise faise Pause 1 0 0 true true faise faise faise faise	STER_1	STRUCT UINT 16 UINT 16 UINT 16 UINT 16 ENUM BOOLEAN BOOLEAN BOOLEAN BOOLEAN BOOLEAN BOOLEAN BOOLEAN BOOLEAN BOOLEAN		Auto frequ for t	omatically uency an he clock- setup	y calo nd pro -sour	culat escal ces
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stack Item Options ID SPI Interface Receive Interrupt Priority Transmit Interrupt Priority Error Interrupt Priority Type of Interrupt Priority Type of Interrupt Priority Maximum Channel Baudrate Chaloe sleep Mode Pause On Baudrate Spike Errors Run or Pause Mode TX FIFO Interrupt Threshold Enabled Interrupt Threshold Enabled Interrupt TX Interrupt PT1 Interrupt PT2 Interrupt USD Interrupt USD Interrupt DMA Configuration Use DMA	IFX_QSPI_MA 2 1 0x30 Cpu0 10000000 Vaise false false Pause 1 0 true true false false false false false	STER_1	STRUCT UINT 16 UINT 16 UINT 16 UINT 2 BOOLEAN BOOLEAN ENUM ENUM ENUM STRUCT BOOLEAN BOOLEAN BOOLEAN BOOLEAN BOOLEAN BOOLEAN STRUCT BOOLEAN		Auto frequ for t Can s	omatically uency an he clock- setup	y calo id pro-sour	culat escal
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ACT – Generated Struct

• E. g., for QSPI Master, the generated init-struct is

Property	Value
Stack Item Options	
ID	IFX_QSPI_MASTER_1
SPI Interface	
Receive Interrupt Priority	2
Transmit Interrupt Priority	1
Error Interrupt Priority	0x30
Type of Interrupt Service	Cpu0
Maximum Channel Baudrate	1000000
Enable Sleep Mode	false
Pause On Baudrate Spike Errors	false
Run or Pause Mode	Pause
TX FIFO Interrupt Threshold	1
RX FIFO Interrupt Threshold	0
 Enabled Interrupts 	
TX Interrupt	true
RX Interrupt	true
PT1 Interrupt	false
PT2 Interrupt	false
USR Interrupt	false
 DMA Configuration 	
Use DMA	false

* Software Platform Generated File
*
*/

#include "ifx_qspi_master_cfg_instance.h"

const ifx_qspi_master_cfg_instance_t ifx_qspi_master_instance_table[1] =





ACT – OS



OS – With Respect To The TASKING OS

- 3 stage implementation:
 - Configurator
 - Generates an oil-file
 - OIL compiler
 - Generates c- and h-files
 - Normal compiler+linker
 - Generates the hex-/elf-file





OS – Create the Config

■ Select File □ New



And create the oil-file



OS – OIL-Configurator

Object / Attribute	Value		Туре	Description
🕀 🧿 OS	New_OS OS	-routines		
APPMODE	APPMODE1			
🗄 🚺 TASK	T1			
🗄 🚺 TASK	T2			
🗄 🚺 TASK	тз аз	sk-config		
🗄 🚺 TASK	T4			
🗄 🚺 TASK	T5			
🗄 🚺 TASK	T6			
🗄 🚺 TASK	T7			
🗄 🌍 TASK	T8			
E 🚯 ISR	Taster 1ISR			
🗄 🚯 ISR	Taster 2ISR			
🗄 🚯 ISR	Taster 3ISR			
🗄 🚯 ISR	Taster4ISR			
O COUNTER	SYSTEM COUNTER			System timer counter
🕀 🔕 ALARM	A1			
🗄 🔕 ALARM	A2	C .		
🗄 🔕 ALARM	Alar Alar	m-config		
🗄 🔕 ALARM	A4			
🗄 🔕 ALARM	A5			
🗄 🔕 ALARM	A6			
🗄 🔕 ALARM	A7			
E 🔕 ALARM	AS			
EVENT	E1 EVO	nt-config		
G EVENT	F2 LVC	nt-conng		
E 🔞 RESOURCE	R1 Do	courco-confi	a	
E 🔞 RESOURCE	R2 RE	source-conn	y	
RESOURCE	RES_SCHEDULER	RES_SCHEDULER		System scheduler resource
F O COM	New_COM			
🕀 🕲 MESSAGE	M1	seage config		
🕀 🔕 MESSAGE	M2 MES	saye-comig		



OS – Basic Configuration

	oş	New_OS		➤ Task-config
STATUS STARTUPHOOK		EXTENDED	ENUM	rack comig
		TRUE	BOOLEAN	
	ERRORHOOK	FALSE	BOOLEAN	
	SHUTDOWNHOOK	FALSE	BOOLEAN	
	PRETASKHOOK	FALSE	BOOLEAN	
	POSTTASKHOOK	FALSE	BOOLEAN	Used hook-routines
	USEGETSERVICEID	FALSE	BOOLEAN	
	USEPARAMETERACCESS	FALSE	BOOLEAN	
	USERESSCHEDULER	TRUE	BOOLEAN	
	LONGMSG	FALSE	BOOLEAN	
	ORTI	FALSE	BOOLEAN	
	RUNLEVELCHECK	FALSE	BOOLEAN	
	SHUTDOWNRETURN	FALSE	BOOLEAN	
	IDLEHOOK	FALSE	BOOLEAN	
	IDLELOWPOWER	FALSE	BOOLEAN	
Ξ	USERTOSTIMER	TRUE	BOOLEAN	
	RTOSTIMERPRIO	1	UINT32 [1255]	
	RTOSTIMER	T6	ENUM	
	OSCLOCKHZ	10	UINT32 [1100000]	
	CPUCLOCKMHZ	200	UINT32 [1400]	

OS – Alarm Configuration







OS – Task Configuration



T1		Proomntiv/non	
1	UINT32 [1254]	Freeinpuv/non	
FULL	ENUM	preemptive scheduling	
1	UINT32 [1255]		
FALSE	BOOLEAN	Resource assignment	
[RES_SCHEDULER, R1]	RESOURCE_TYPE		
[E1]	EVENT_TYPE	→ Event assignment	
[M2]	MESSAGE_TYPE	Moccogo accignment	
250	UINT32	Message assignment	
	T1 1 FULL 1 FALSE [RES_SCHEDULER, R1] [E1] [M2] 250	T1 UINT32 [1254] 1 UINT32 [1254] FULL ENUM 1 UINT32 [1255] FALSE BOOLEAN [RES_SCHEDULER, R1] RESOURCE_TYPE [E1] EVENT_TYPE [M2] MESSAGE_TYPE 250 UINT32	



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