

ACT – AURIX™ Configuration Tool

ATV MC
July 2015



ACT – Intention

- The ACT was developed to:
 - Simplify pin mapping
 - Provides an overview over used/configured pins
 - Shows possible module connections and signal paths to the single pins/balls
 - Support PCB-design
 - Provide an interface to easily configure the iLLD
 - Have a single core OS

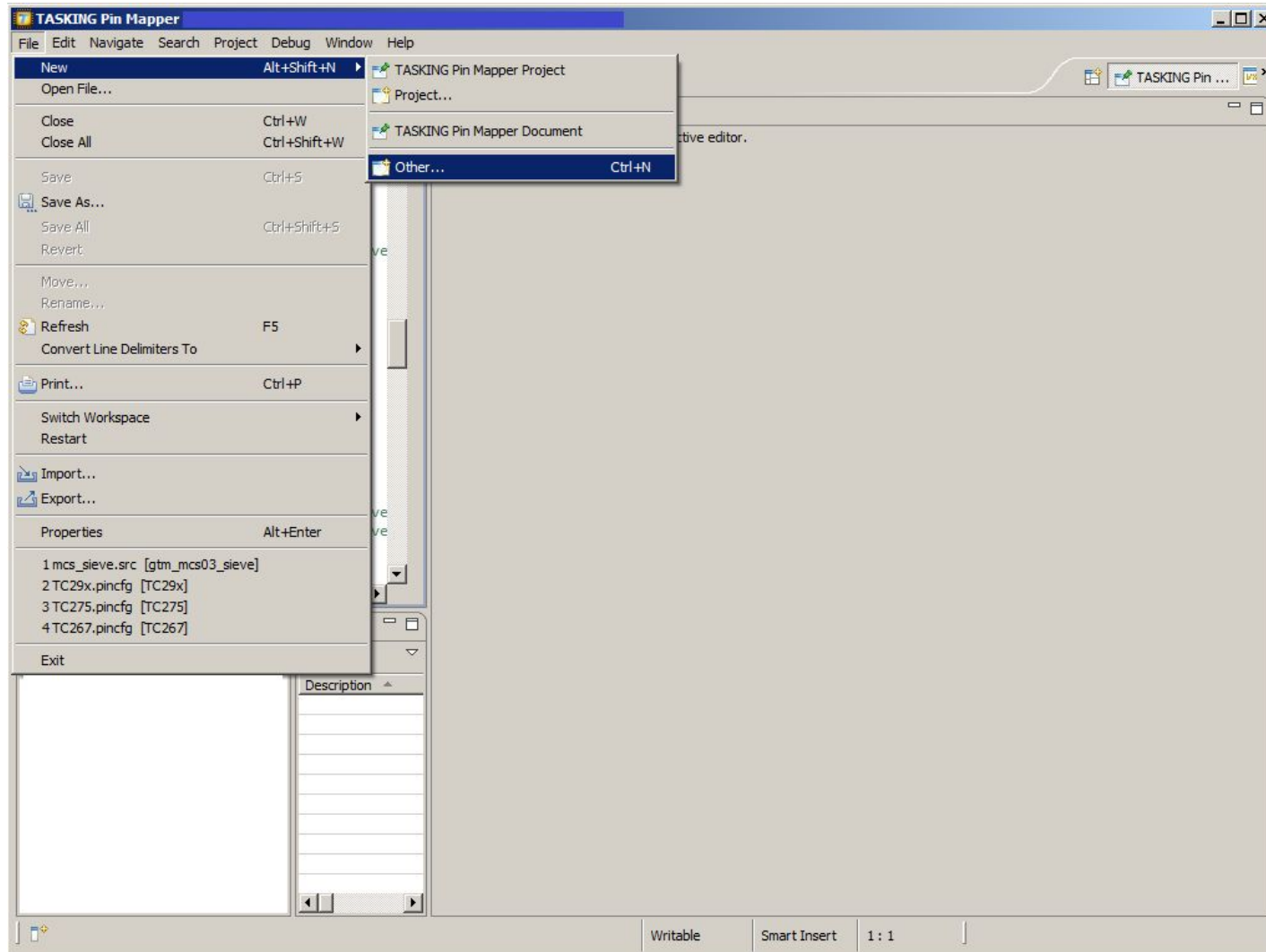
AURIX™ Configuration Tool – ACT

- ACT will be provided as a plugin for Tasking VX Toolset for Tricore from Altium

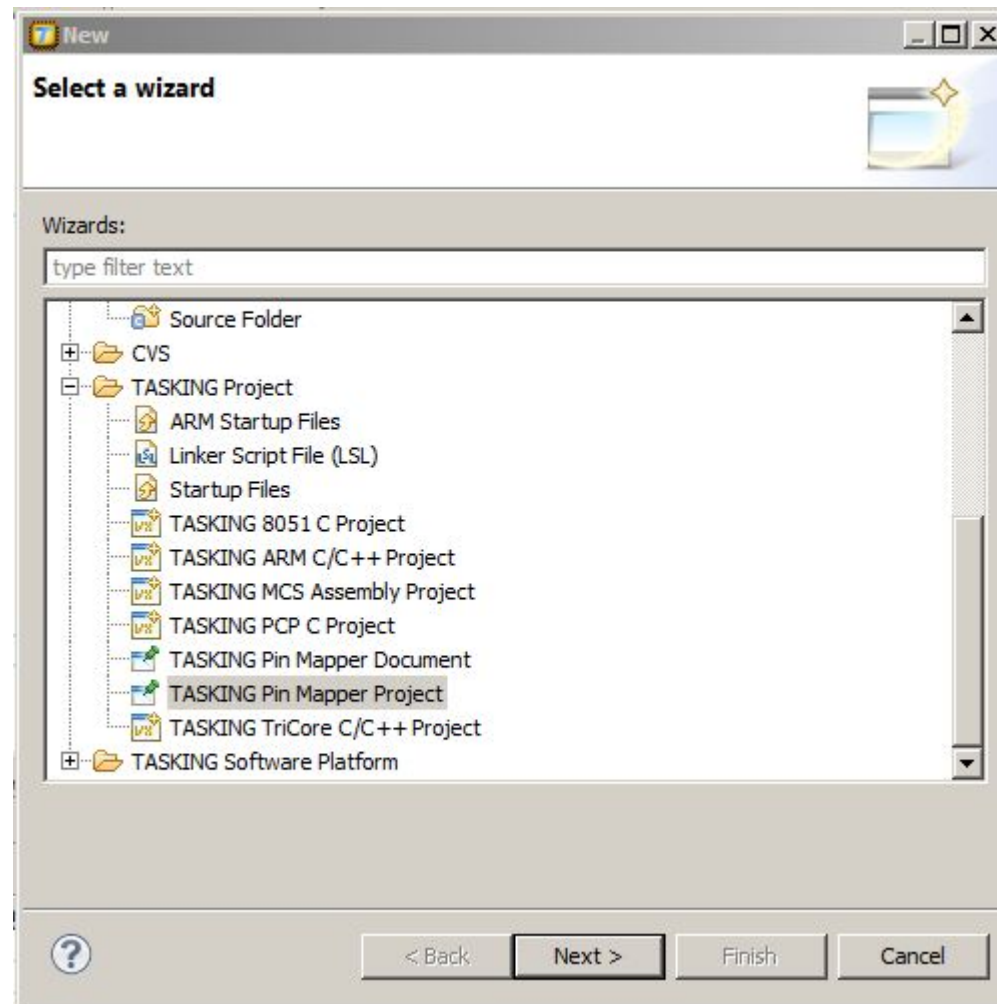
Free of charge!

Pin-Mapper

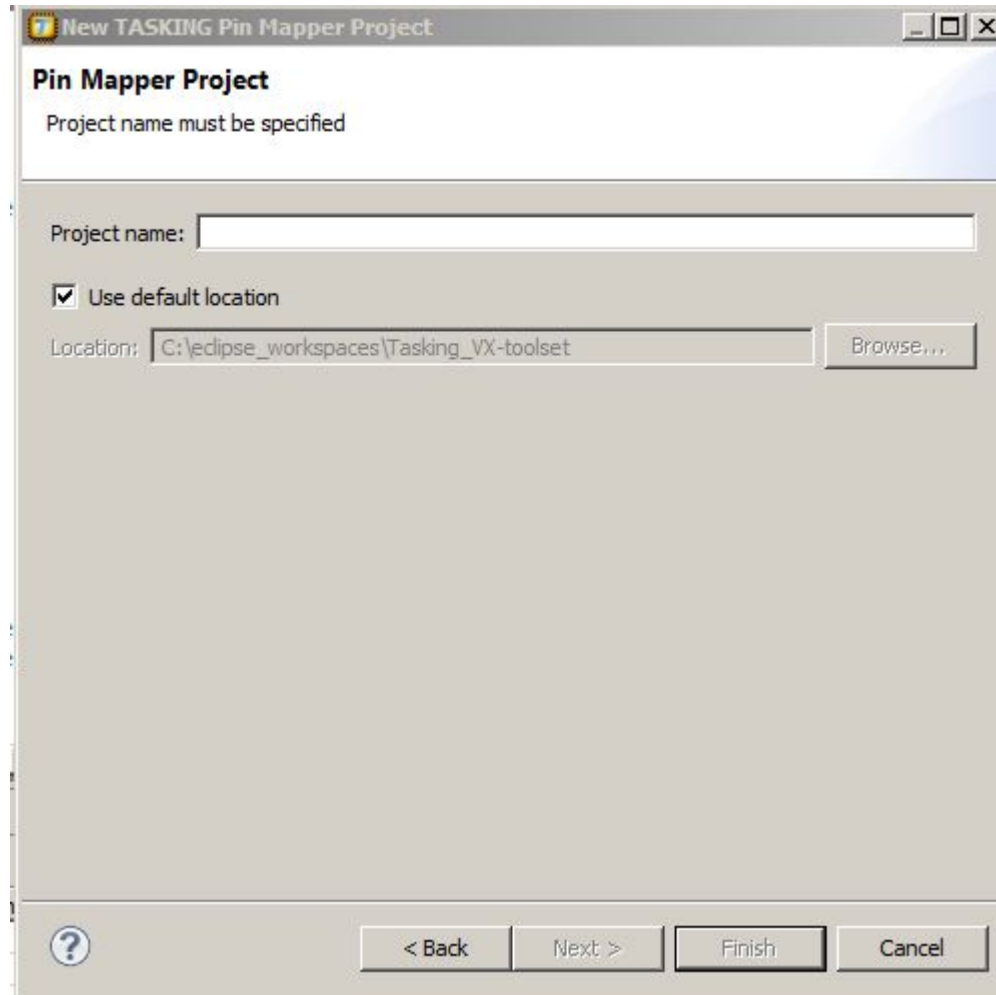
New Pin-Mapper project



Select TASKING Pin Mapper Project



Give the project a name



New TASKING Pin Mapper Project

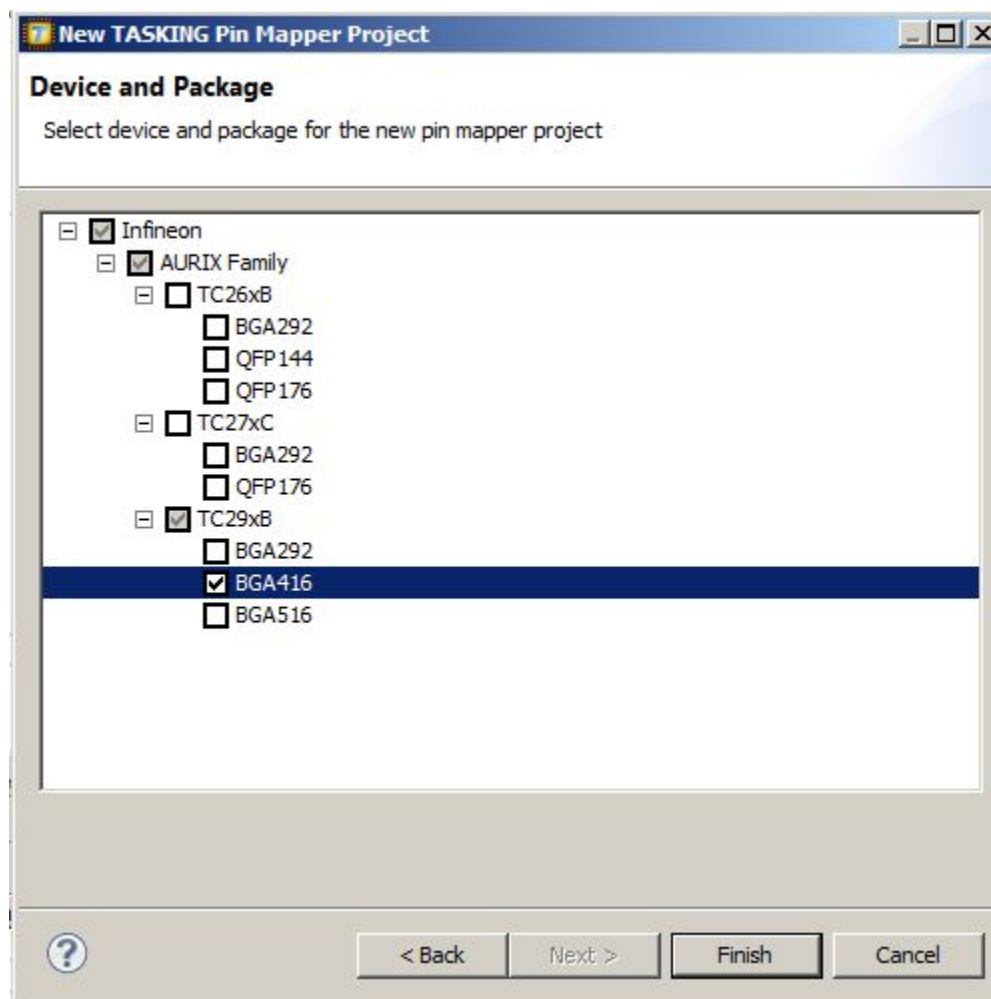
Pin Mapper Project
Project name must be specified

Project name:

☒ Use default location

Location:

Select the derivate and the package



Open the pin-mapper

- Select the project in the project explorer on the left side
- Right click on the project



Overview

Ports

Configuraiton

Package and Overview

The screenshot displays the Infineon Pin Manager software interface, divided into two main panes: Pin configuration and Package overview.

Pin configuration pane (Left):

- Pin selection:** A list of pins categorized by function:
 - Ports:** P00, P01, P02, P10, P11, P12, P13, P14, P15, P20, P21, P22, P23, P24, P25, P26, P30, P31, P32, P33, P34, P40.
 - Peripherals:** ADC, ASCLIN0, ASCLIN1, ASCLIN2, ASCLIN3, CAN0, CAN1, CCU60, CCU61, CIF, Cerberus, DSADC, E-Ray0, E-Ray1, EBU, ETH, GPT, GTM, HSM, HSSL, I2C0.
- Pin configuration:** A table for configuring pins for the **ETH0** module (Ethernet module 0).

Module name:	ETH0
Description:	Ethernet module 0
Input	
MDI:	None
IN2:	None
CRS:	None
COL:	None
IN5:	None
RXER:	None
RXDO:	None
RXD1:	None
RXD2:	None
RXD3:	None
TXCLK:	None
Output	
MDO0:	None
MDO1:	None
MDO2:	None
MDO3:	None
MDC:	None
TXER:	None
TXDO:	None
TXD1:	None
TXD2:	None
TXD3:	None
TXEN:	None

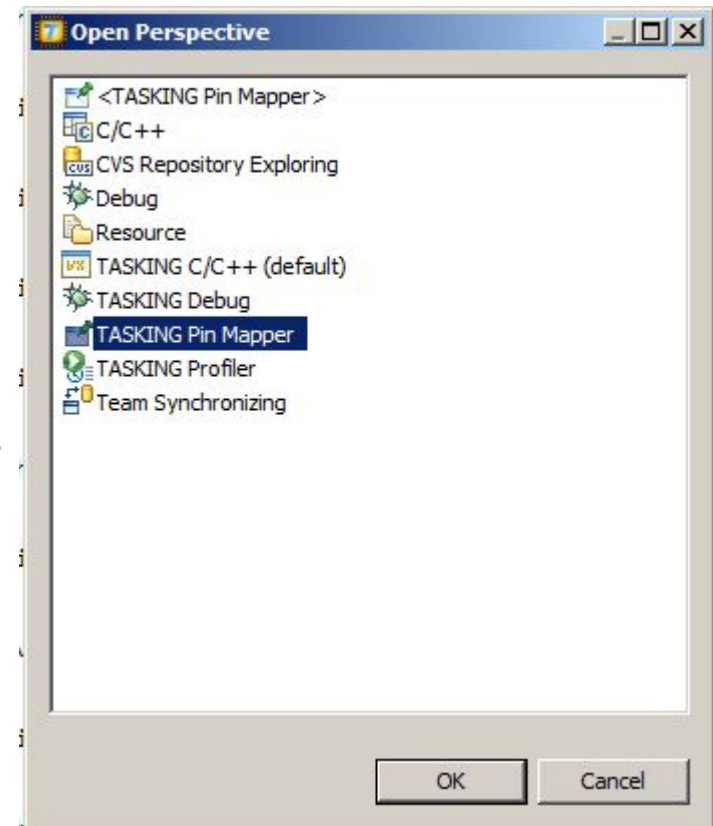
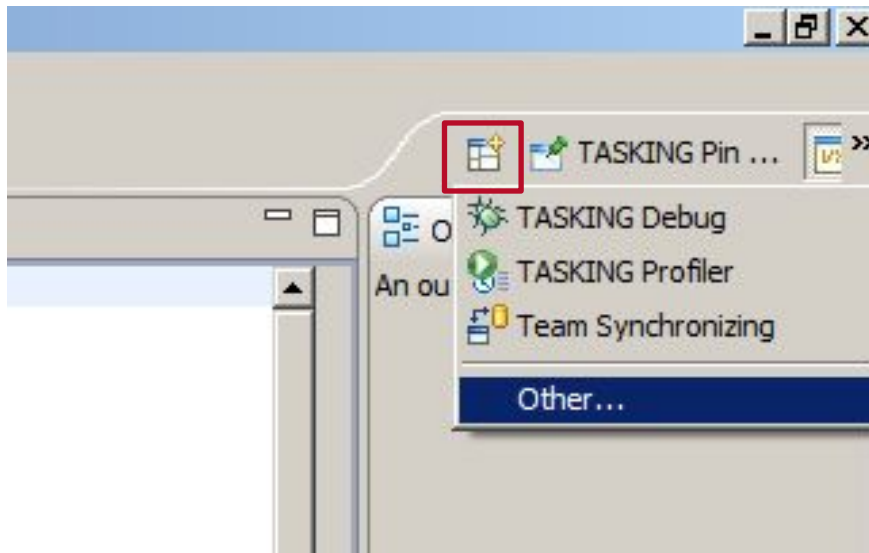
Package overview pane (Right):

- Package:** TC29x8 - BGA516 (Top View)
- Connection status:**
 - Error (Pink)
 - Warning (Orange)
 - OK (Green)
- Pin List:** A table showing the pin list for the package, including pin number, name, and location.

Pin	Name	Location
1	NC	
2	VBXT	
3	NC	
4	NC	
5	P10_15P10_13P10_11	
6	NC	
7	NC	
8	NC	
9	P13_15P13_13P13_11	
10	P13_9	
11	P13_7	
12	P13_5	
13	NC	
14	P14_15P14_13P14_11	
15	NC	
16	P15_15P15_13P15_11	
17	NC	
18	NC	
19	NC	
20	VDDP3	
21	VSS	
22	VSS	
23	NC	
24	NC	
25	NC	
26	NC	
27	NC	
28	NC	
29	NC	
30	NC	

If package is not shown

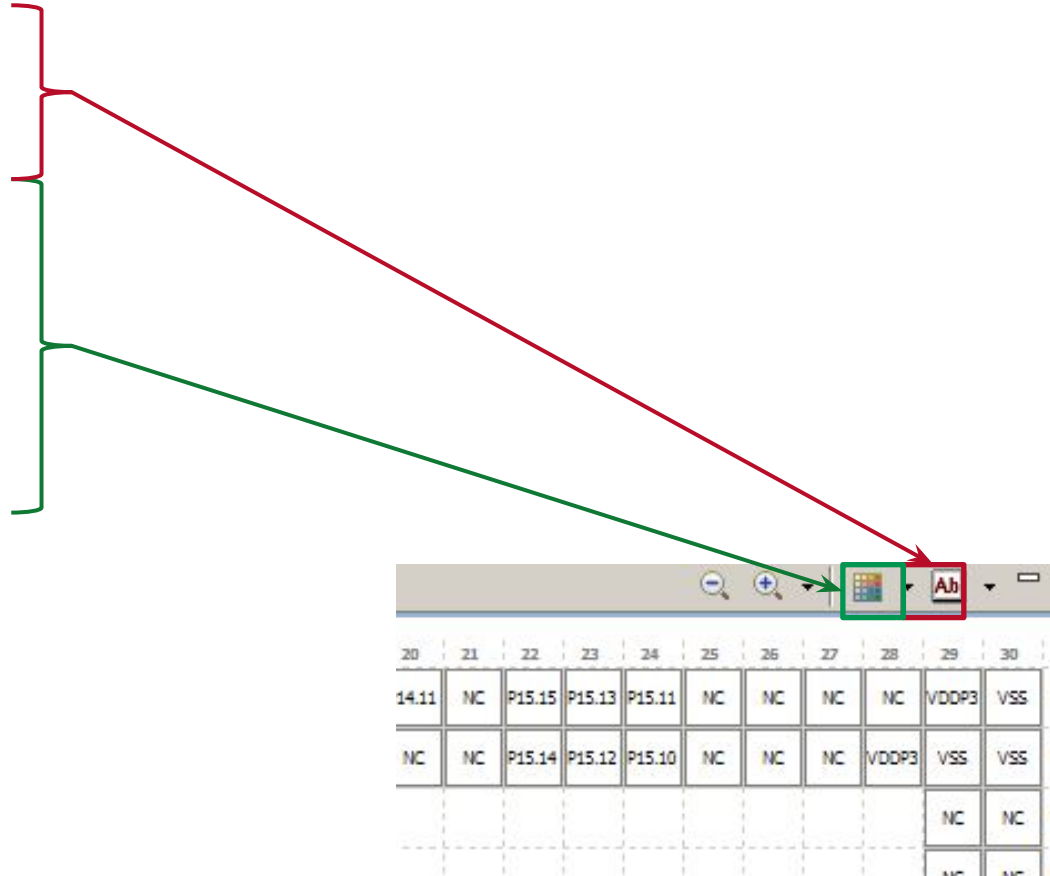
- Open the right perspective



Package Overview – Different States

■ Can display:

- ☐ Module names
- ☐ Symbolic names
- ☐ Connection status
- ☐ Pad classes
- ☐ Power domains
- ☐ Reset state



Configuration

- Easily assign symbolic names to pins
- Easily mark connections between modules and pins as Use-tags

The screenshot displays the Infineon Pin Manager software interface, divided into three main sections:

- Module/Pin selection:** A tree view on the left showing the hierarchy of pins. P20_11 is selected and highlighted in blue.
- Module/Pin configuration:** A central panel for configuring the selected pin.
 - Module name:** P20_11
 - Pad class:** MP
 - Reset state:** PU1
 - Power domain:** VEXT
 - Symbolic name:** Clock_QSPI0 (highlighted with a red box)
 - Comment:** Clock_Output_QSPI0
 - Direction:** Output
 - Pad level:** CMOS/Automotive
 - Pad strength:** Speed grade 4
 - Chip input:** Mode: Pull-up, IN: None
 - Chip output:** Mode: Push-pull, OUT: QSPI0_CLK (checked)
- Use-tag:** A dropdown menu at the top right of the configuration panel is set to "qspi0" (highlighted with a green box).

Annotations on the image include:

- A red arrow pointing from the "Symbolic name" field to the "Clock_QSPI0" entry in the pin list on the right.
- A green arrow pointing from the "Use tag" dropdown to a green circle labeled "qspi0" in the pin list.
- A red circle highlights the "Clock_QSPI0" entry in the pin list, which has a checkmark next to it.

On the right side, a portion of the pin list is visible, showing pins 30 through 22. The "Clock_QSPI0" entry is highlighted in green.

Configuration

- Select the pin you want to use for the signal
- If two pins are selected for an unique signal, a warning is displayed

Module/Pin selection

type filter text

- Port
- CCU
- GTM
- VADC
- QSPI
 - QSPI0_0
 - QSPI0_1
 - QSPI0_2
 - QSPI0_3
 - QSPI0_4
 - QSPI0_5
- DSADC
- HSSL
- ETH
- SCU
- STM
- CAN
- IOM
- MSC
- GPT
- ASCLIN
- Others

Module/Pin configuration

Use tag: qspi0

Module name: QSPI0_0

Input

IN: ☒ P20_12.IN

Output

QSPI0_OUT: ☒ Select... ☐ P20_12.OUT ☐ P20_13.OUT ☐ P22_5.OUT ☐ P22_10.OUT ☐ P22_7.OUT ☐ P22_8.OUT

QSPI0_CLK: ☒ Select... ☐ P20_11.OUT ☐ P20_13.OUT

QSPI0_SEL0: None

QSPI0_SEL1: None

QSPI0_SEL2: None

QSPI0_SEL3: None

QSPI0_SEL4: None

Pin Conflicts

0 errors, 1 warning, 0 others

Description	Module	Pin	Configurat...	Location	Resource	Path
Multiple selections for a 1-to-N connection	QSPI0_0	QSPI0_CLK	QSPI0_CLK	N.A.	tsk_demo...	/tsk_demo_tc29...

After configuration

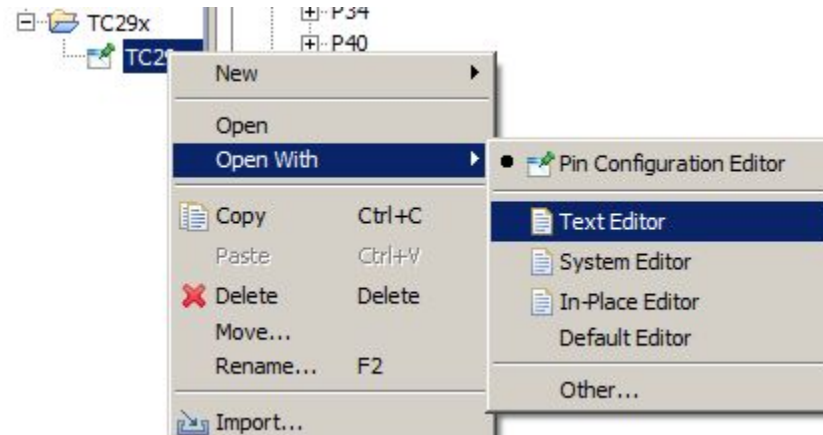
- Generate .c and .h files if needed



- And select the folder in the project where the files should be

Config-file itself

- The configuration is stored in xml-like-format



- Can be used for further processing

- Next time open the file with Pin Configuration Editor again

ACT – Pin Mapper

- Shows all configured pins with possible errors and warnings

- Can display:

- Module names
- Symbolic names
- Connection status
- Pad classes
- Power domains
- Reset state

Package - TC29x - BGA516

	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1									
AK	VSS	VFLX1	P30_15	P30_13	P30_11	P30_9	P30_7	P30_5	P30_3	P30_1	VFLX1	P31_15	P31_13	P31_11	P31_9	P31_7	P31_5	P31_3	P31_1	VFLX1	VSS	VDDH	VSSM	AN48	AN51	AN53	AN55	N.C.	N.C.	N.C.	AK								
AJ	VEXT	VSS	P30_14	P30_12	P30_10	P30_8	P30_6	P30_4	P30_2	P30_0	VGATE	P31_14	P31_12	P31_10	P31_8	P31_6	P31_4	P31_2	P31_0	VFLX1	VSS	VDDH	VSSM	AN49	AN50	AN52	AN54	N.C.	N.C.	N.C.	AJ								
AH	VEBU	VEXT																											N.C.	N.C.	AH								
AG	P25_0	P25_0																											N.C.	N.C.	AG								
AF	P25_1	P25_2																													AN57	AN56	AF						
AE	P25_3	P25_4				VSS	P32_3	P32_2	P32_0	P31_13	P31_11	P31_9	P31_7	P31_5	P31_3	P31_1	AN5	AN10	VAGNDVAREF	VDDH	VSSM	AN20	AN21	N.C.							AN58	AN59	AE						
AD	P25_5	P25_7				VEXT	VSS	P32_4	VGATE	1P	P33_12	P33_10	P33_8	P33_6	P33_4	P33_2	P33_0	AN2	AN6	AN11	AN13	AN16	AN18	AN19	P40_0/P40_1/AN24						AN61	AN60	AD						
AC	P25_9	P25_8				P23_0	VEXT																		P40_2/P40_3/AN26						AN62	AN63	AC						
AB	P25_11	P25_10				P23_2	P23_1		VSS	P32_7	P32_6	P31_15	P34_5	P34_3	P34_1	AN1	AN3	AN7	AN9	AN14	AN17	N.C.									AN64	AN65	AB						
AA	P25_12	P25_11				P23_4	P23_3		P23_5	VSS	P32_5	P31_14	P34_4	P34_2	VEVRH	AND	AN4	AN6	AN12	AN15	AN22	AN30			VAGNDVAREF						AN66	P40_10	AA						
Y	P25_15	P25_14				P22_2	P22_3		P23_6	P23_7																						P40_13/P40_11/AN68		Y					
W	N.C.	P25_6				P22_0	P22_1		P22_5	P22_4			VDD	VSS_21	VSS_20	VSS_27	VSS_21	VDD														P40_14/P40_13/AN71		W					
V	N.C.	N.C.				VDDP3/VDD_9	13		P22_7	P22_6			VDD	VSS_21	VSS_21	VSS_21	VSS_21	VDD															N.C.	N.C.	V				
U	P24_1	P24_0				XTAL1	XTAL2		P22_9	P22_8			VSS_22	VSS_22	VSS_22	VSS_22	VSS_22																P00_10	P00_15	U				
T	P24_3	P24_2				VSS	TRST_n		P22_11	P22_10			VSS_23	VSS_23	VSS_23	VSS_23	VSS_23	VSS_23																P00_13	N.C.	T			
R	P24_5	P24_4				P21_4	P21_2		P21_0	TMS			N.C.	VSS_24	VSS_24	VSS_24	VSS_24	VSS_24																N.C.	N.C.	R			
P	P24_7	P24_6				P21_5	P21_3		P21_1	TCK			VSS_25	VSS_25	VSS_25	VSS_25	VSS_25	VSS_25																P01_15	P01_14	P			
N	P24_9	P24_8				P20_9	P20_2		P21_6	P21_7			VDD	VSS_26	VSS_26	VSS_26	VSS_26	VDDVD																P01_12	P01_13	N			
M	P24_11	P24_10				P20_3	P20_1		PORST_ERST_n				VDD	VSS_26	VSS_26	VSS_26	VSS_26	VDDVD																P01_10	P01_11	M			
L	P24_13	P24_12				P20_8	P20_7		P20_6	ESR0_n																									P01_9	P01_8	L		
K	P24_15	P24_14				P20_9	P20_10		P20_8	VSS	VDDP3/P15_5	P14_3	P12_0	P12_1	P11_0	P11_1	P11_7	P11_8	P11_13	VSS	P02_9														P01_7	P01_6	K		
J	VEBU	VEBU				P20_13	P20_12		VSS	VDDP3/P15_7	P15_8	P14_7	P14_9	P14_10	P11_4	P11_6	P11_5	P11_15	P11_14	VFLX1	VSS															P01_5	N.C.	J	
H	VSS	VSS				P20_15	P20_14		P20_15	P20_12																											P01_4	P01_3	H
G	N.C.	N.C.				P15_0	VSS	VDDP3/P15_3	P14_0	P14_4	P14_5	P14_6	P13_0	P13_2	P11_3	P11_10	P11_12	P10_1	P10_4	P10_5	P10_8	VEXT	VSS	P02_0												P02_14	P02_15	G	
F	N.C.	N.C.				VSS	VDDP3/P15_1	P15_4	P15_6	P14_1	P14_5	P14_8	P13_1	P13_3	P11_2	P11_9	P11_11	P10_0	P10_3	P10_2	P10_6	P10_7	VEXT	N.C.													P02_12	P02_13	F
E	N.C.	N.C.																																			N.C.	N.C.	E
D	N.C.	N.C.																																			N.C.	N.C.	D
C	N.C.	N.C.																																			N.C.	N.C.	C
B	VSS	VSS	VDDP3	N.C.	N.C.	N.C.	N.C.	P15_15	P15_12	P15_14	N.C.	N.C.	P14_12	P14_14	N.C.	P13_4	P13_6	N.C.	P13_13	P13_12	P13_14	N.C.	N.C.	N.C.	P10_9	P10_10	N.C.	P10_14	N.C.	VEXT	VSS	N.C.				B			
A	VSS	VDDP3	N.C.	N.C.	N.C.	N.C.	N.C.	P15_11	P15_13	P15_15	N.C.	N.C.	P14_11	P14_13	N.C.	P13_5	P13_7	P13_9	P13_11	P13_13	P13_15	N.C.	N.C.	N.C.	N.C.	P10_11	P10_13	P10_15	N.C.	N.C.							A		

Connection status:

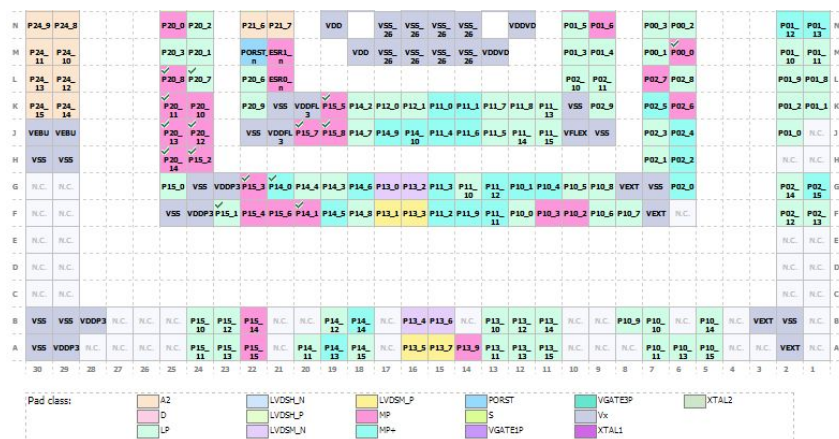
Error

Warning

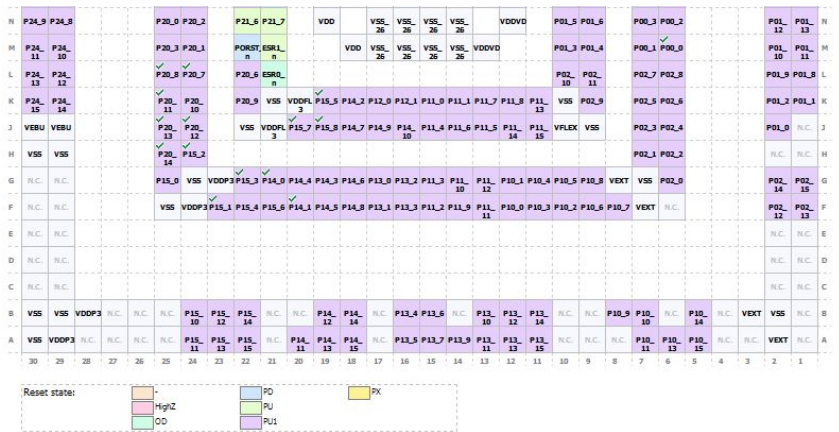
OK

Info

■ Pad Class

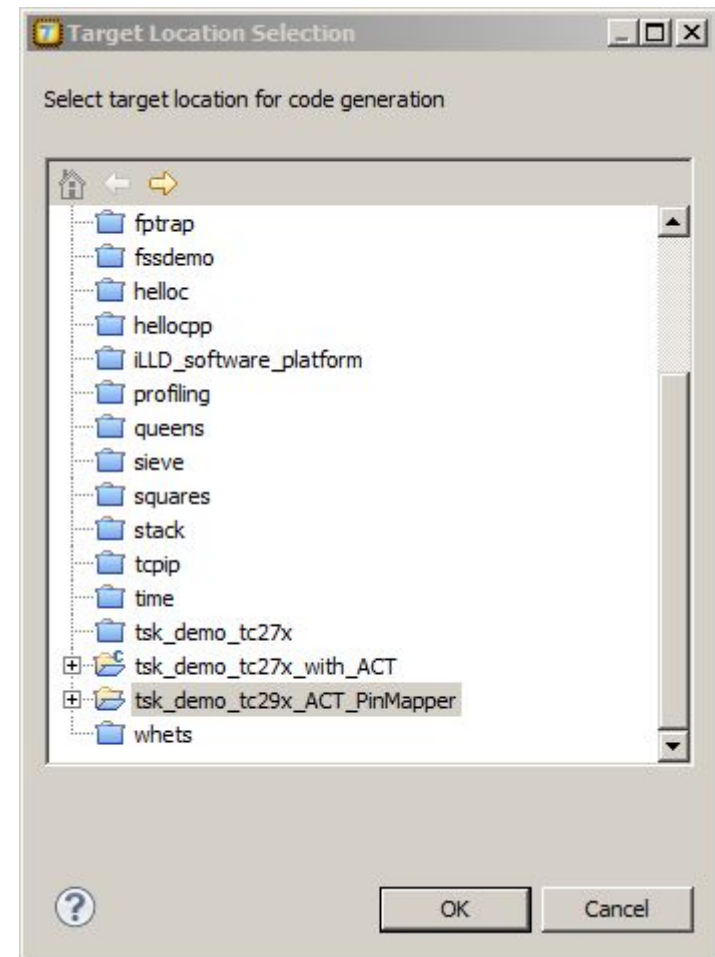


■ Reset State



ACT – Pin Mapper

- After the configuration the target project for the setting has to be chosen
- The configuration is stored in xml-like-format



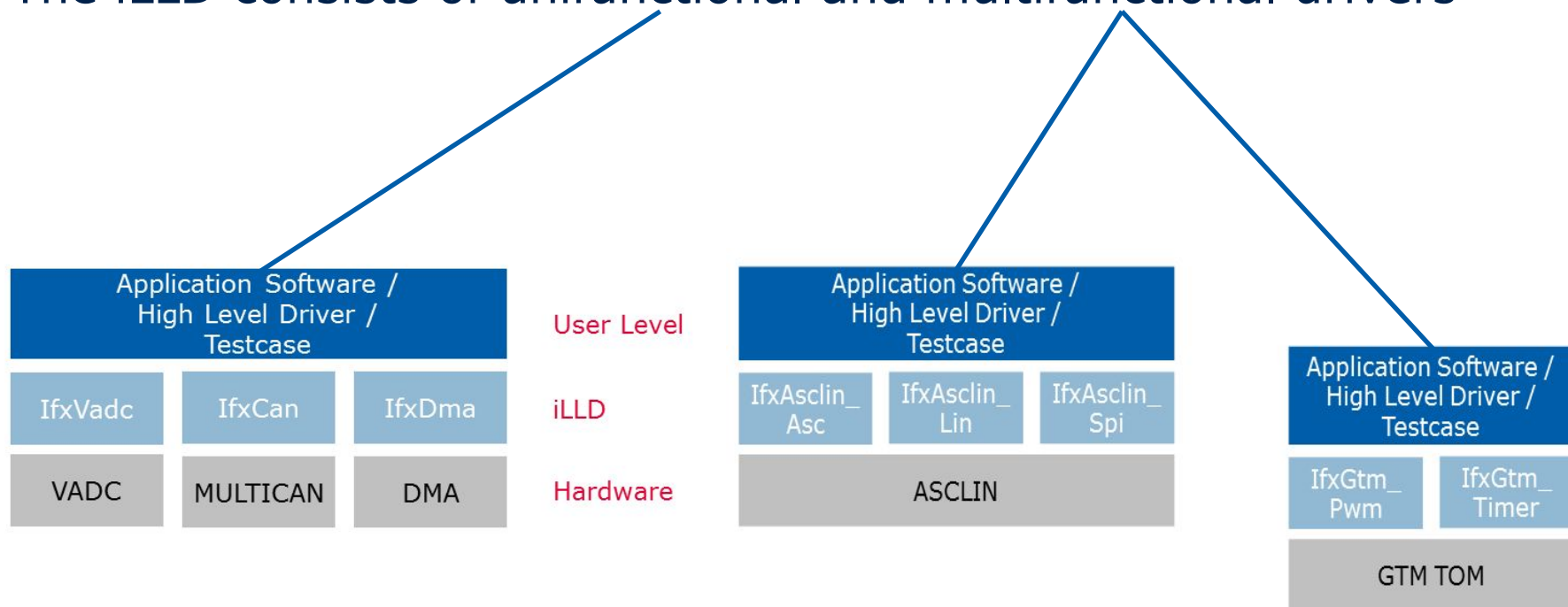
ACT – Driver Configuration

ACT – Driver Configuration

- iLLD come from tests and application used by several teams at infineon ATV
- iLLD are basic function low level drivers for use and demonstration for almost every module
- All drivers have the same code styling -> common look and feel
- Already tested in pre-silicone with a virtual prototype or in RTL-simulations
- Each derivate (TC2YX) has its own set of drivers
- No dependency between the peripheral drivers
- The strict iLLD coding guidelines allow layering of drivers for multi-dimensional system scenarios
- Available in the beta ACT-release (estimated Q2/15)

ACT – Driver Configuration

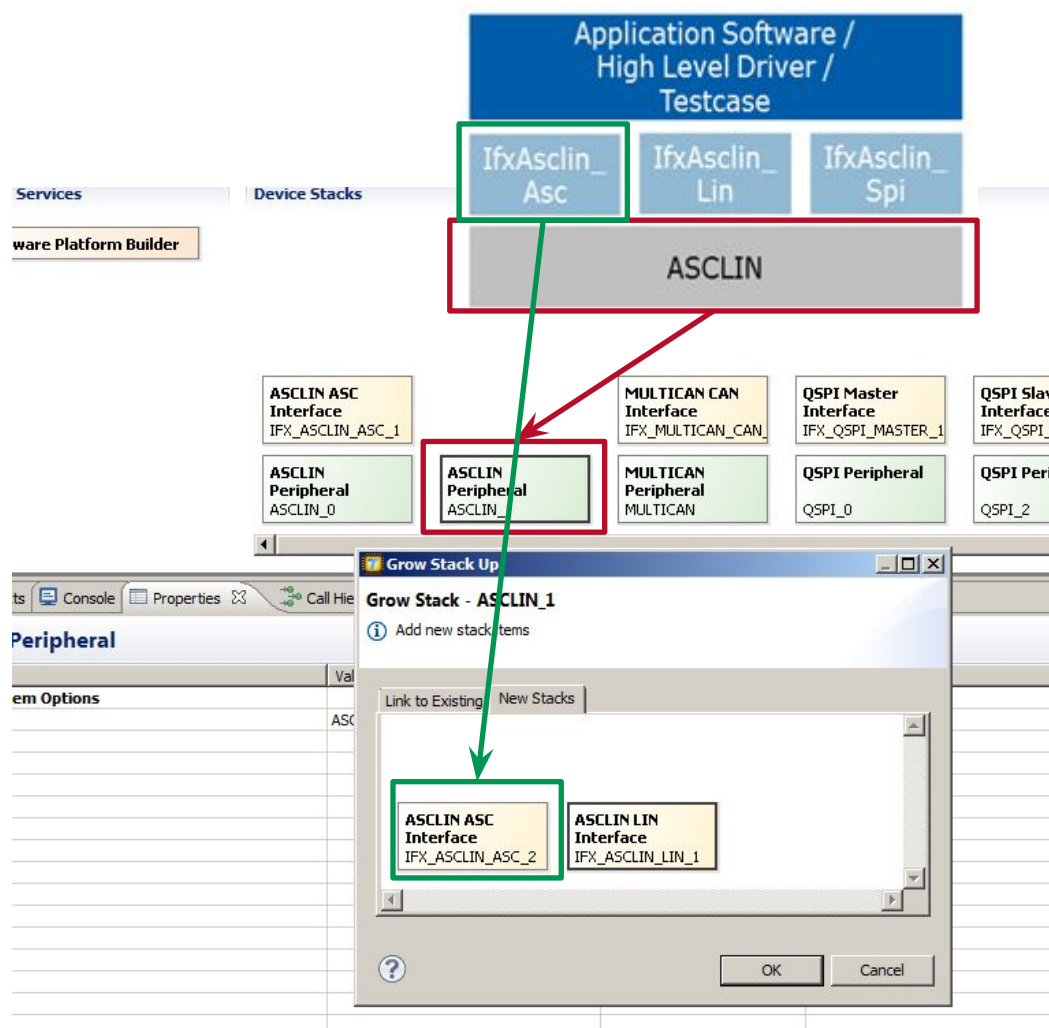
- The iLLD consists of unifunctional and multifunctional drivers



ACT – Driver Configuration

- Multifunctional drivers: Add a new peripheral and choose the iLLD for this module

- Right click in the window and add a new service or driver
- Then you can choose the iLLD for the module



ACT – Driver Configuration

- Select the iLLD from a module and configure your parameters

TASKING Software Platform - TC27X

Software Services | Device Stacks

Software Platform Builder

ASCLIN ASC Interface
IFX_ASCLIN_ASC_1

MULTICAN CAN Interface
IFX_MULTICAN_CAN_1

**QSPI Master Interface
IFX_QSPI_MASTER_1**

QSPI Slave Interface
IFX_QSPI_SLAVE_1

STM Comparator
IFX_STM_COMPARAT

ASCLIN Peripheral
ASCLIN_0

MULTICAN Peripheral
MULTICAN

QSPI Peripheral
QSPI_0

QSPI Peripheral
QSPI_2

STM Peripheral
STM_0

Pin Conflicts | Console | Properties | Call Hierarchy | Search

QSPI Master Interface

Property	Value	Type	Range / Prototype
Stack Item Options			
ID	IFX_QSPI_MASTER_1		
SPI Interface			
Receive Interrupt Priority	2	UINT 16	
Transmit Interrupt Priority	1	UINT 16	
Error Interrupt Priority	0x30	UINT 16	
Type of Interrupt Service	Cpu0	ENUM	
Maximum Channel Baudrate	10000000	UINT32	
Enable Sleep Mode	false	BOOLEAN	
Pause On Baudrate Spike Errors	false	BOOLEAN	
Run or Pause Mode	Pause	ENUM	
TX FIFO Interrupt Threshold	1	ENUM	
RX FIFO Interrupt Threshold	0	ENUM	
Enabled Interrupts			
TX Interrupt	true	BOOLEAN	
RX Interrupt	true	BOOLEAN	
PT1 Interrupt	false	BOOLEAN	
PT2 Interrupt	false	BOOLEAN	
USD Interrupt	false	BOOLEAN	
DMA Configuration			
Use DMA	true	BOOLEAN	
Receive DMA Channel	2	INT 16	-1..127
Transmit DMA Channel	1	INT 16	-1..127
Receive DMA Interrupt Priority	11	UINT 16	
Transmit DMA Interrupt Priority	10	UINT 16	

Automatically calculates frequency and prescaler for the clock-sources

Can setup DMA

ACT – Generated Struct

- E. g., for QSPI Master, the generated init-struct is

QSPI Master Interface	
Property	Value
<input checked="" type="checkbox"/> Stack Item Options	
ID	IFX_QSPI_MASTER_1
<input checked="" type="checkbox"/> SPI Interface	
Receive Interrupt Priority	2
Transmit Interrupt Priority	1
Error Interrupt Priority	0x30
Type of Interrupt Service	Cpu0
Maximum Channel Baudrate	10000000
Enable Sleep Mode	false
Pause On Baudrate Spike Errors	false
Run or Pause Mode	Pause
TX FIFO Interrupt Threshold	1
RX FIFO Interrupt Threshold	0
<input checked="" type="checkbox"/> Enabled Interrupts	
TX Interrupt	true
RX Interrupt	true
PT1 Interrupt	false
PT2 Interrupt	false
USR Interrupt	false
<input checked="" type="checkbox"/> DMA Configuration	
Use DMA	false

```

/*
 * Software Platform Generated File
 * -----
 */

#include "ifx_qspi_master_cfg_instance.h"

const ifx_qspi_master_cfg_instance_t ifx_qspi_master_instance_table[1] =
{
    {
        2,
        1,
        0x30,
        IFX_QSPI_MASTER_INSTANCE_BASE_ISR_PROVIDER_CPU0,
        10000000,
        },
        false,
        false,
        IFX_QSPI_MASTER_INSTANCE_PAUSE_RUN_TRANSITION_PAUSE,
        IFX_QSPI_MASTER_INSTANCE_TX_FIFO_THRESHOLD_1,
        IFX_QSPI_MASTER_INSTANCE_RX_FIFO_THRESHOLD_0,
        {
            true,
            true,
            false,
            false,
            false,
        },
        {
            false,
            2,
            1,
            11,
            10,
        },
        0,
    },
};

```

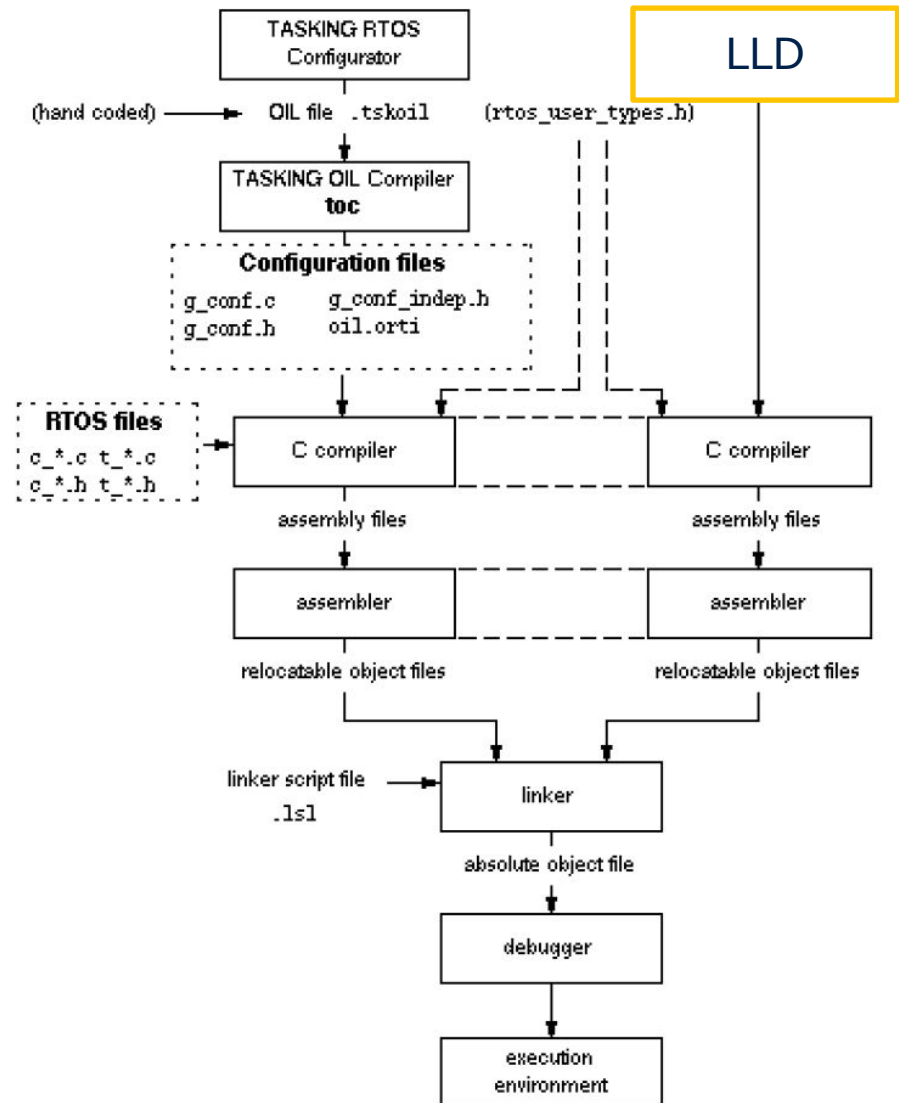
DMA

ACT – OS

OS – With Respect To The TASKING OS

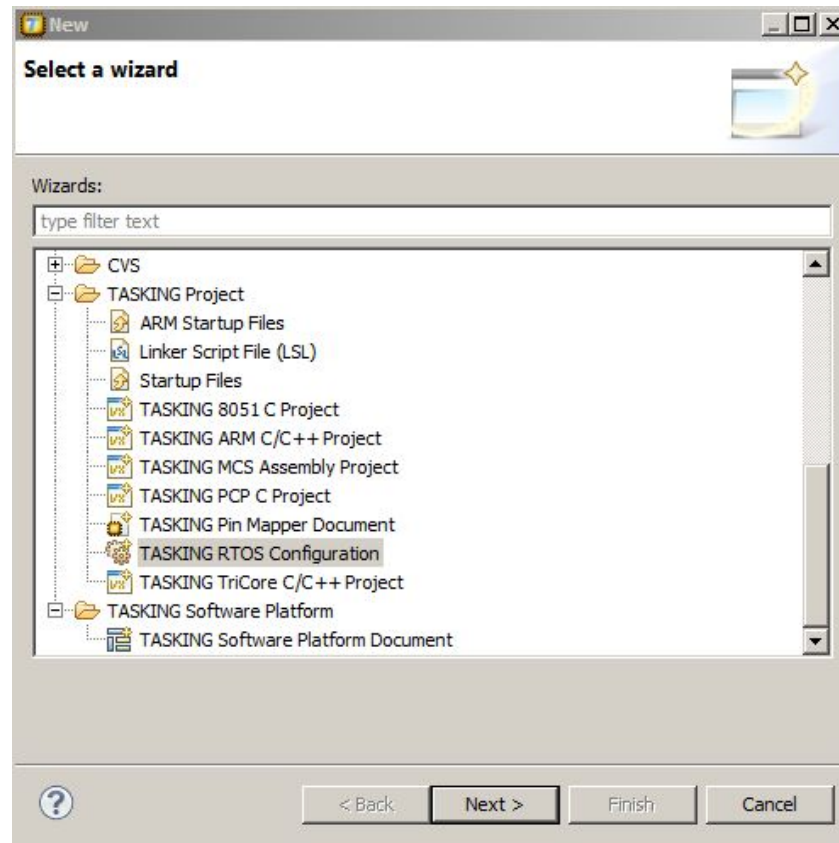
■ 3 stage implementation:

- Configurator
 - Generates an oil-file
- OIL compiler
 - Generates c- and h-files
- Normal compiler+linker
 - Generates the hex-/elf-file



OS – Create the Config

- Select File ☐ New



- And create the oil-file

OS – OIL-Configurator

Object / Attribute	Value	Type	Description
+ OS	New_OS	OS-routines	
APPMODE	APPMODE1		
+ TASK	T1	Task-config	
+ TASK	T2		
+ TASK	T3		
+ TASK	T4		
+ TASK	T5		
+ TASK	T6		
+ TASK	T7		
+ TASK	T8		
+ ISR	Taster1ISR		
+ ISR	Taster2ISR		
+ ISR	Taster3ISR		
+ ISR	Taster4ISR		
COUNTER	SYSTEM_COUNTER		System timer counter
+ ALARM	A1	Alarm-config	
+ ALARM	A2		
+ ALARM	A3		
+ ALARM	A4		
+ ALARM	A5		
+ ALARM	A6		
+ ALARM	A7		
+ ALARM	A8		
+ EVENT	E1	Event-config	
+ EVENT	E2		
+ RESOURCE	R1	Resource-config	
+ RESOURCE	R2		
RESOURCE	RES_SCHEDULER		System scheduler resource
COM	New_COM		
+ MESSAGE	M1	Message-config	
+ MESSAGE	M2		





OS – Basic Configuration

New OS			
STATUS	EXTENDED	ENUM	Task-config
STARTUPHOOK	TRUE	BOOLEAN	
ERRORHOOK	FALSE	BOOLEAN	Used hook-routines
SHUTDOWNHOOK	FALSE	BOOLEAN	
PRETASKHOOK	FALSE	BOOLEAN	
POSTTASKHOOK	FALSE	BOOLEAN	
USEGETSERVICEID	FALSE	BOOLEAN	
USEPARAMETERACCESS	FALSE	BOOLEAN	
USERESSCHEDULER	TRUE	BOOLEAN	
LONGMSG	FALSE	BOOLEAN	
ORTI	FALSE	BOOLEAN	
RUNLEVELCHECK	FALSE	BOOLEAN	
SHUTDOWNRETURN	FALSE	BOOLEAN	
IDLEHOOK	FALSE	BOOLEAN	
IDLELOWPOWER	FALSE	BOOLEAN	OS-timer setup
USERTOSTIMER	TRUE	BOOLEAN	
RTOSTIMERPRIO	1	UINT32 [1..255]	
RTOSTIMER	T6	ENUM	
OSCLOCKHZ	10	UINT32 [1..100000]	
CPUCLOCKMHZ	200	UINT32 [1..400]	

OS – Alarm Configuration

[-] [A] ALARM	A1		
[G] COUNTER	SYSTEM_COUNTER	COUNTER_TYPE	Base counter
[-] ACTION	ACTIVATETASK	ENUM	
[T] TASK	T1	TASK_TYPE	Task assignment
[-] AUTOSTART	TRUE	BOOLEAN	
CYCLETIME	11	UINT32	Period
[A] APPMODE[1]	[APPMODE1]	APPMODE_TYPE	
ALARMTIME	11	UINT32	Duration

OS – Task Configuration

☰  TASK	T1	
PRIORITY	1	UINT32 [1..254]
SCHEDULE	FULL	ENUM
ACTIVATION	1	UINT32 [1..255]
AUTOSTART	FALSE	BOOLEAN
 RESOURCE[2]	[RES_SCHEDULER, R1]	RESOURCE_TYPE
 EVENT[1]	[E1]	EVENT_TYPE
 MESSAGE[1]	[M2]	MESSAGE_TYPE
STACKSIZE	250	UINT32

Preemptiv/non
preemptive scheduling

Resource assignment

Event assignment

Message assignment



ENERGY EFFICIENCY MOBILITY SECURITY

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