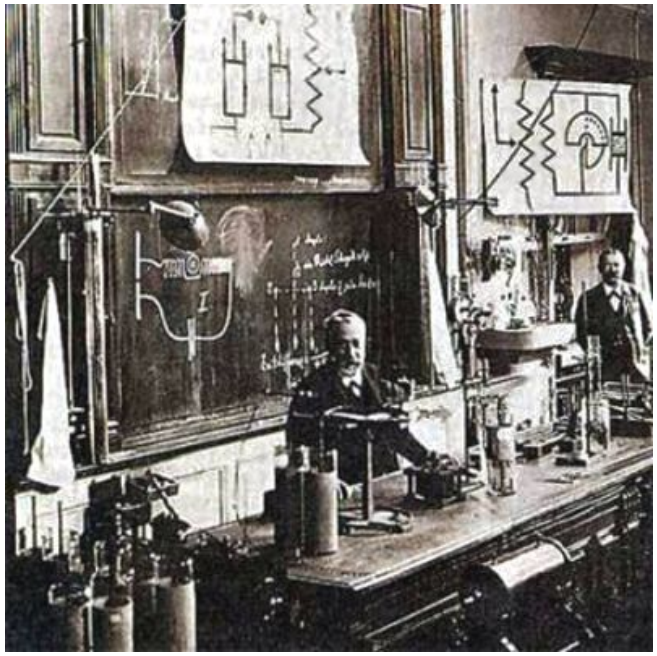
1874 - Semiconductor Point-Contact Rectifier Effect Discovered



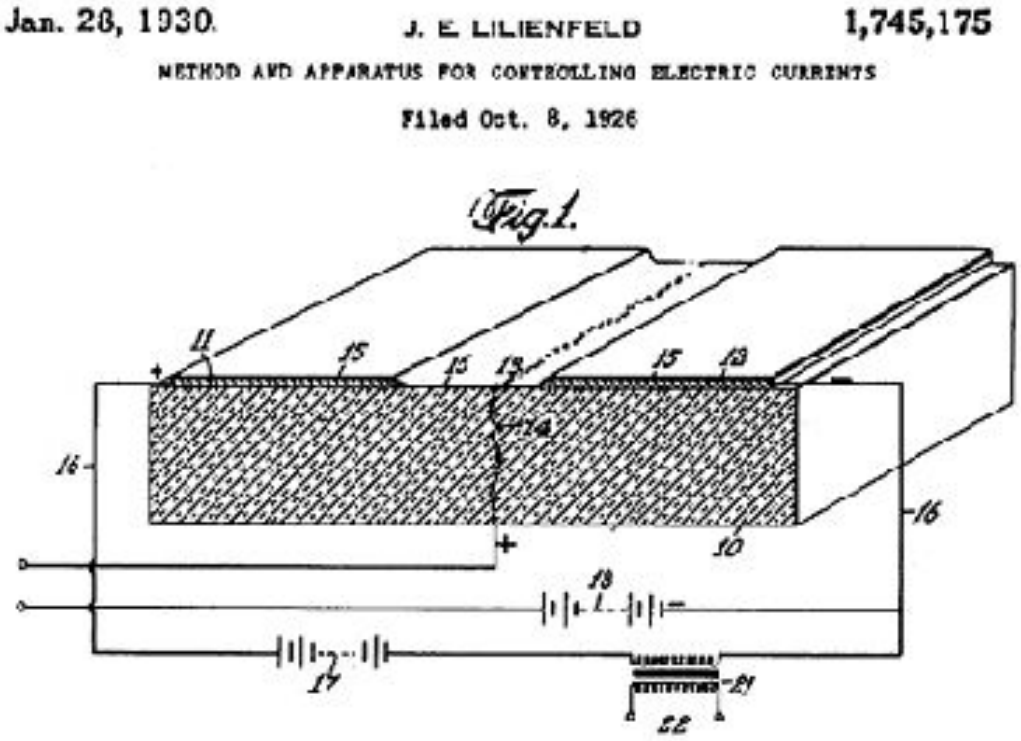
Ferdinand Braun
Nobel Laureate in Physics in 1909

In the first written description of a semiconductor diode, he noted that current flows freely in only one direction at the contact between a metal point and a galena crystal (lead sulfide). More famous for his invention of CRT.

Source for this and next 8 slides: http://www.computerhistory.org/semiconductor/timeline.html

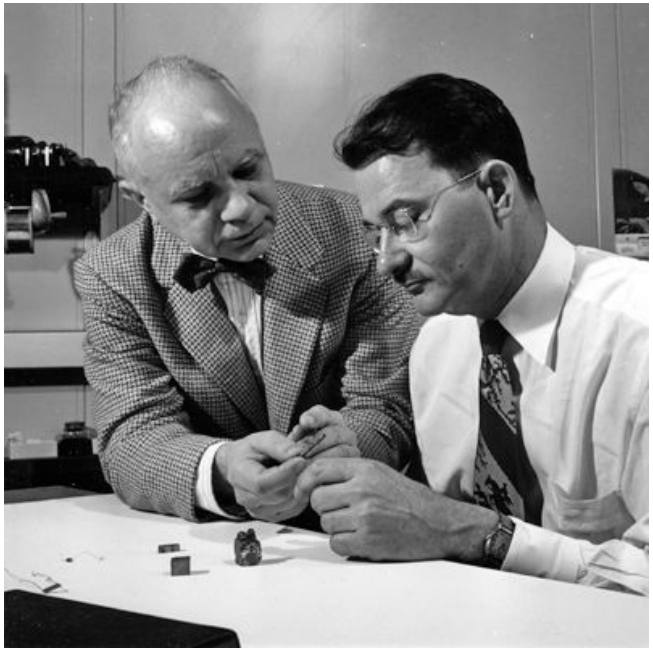
1930: Field Effect Semiconductor Device Concepts Patented

Julius Lilienfeld

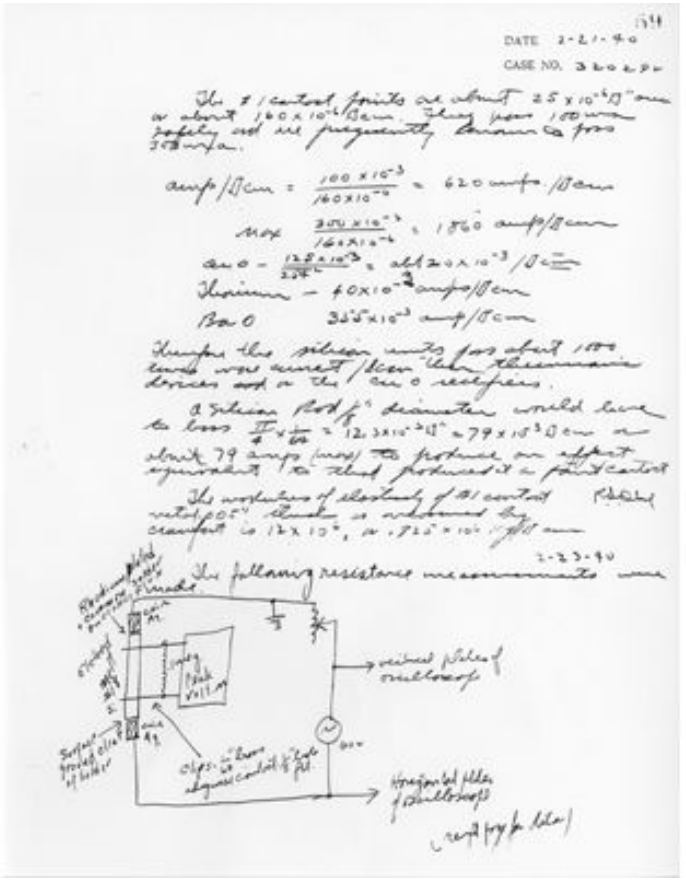


Julius Lilienfeld filed a patent describing a three-electrode amplifying device based on the semiconducting properties of copper sulfide. He did not demonstrate the device experimentally.

1940 - Discovery of the p-n Junction



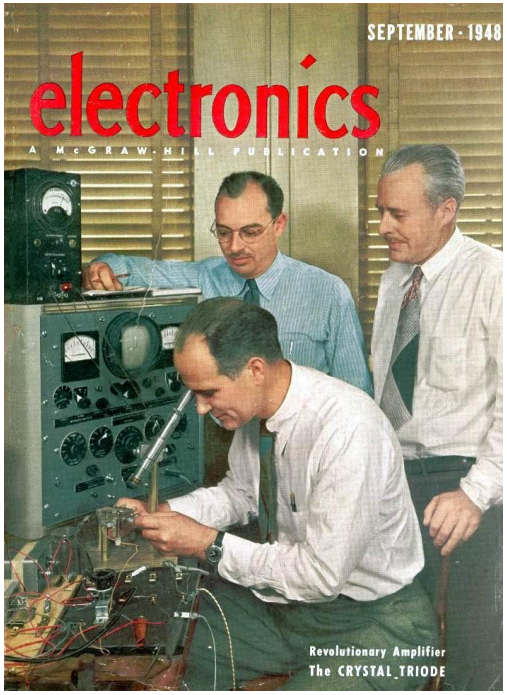
Russell Ohl and Jack Scaff

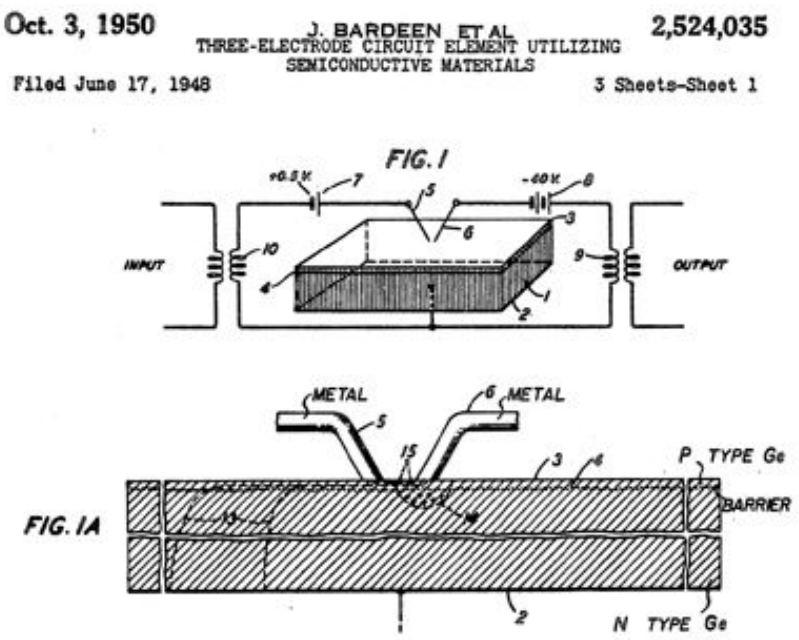


Russell Ohl and Jack Scaff at Bell Telephone Labs discovered the p-n junction and photovoltaic effects in silicon that lead to the development of junction transistors and solar cells.

1947 - Invention of the Point-Contact Transistor in Germanium

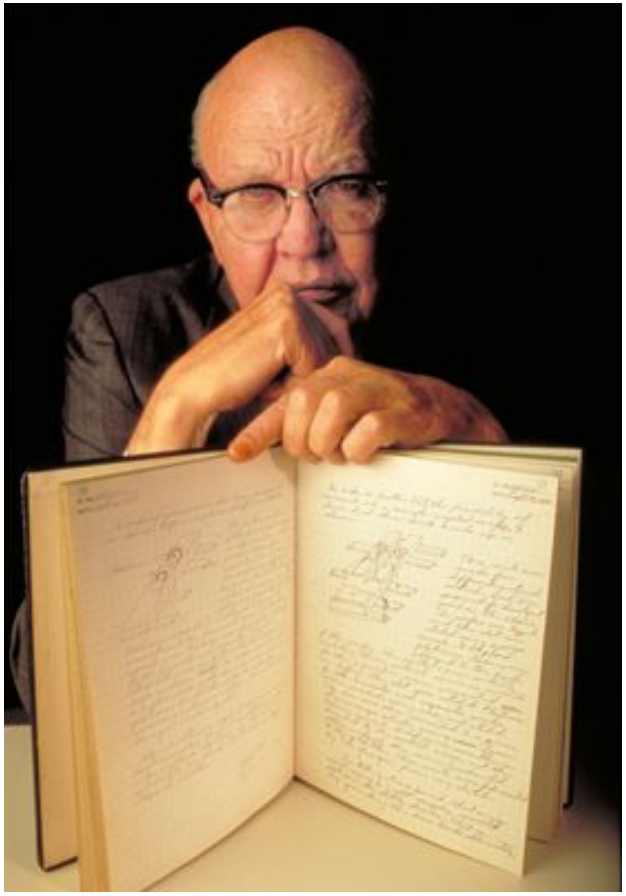
By Bardeen, Brattain, and Shockley,
Nobel Laureates in Physics 1956

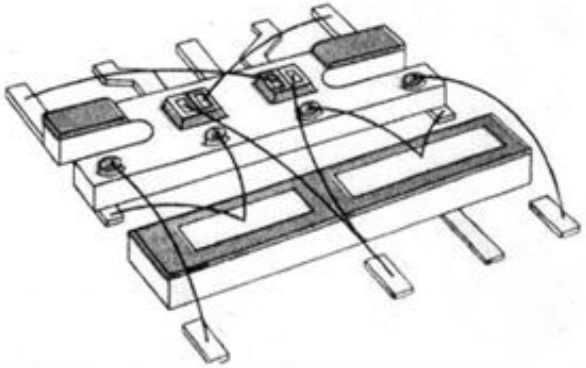


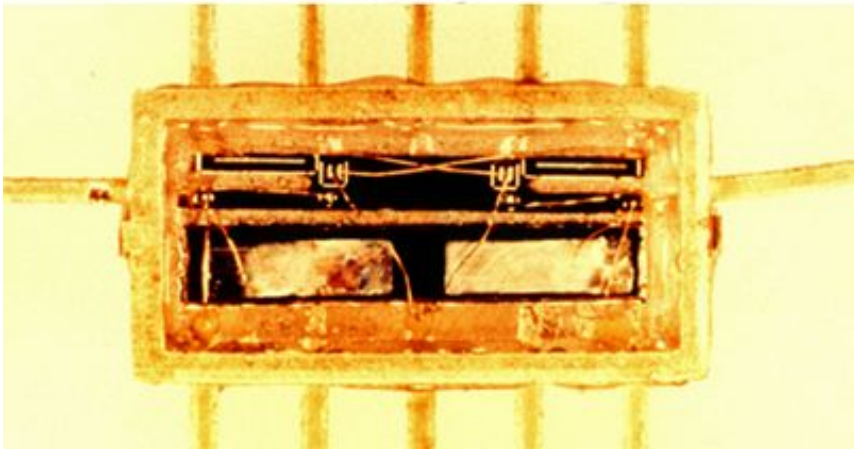


1958 - All semiconductor “Hybris Integrated Circuit" is demonstrated in Germanium

By Jack Kilby (TI),
Nobel Laureates in Physics 2000

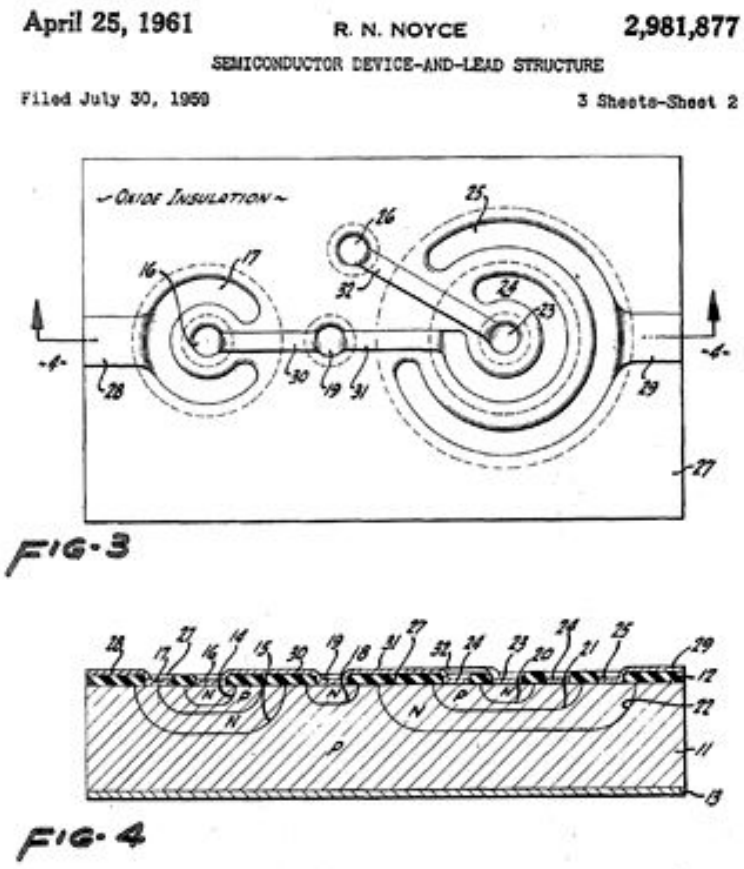






1959 - Practical Monolithic Integrated Circuit Concept Patented

Robert Noyce



Challenged by patent attorney to identify other uses for Hoerni's planar process, Fairchild co-founder Robert Noyce conceived the idea for a monolithic integrated circuit (IC) in **silicon**.

1960 - MOS Transistor Demonstrated

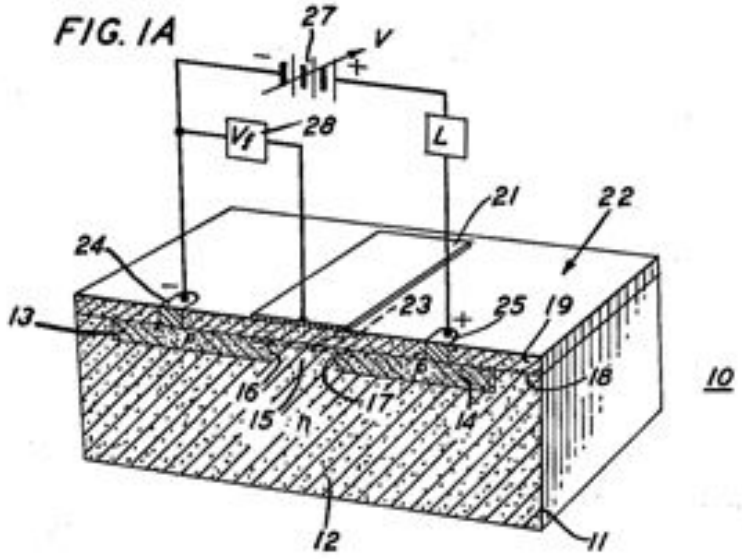
Dawon Kahng

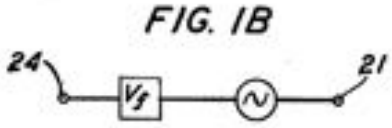
John Atalla

Aug. 27, 1963 DAWON KAHNG 3,102,230

ELECTRIC FIELD CONTROLLED SEMICONDUCTOR DEVICE

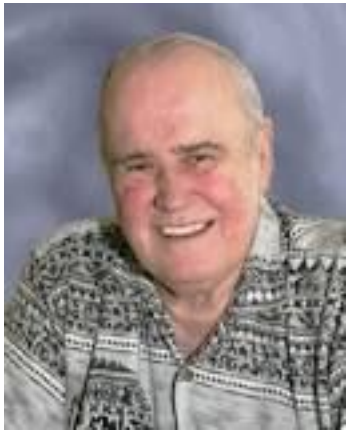
Filed May 31, 1960



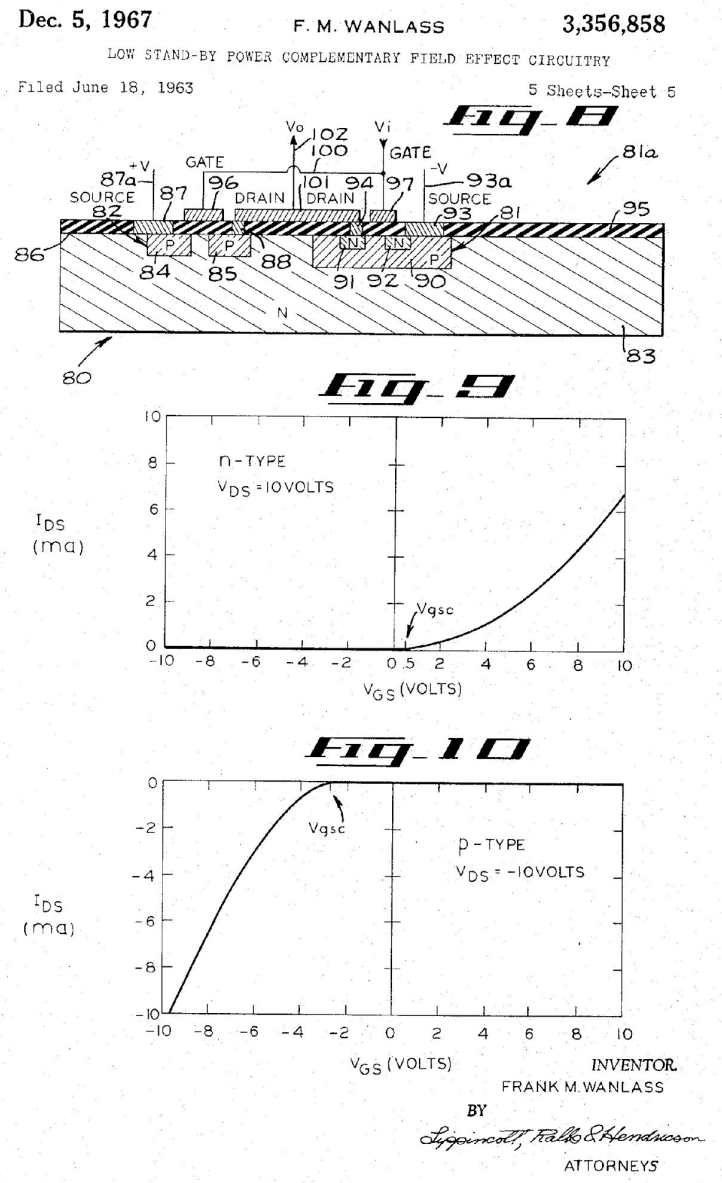


John Atalla and Dawon Kahng at Bell demonstrate the first successful silicon PMOS field-effect amplifier.

1963 - Complementary MOS Circuit Invented

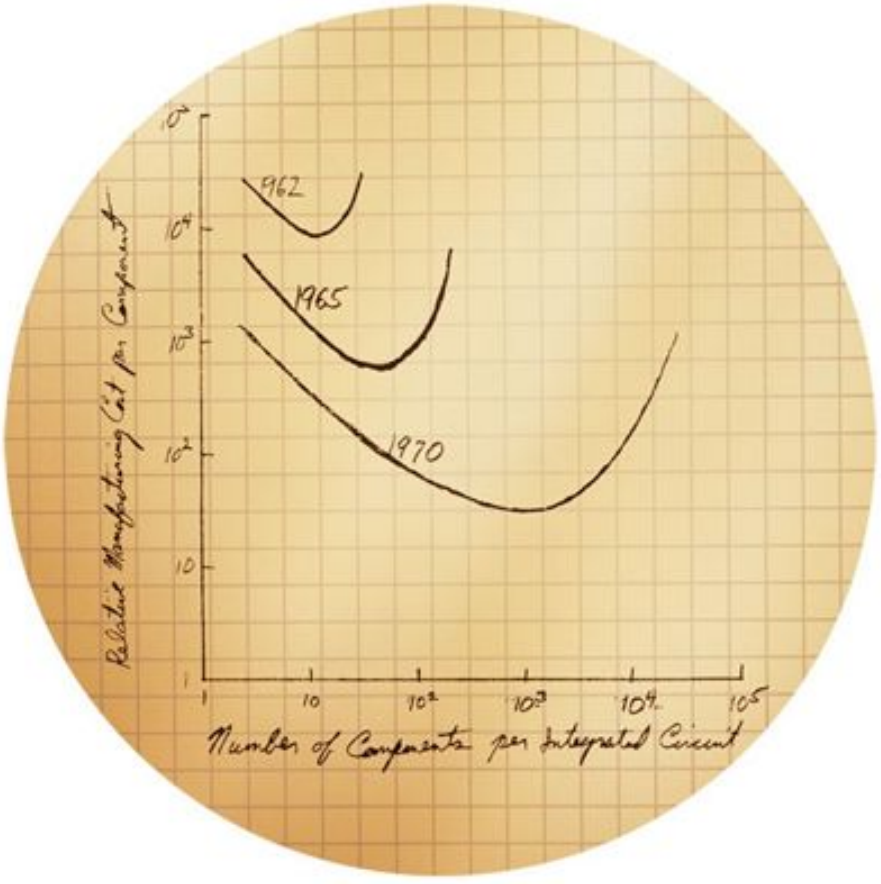


Frank Wanlass and C. T. Sah at Fairchild R & D Labs report the lowest power logic configuration .



1965 - "Moore's Law" Predicts the Future of Integrated Circuits

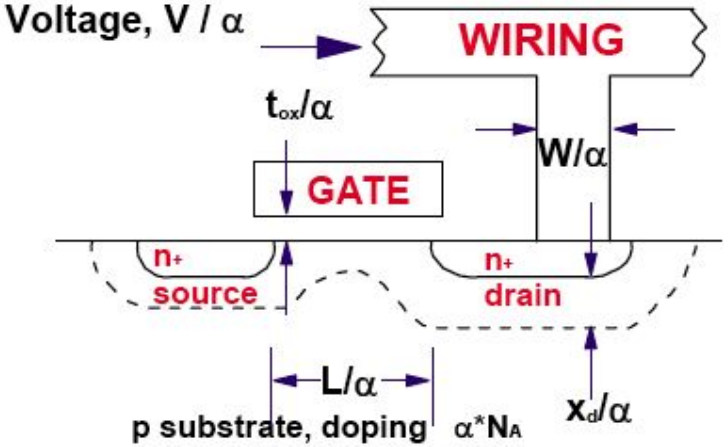
Gordon Moore



Cost vs. time sketch from Moore's 1964 notebook

1974 - Scaling of IC Process Design Rules Quantified

Robert Dennard, et al., IEEE J. Solid State Circuits, Oct. 1974.



Constant E Field Scaling

All device parameters are scaled by the same factor α.

- Channel length L ↓
- Gate oxide thickness t_{ox} ↓
- Supply voltage V_D ↓
- Source/drain junction depth X_j ↓
- Channel doping ↑

Thank you