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Placement and routing guidelines for Power Electronics Devices

Printed Circuit Board Design for Power Electronics: A Practical Guide

Dr. Oleksandr Velihorskyi, PhD

Lecture plan

- Planning the layout.
- Single-board PCB layout.
- Placement of Layers for PE devices.
- Current loops in Power Electronics Devices.
- Grounding in the PE devices.
- Land Patterns for SMD components in PE devices.
- Control scheme layout consideration.

Current position: 1/7

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PCB design for PE devices. Why is it so important?

- Improper PCB design leads to:
  - "unstable" switching waveforms and jittering,
  - audible noise from the magnetic components,
  - ringing, crosstalk, ground bounce,
- PCB design can lead good scheme to fail.
  - but even best PCB design can’t improve bad schematic solution.

Planning the layout.

- Each PE device contains power part and control scheme.
  - Power part - DC/DC, DC/AC, AC/AC.
  - Control - measure parameters and generate signals.
- Type of signals in the PE devices:
  - analog – measured values (control) - **victims**,
  - digital – control signals, interface with the environment (PC, memory, etc.) – **aggressors/victims**,
  - power – DC or AC, sine, pulse - **aggressors**.

Planning the layout.

- Do we need to separate power and control on to two different PCB's?
  - device characteristics?
    - EMC?
    - accuracy?
    - maintainability?
  - cost?
  - reliability?

Planning the layout.

Parameter	Multi-board	Single-board
EMC	+	-
accuracy	+	-
maintainability	+	-
cost	-	+
reliability	-	+

Current position: 2/7

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Single-board PCB layout.

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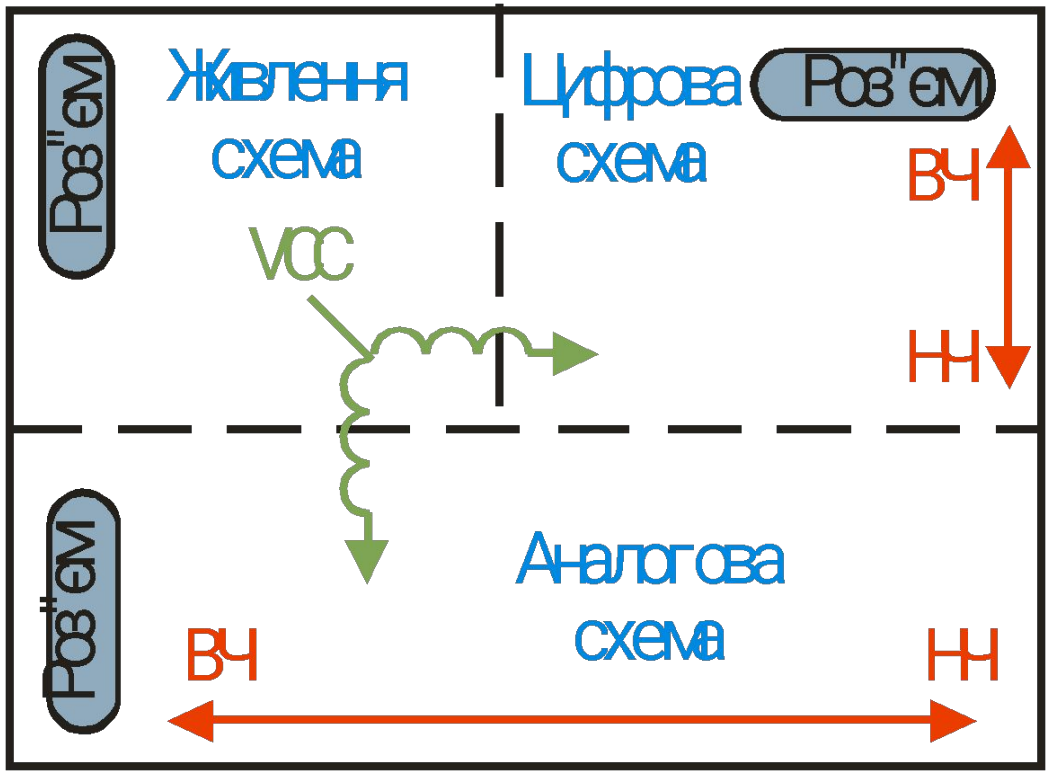
- Power part location should be done at the first stage of PCB layout.
- “Rooms” in CAD like Altium Designer can significantly improve PCB layout efficiency.
- Power part is a one of the most complex part of the PE device.

Single-board PCB layout.

- Typical PCB layout of the single-board PE device.



Single-board PCB layout.

- High speed components (both analog and digital) need to be placed as close as possible to external connectors (if required)!
- Analog and digital signals in an ideal case should never run parallel to each other at a small distance!

Current position: 3/7

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Stack of layers – 1, 2 or more?

- 1-layer PCB:
  - Most sensitive to crosstalk and another EMI.
  - Need to use Jumpers.
- 2-layer PCB:
  - Better than 1-layer – more space for traces/components.
  - More resistant to EMI.
  - Plane layers are possible, but not fully realizable.
  - BGA components is not eligible.

Stack of layers – 1, 2 or more?

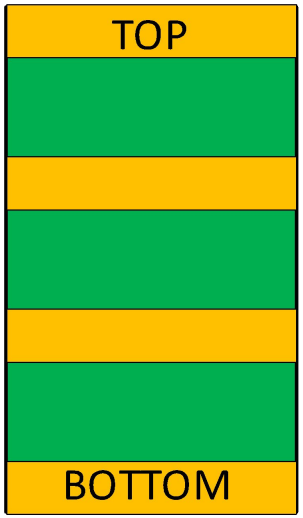
- Multi-layer PCB:
  - Better than 2-layer – more space for traces.
  - Best resistance to EMI (around +20dB compared to 2-layer).
  - Plane layers are fully realizable.
  - All type of components are eligible.
  - Additional cost and design time.

Stack of layers – 1, 2 or more?

- Conclusion:
  - 1-layer PCBs – exceptional cases.
  - 2-layer PCBs – in case of cost-limited projects.
  - Multi-layer PCBs – in typical high-performance cases.

Desirable stack of layers

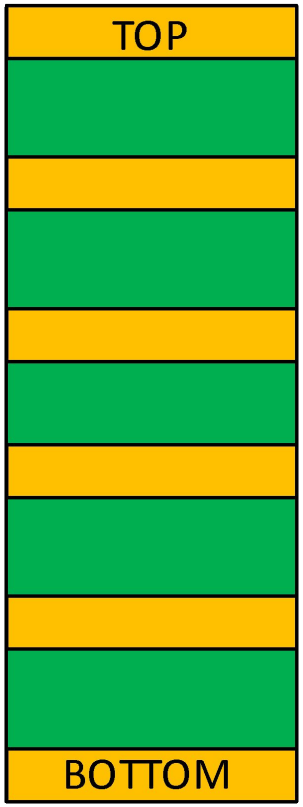
- Typical stack of 4-layers PCB



Power compponent /traces	Power compponent /traces	Power compponent /traces
GND Plane	GND Plane	Small Signal Traces
Small Signal Traces	DC Voltage Plane	GND Plane
Small Signal Traces / Controller components	Small Signal Traces / Controller components	Small Signal Traces / Controller components

Desirable stack of layers

- Typical stack of 6-layers PCB



Power compponent /traces	Power compponent /traces	Power compponent /traces
GND Plane	DC Voltage Plane	Small Signal Traces
Small Signal Traces	Small Signal Traces	GND Plane
Small Signal Traces	Small Signal Traces	DC voltage Plane or GND Plane
DC voltage Plane or GND Plane	GND Plane	Small Signal Traces
Small Signal Traces / Controller components	Small Signal Traces / Controller components	Small Signal Traces / Controller components

Current position: 4/7

- Planning the layout.
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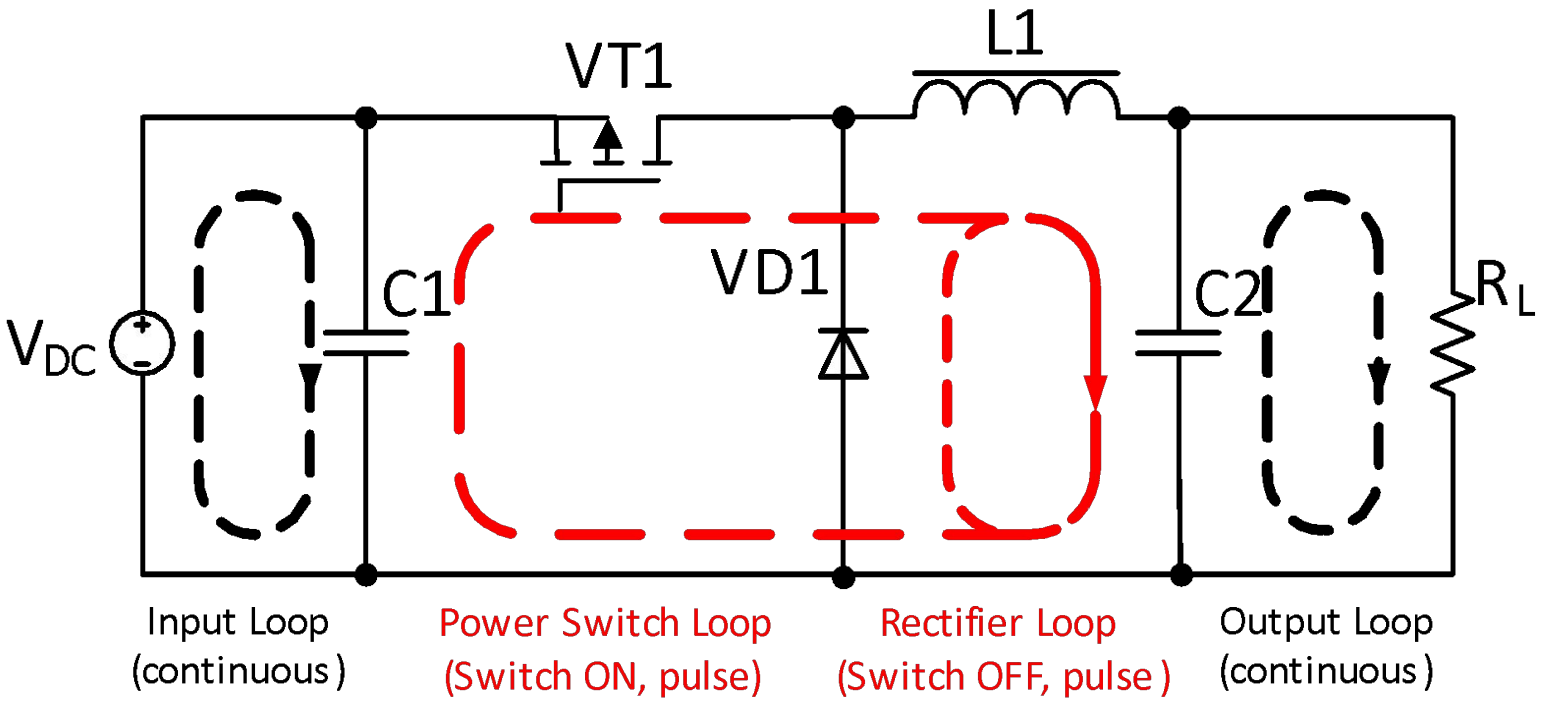
Important features of power part

- Highest currents and voltages in the device
  - What ever – mA and V or A and kV.
  - Traces width and clearances should be wide enough!
- Large current pulses with sharp edges.
  - Sharp edges leads to electromagnetic interference (EMI).
  - PCB designer must pay attention to the each switching circuits in PE device – identify, place components and properly route traces!

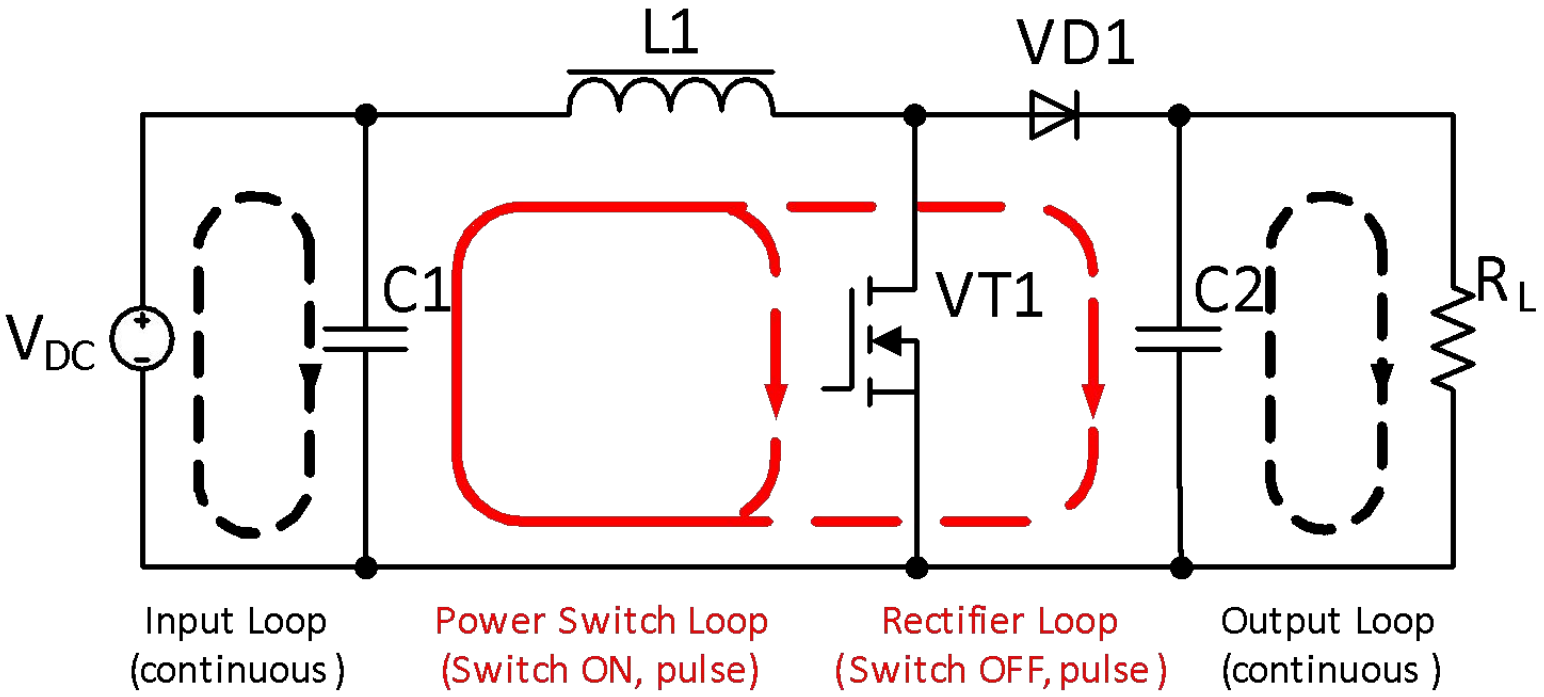
Buck Converter



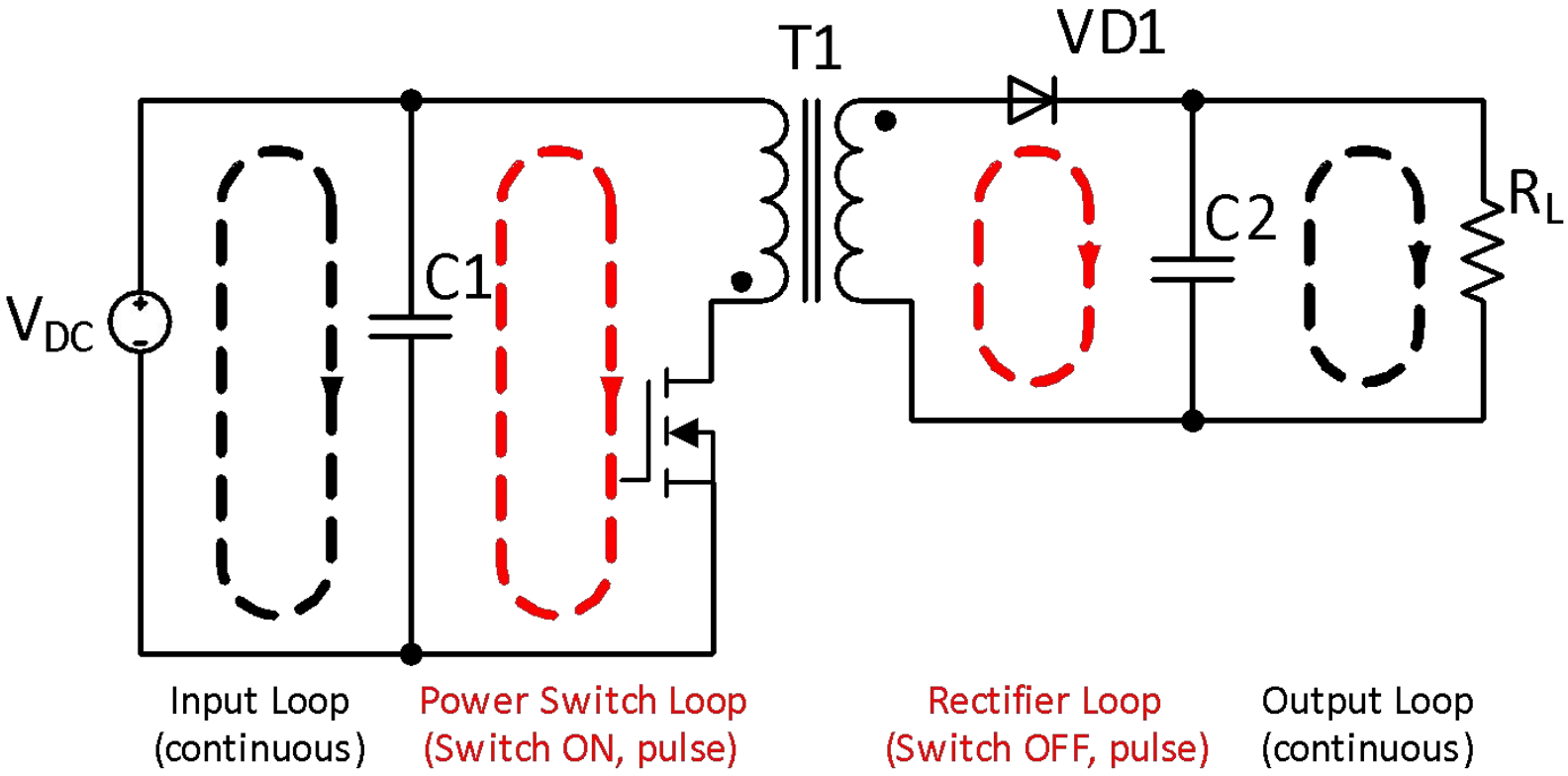
Current loops ordered by EMI generation in power conv.

- 1. Power switch loop – maximum attention!
- 2. Rectifier loop – maximum attention!
- 3. Input source loop.
- 4. Output load loop.

Boost converter



Transformer Isolated Flyback Converter

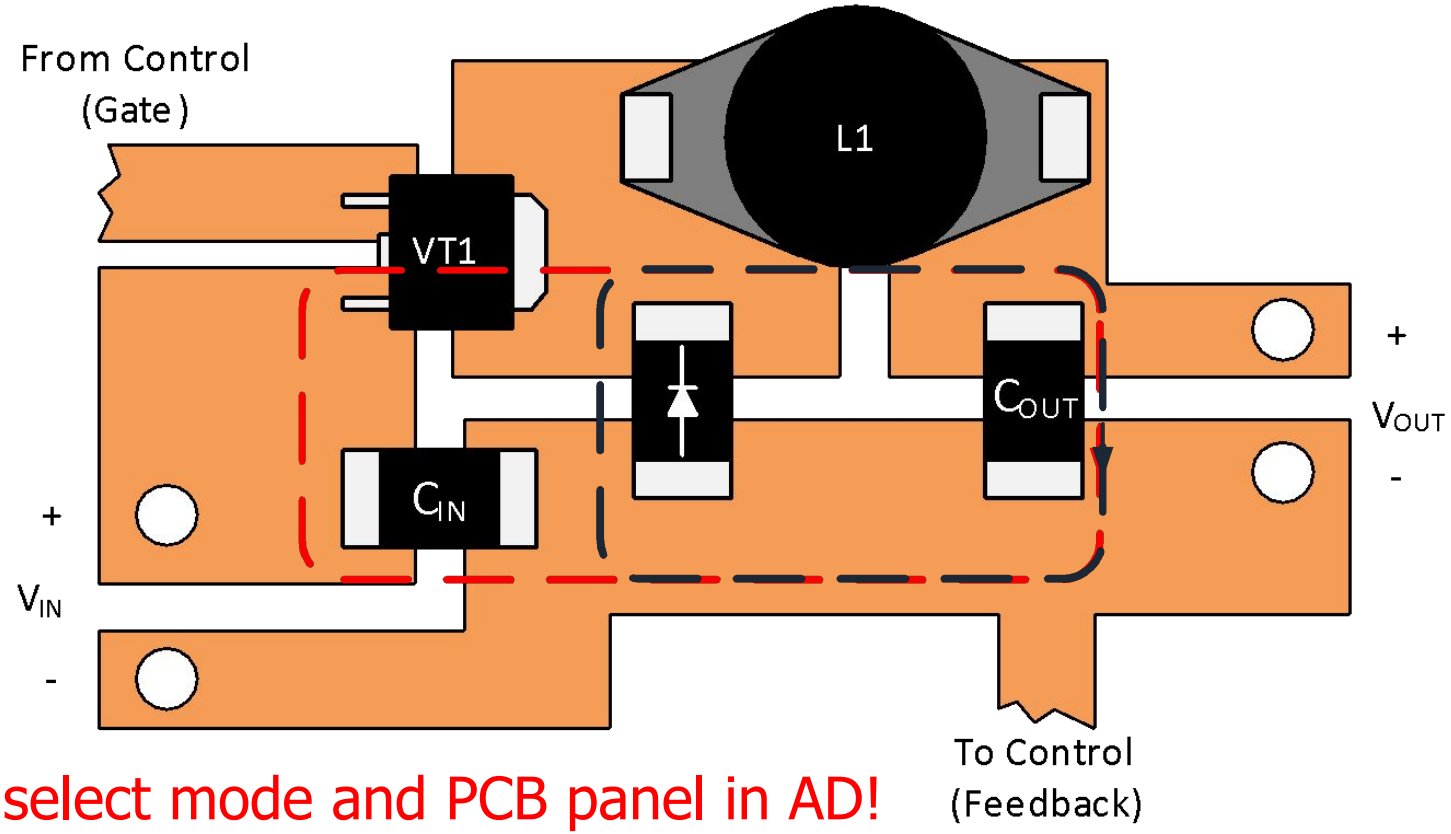


The first rule for PE devices PCB design.

1. The pulse loop circumference must be as short as possible.
   - traces with pulsating current must be as short and wide as possible.
- Results:
  - Trace resistance and inductance improvement.
  - EMI improvement ($\Delta U = L \cdot di/dt$).
  - Efficiency improvement ($P_{trace} = I^2 R$).

PCB layout for buck converter.

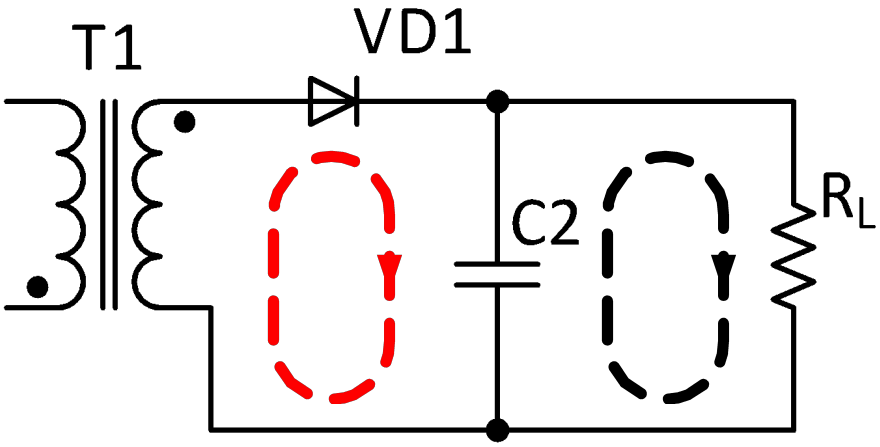
- Red – power switch loop, blue – rectifier loop.

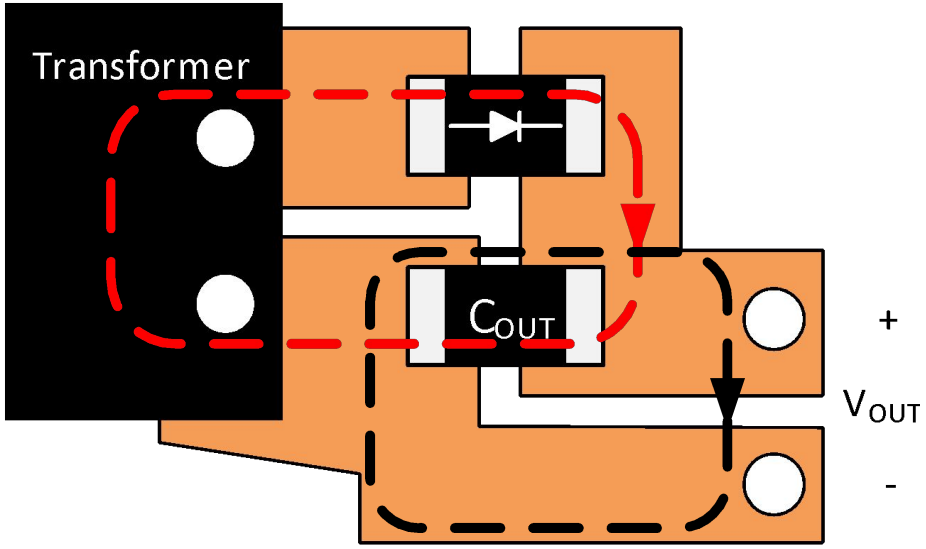


cross select mode and PCB panel in AD!

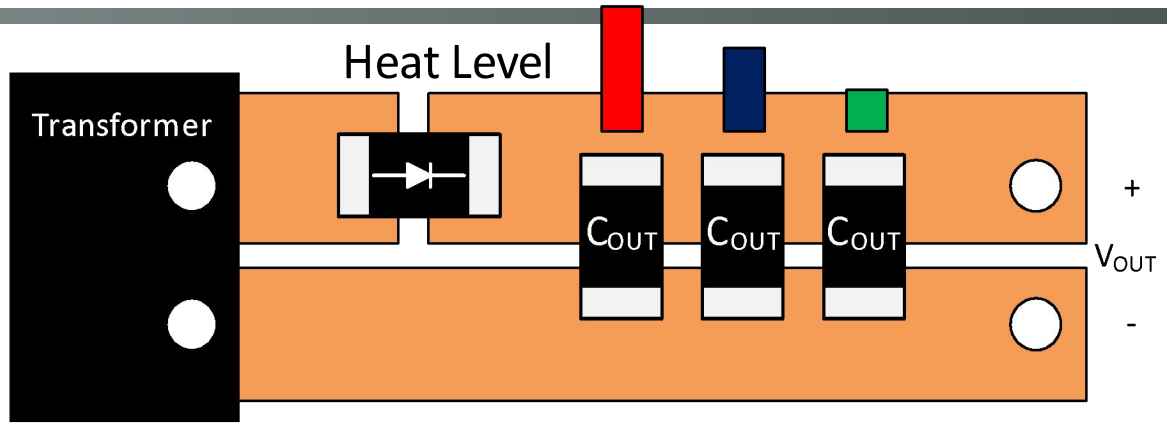
Output Rectifier Loop in Flyback Converter

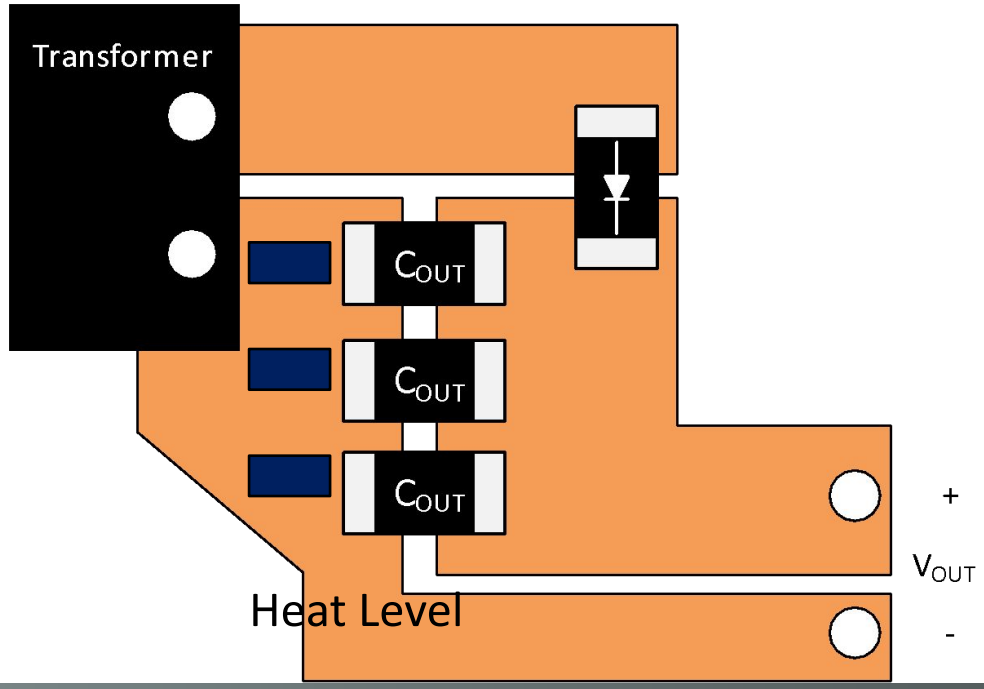
- Red – rectifier loop, black – load loop.





Parallel C Filter Layout





Parallel C Filter Layout

- PCB layout between each capacitor and source in multi-component filter must be as identical as possible!
- Non-identical layout will lead to different current sharing and will reduce capacitor lifespan (mean time between failures, MTBF).

Current position: 5/7

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Grounding in the PE devices.

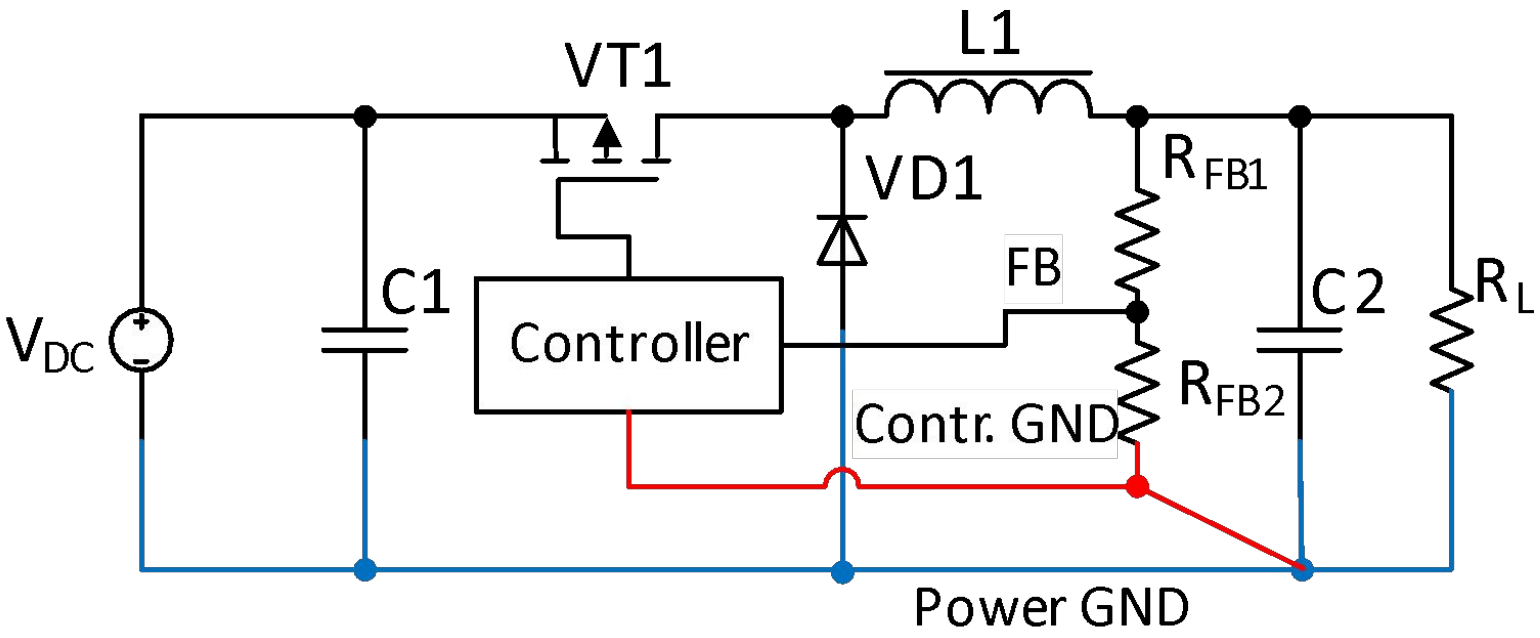
Types of ground in power convertor devices:

- Power ground with high current (DC, AC and pulse).
- Signal ground in controller and feedback part.
  - Analog ground for feedback.
  - Digital ground for controller (MCU, DSP or FPGA device).

Main rule: “separate ground for high-current and signal part”!

Grounding in buck converter

- Red – control ground, blue – power ground.

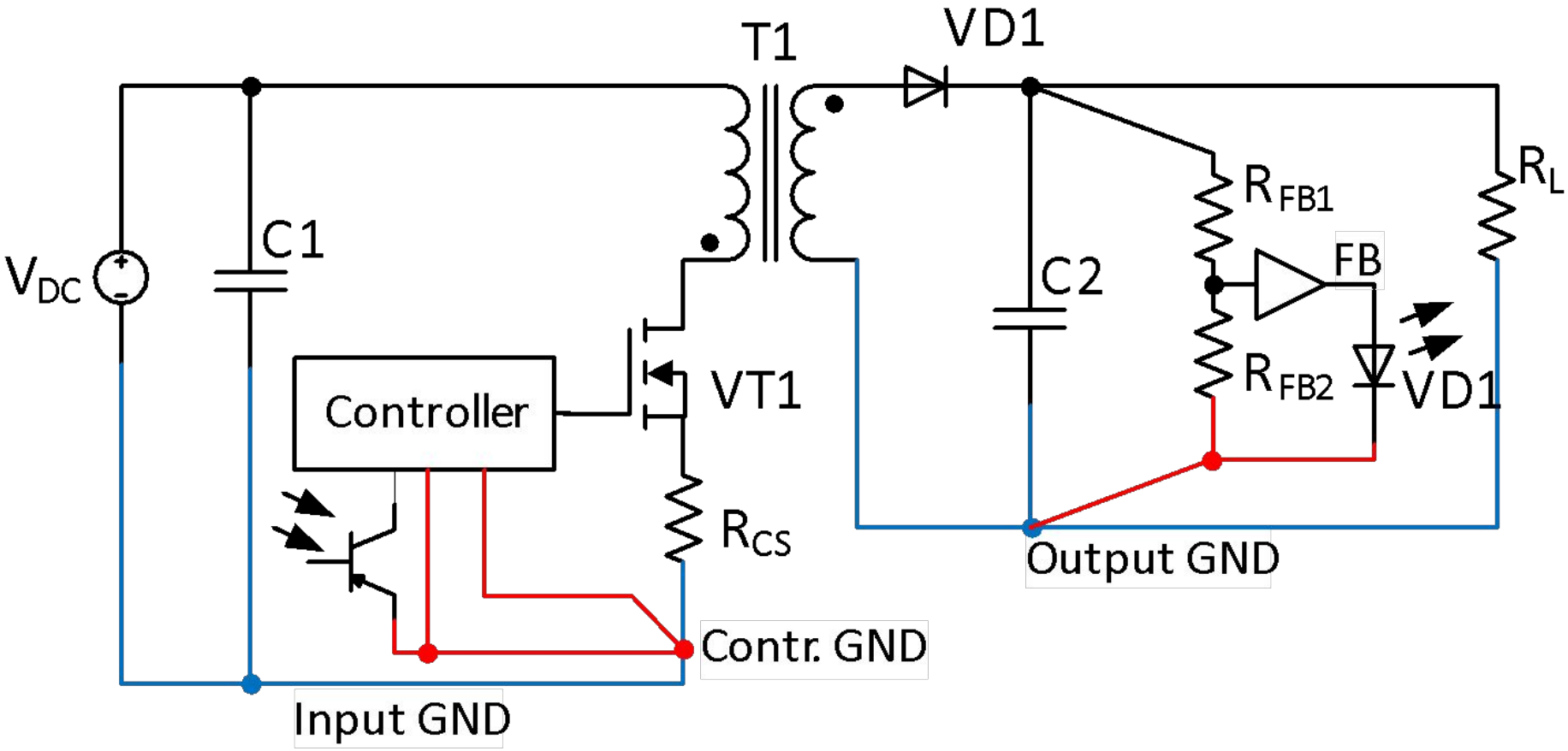


Control and power ground connection.

Rules of thumb for grounding in PE devices:

- Feedback ground must be connected with power ground near the negative pin of output capacitor.
- If control IC has separated (power and control) ground, these pins must be routed separately and connected to the current sensing resistor that measure power switch current.

Grounding in flyback converter



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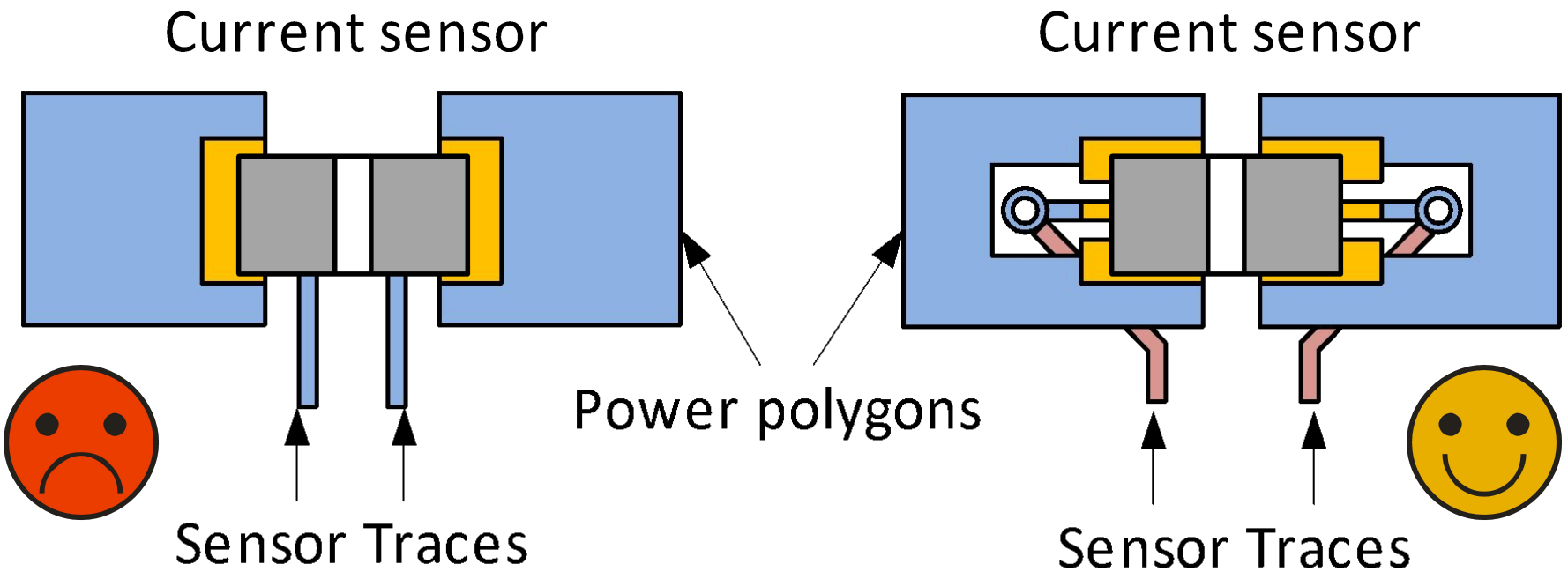
Current sensor resistor PCB layout consideration

- The best characteristic provides 4-wire Kelvin sensing.
- Example of using 2-wire resistors as 4-wire Kelvin



Current sensor resistor PCB layout consideration

- Sensing trace should be placed on opposite layer and connect to pad by using vias.
- Example of measurement for different connection types (by Analog Devices paper* data):

Connection	Measured voltage (mV)	Error (%)
Pseudo-Kelvin sensing	9.55	4.5
Analog Devices solution	9.90	1.0
Without Kelvin sensing	12.28	22.8

* Marcus O'Sullivan. Optimize High-Current Sensing Accuracy by Improving Pad Layout of Low-Value Shunt Resistors. Analog Dialogue. Volume 46. June 2012

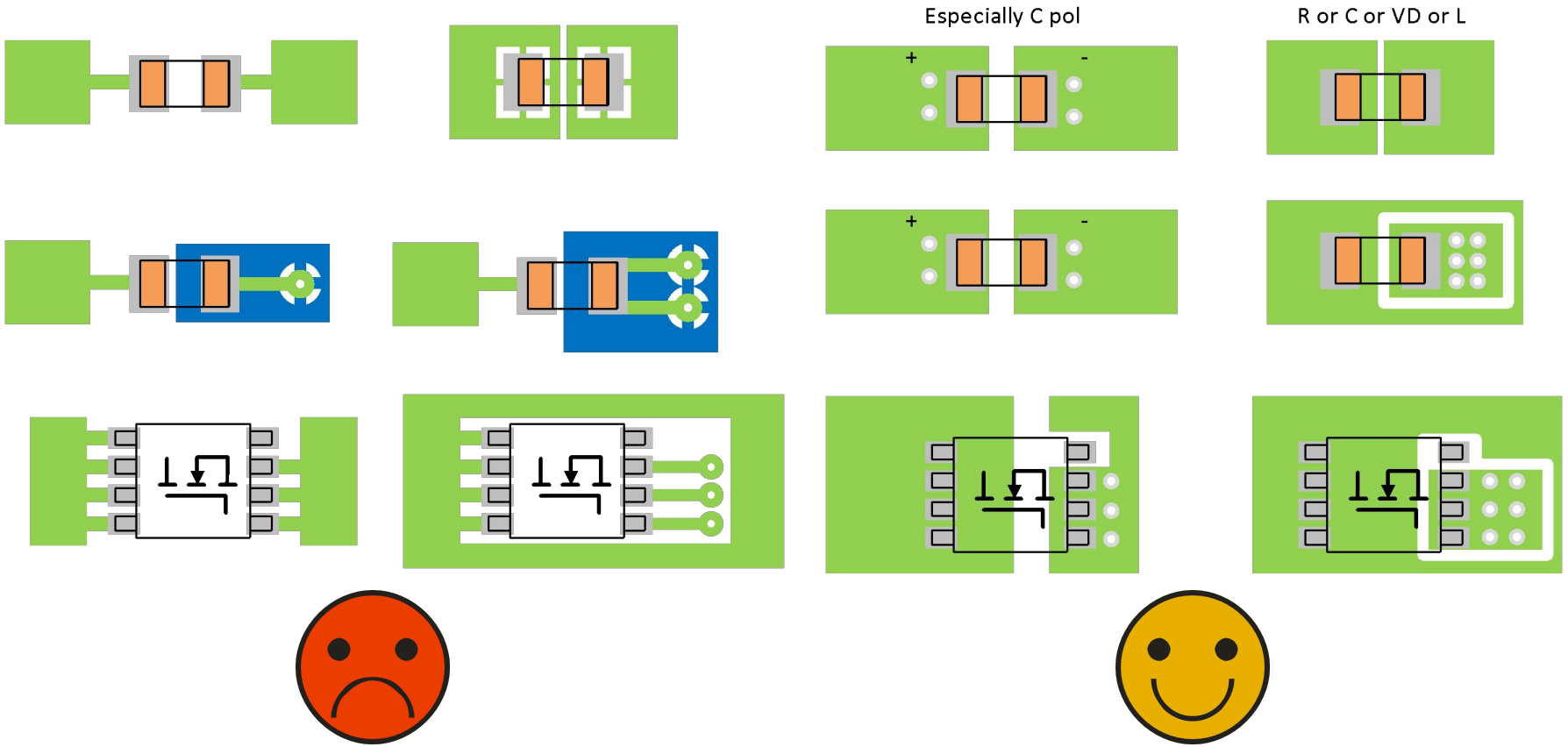
Land Patterns for SMD components in PE devices

- For minimization of ESL and ESR Pad configuration for SMD components must be:
  - Without thermal connection.
  - With vias as close as possible to pad.
  - With sufficient number of vias in case of changing layer near the pad.

- Notice:
  - SMD pad without thermal relief could cause soldering problem!

Land Patterns for SMD components in PE devices

- Examples of Pad configuration:



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Mixed-signal grounding

- Mixed-signal components:
  - External DAC and ADC, MCU with DAC/ADC on board.
- Ground in mixed-signal components – the main question:
  - Digital?
  - Analog?
  - Some pins – digital, another ones – analog?

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- Ground in mixed-signal components – the main question:
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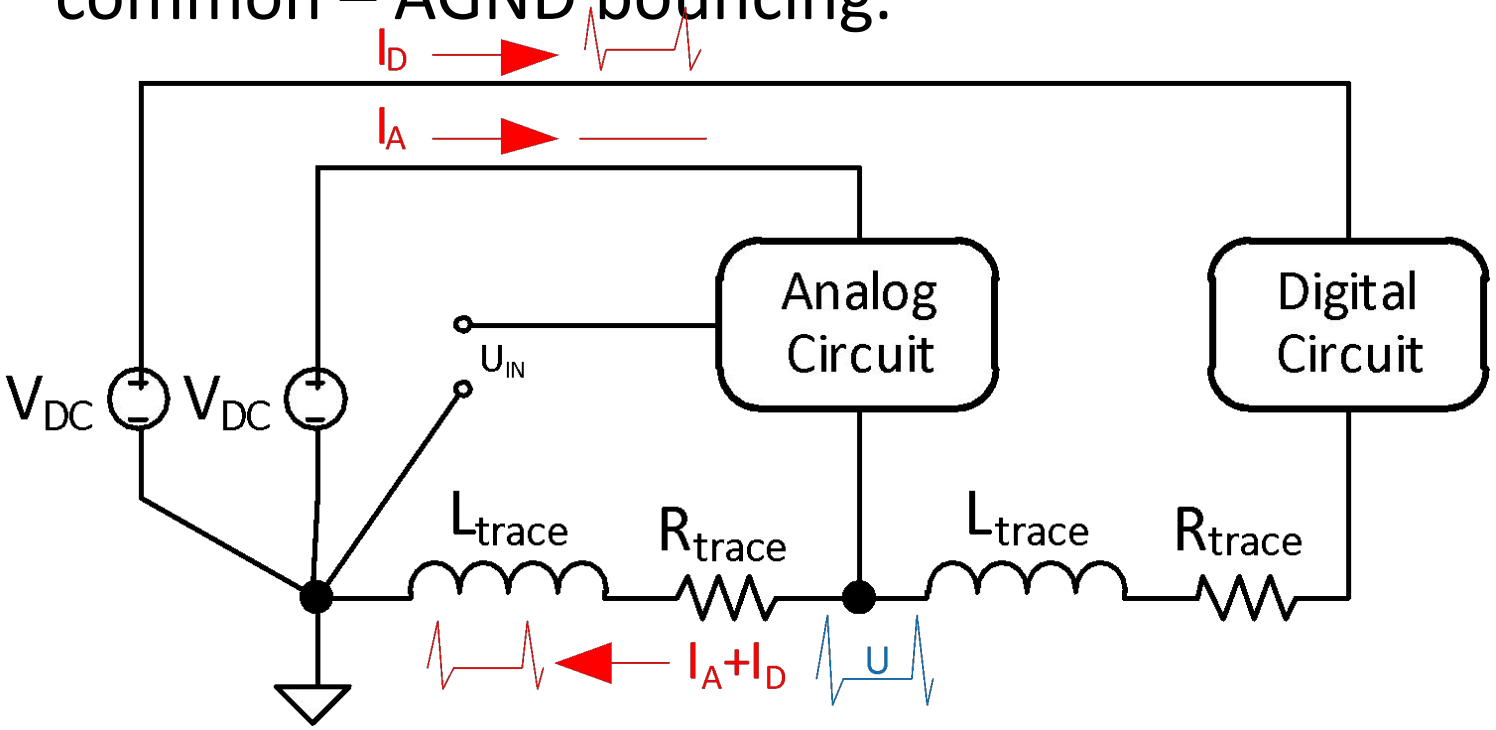
  - Some pins – digital, another ones – analog?

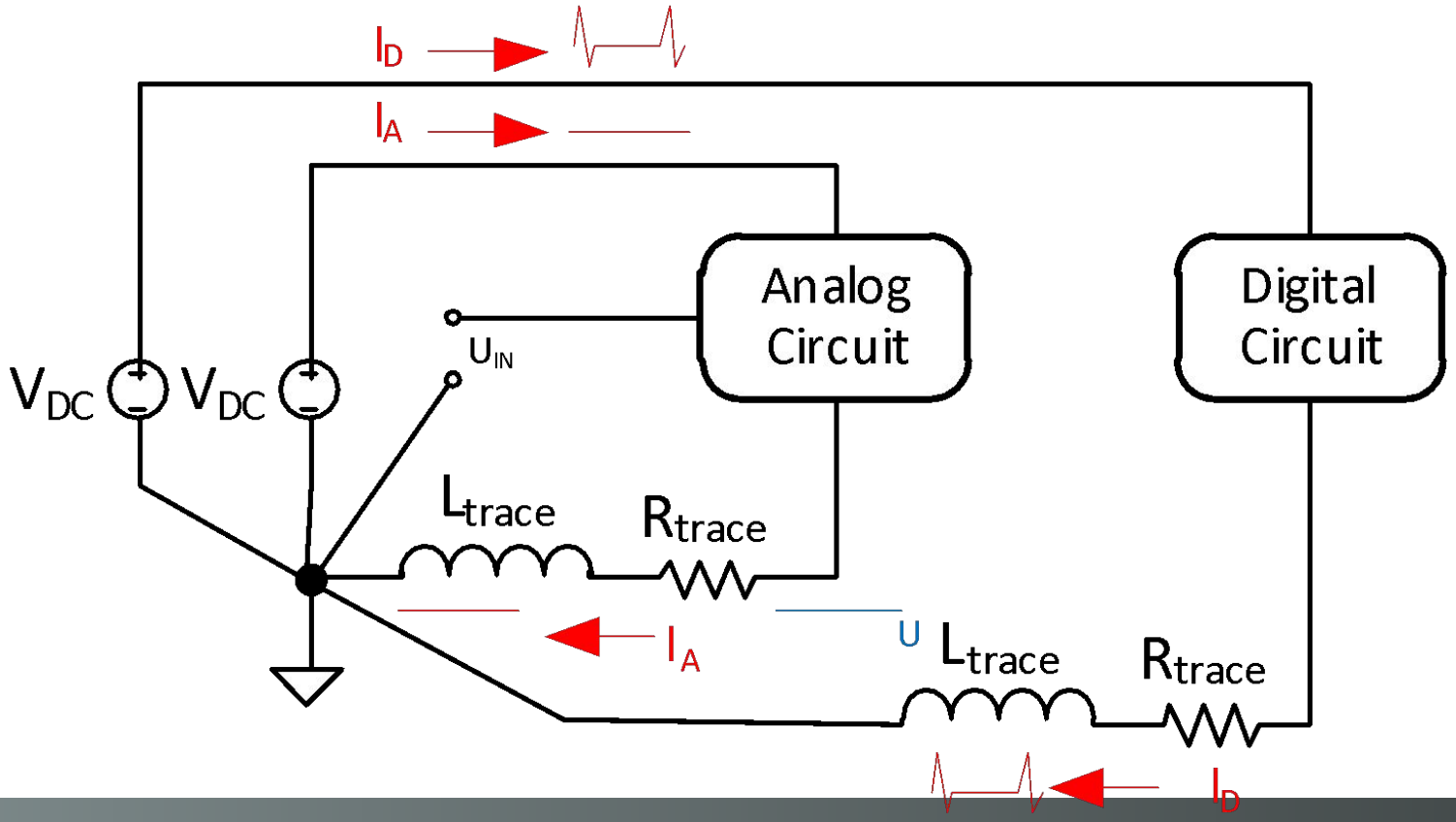
Digital and Analog Ground

- Bed design:
  - Digital (“dirty”) and analog (“clean”) ground are common – AGND bouncing.



Digital and Analog Ground

- Good design:
  - Digital and analog ground are separated.

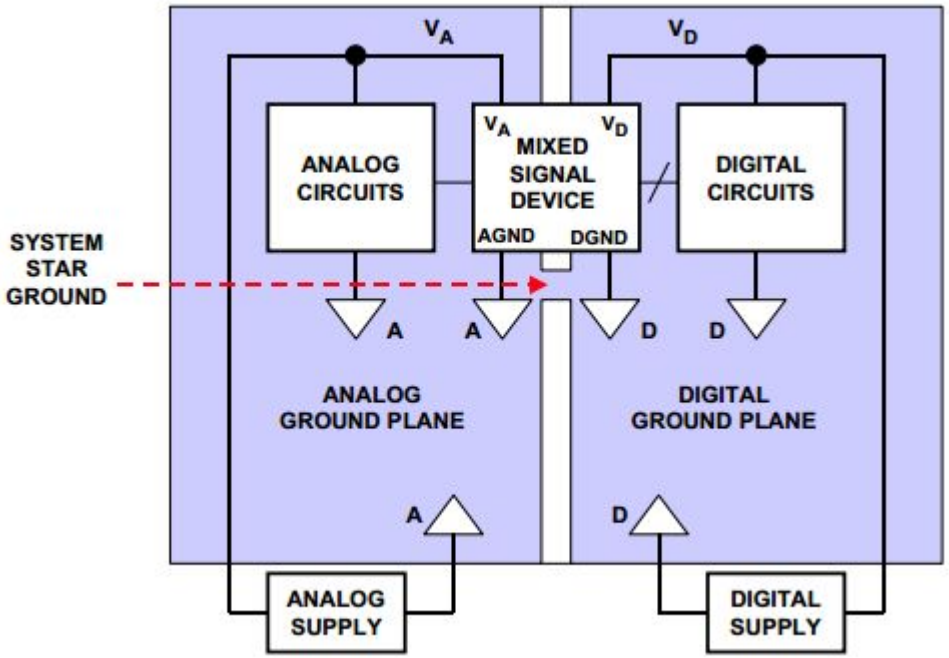


Digital and Analog Ground

- Planes for ground in control circuits of power electronic devices should improve EMC of control circuit.
- 4-layer PCB (sig - VCC– GND - sig) is a typical solution for the control board.
- VCC and GND planes provide additional distributed capacitance for control board power supply.

Mixed-signal grounding – single PCB

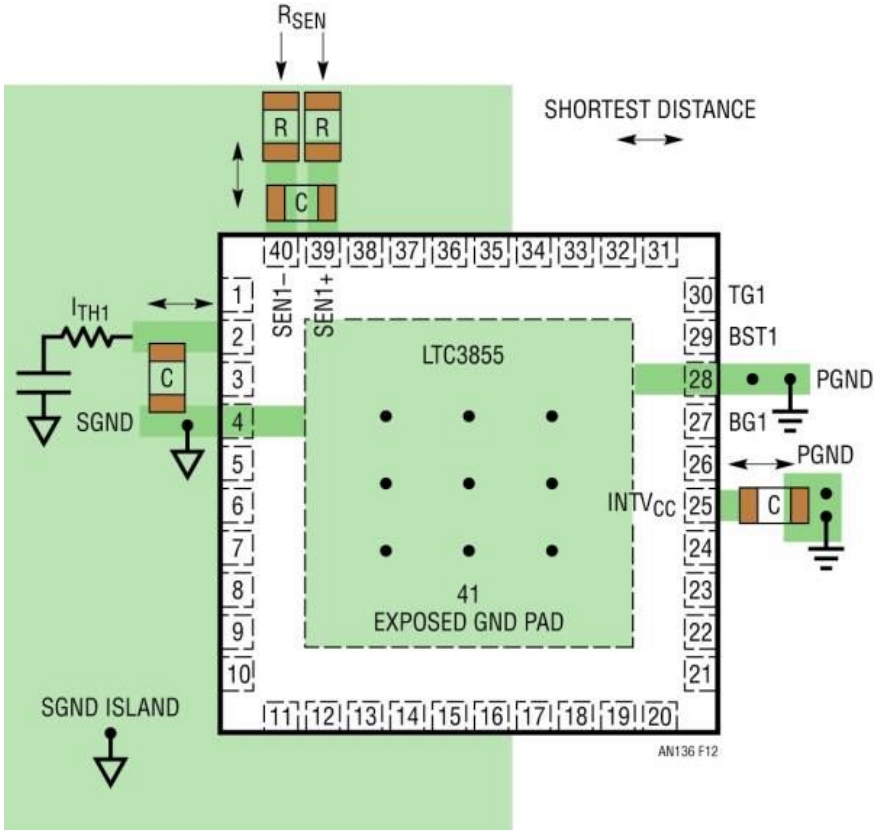
- “Star” grounding in the control part of single-board PE device – Analog Device advice.



http://www.analog.com/en/content/mixed_signal_dsp_design_book/fca.html

Mixed-signal grounding – single PCB

- “Star” grounding in the control part f single-board PE device – Linear Technology AppNote.



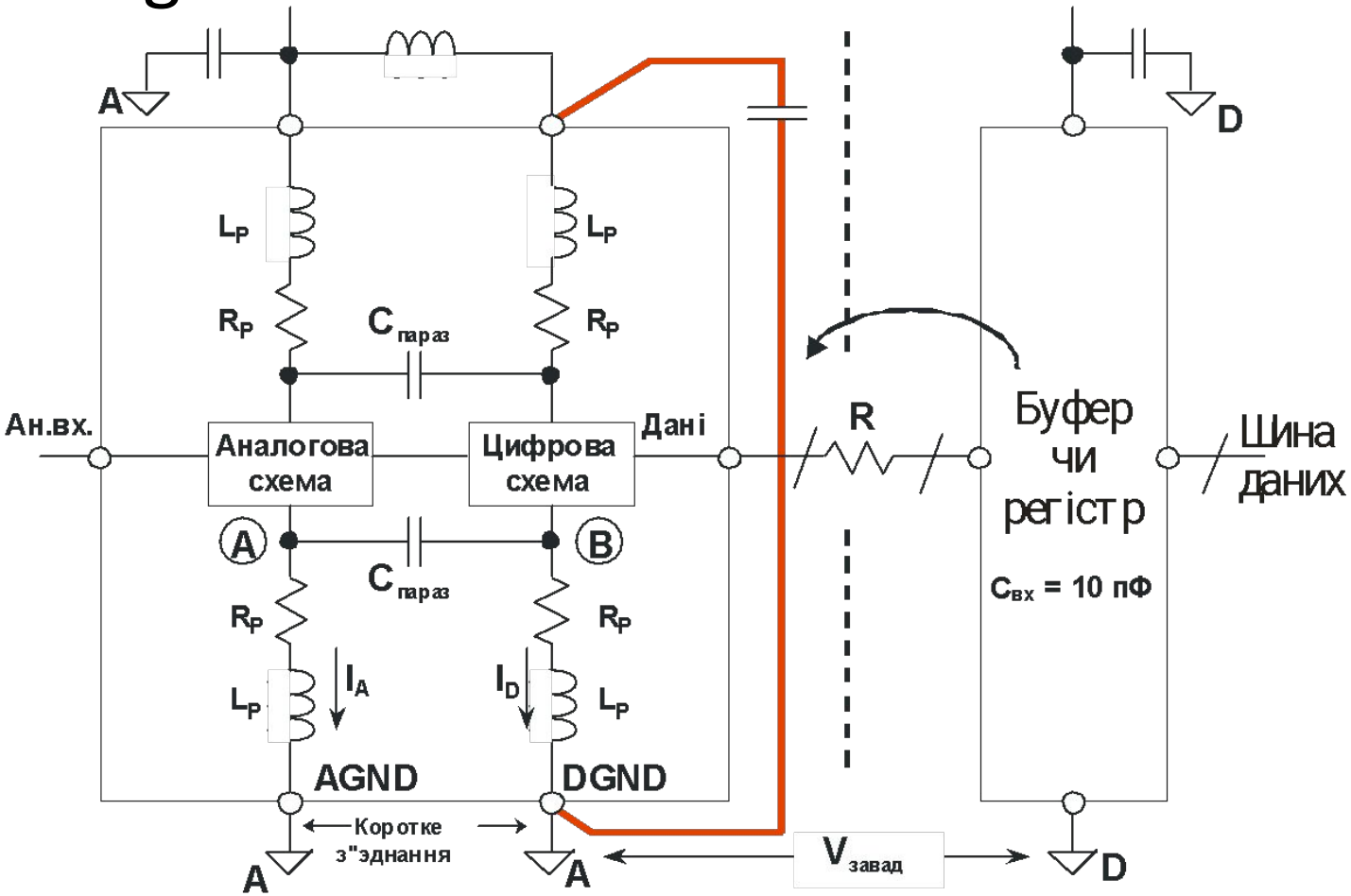
Mixed-signal grounding – multi-board PCB

- Grounding techniques for single-board PE devices are not optimum for multi-board devices.
- Multi-board grounding techniques are depend on
  - Low digital currents.
  - High digital currents.

- Provide additional ground pin in the connectors.
  - Recommend allocate 30-40% connector pins to GND.
  - Separate digital and analog signals by ground pins.

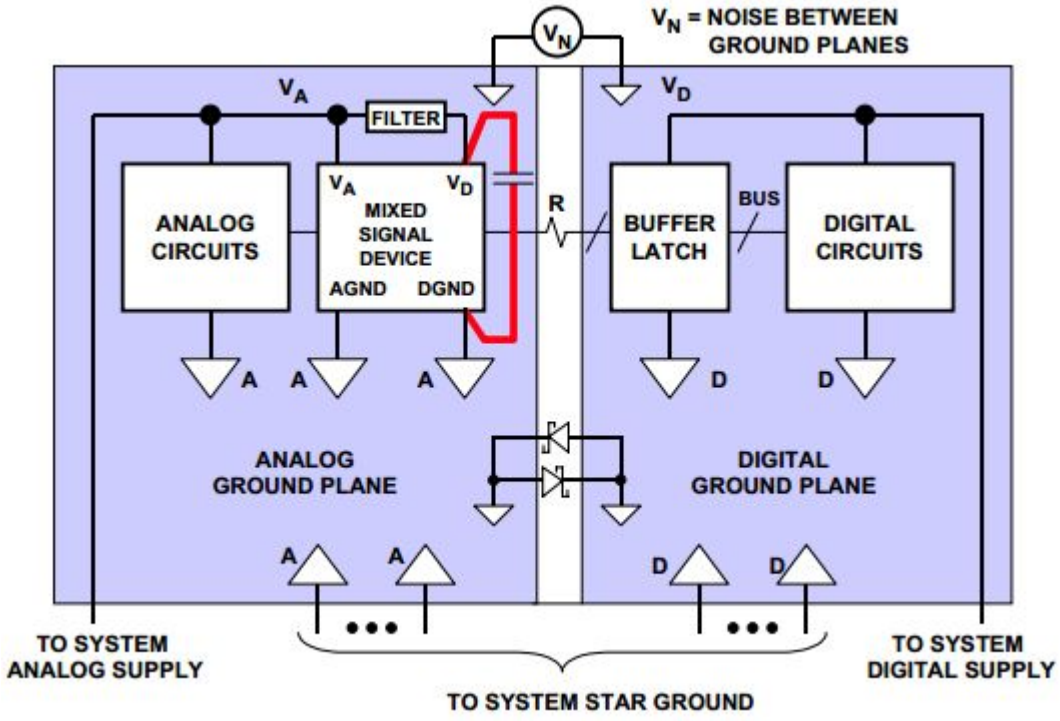
Mixed-signal grounding

- Small digital currents:



Mixed-signal grounding

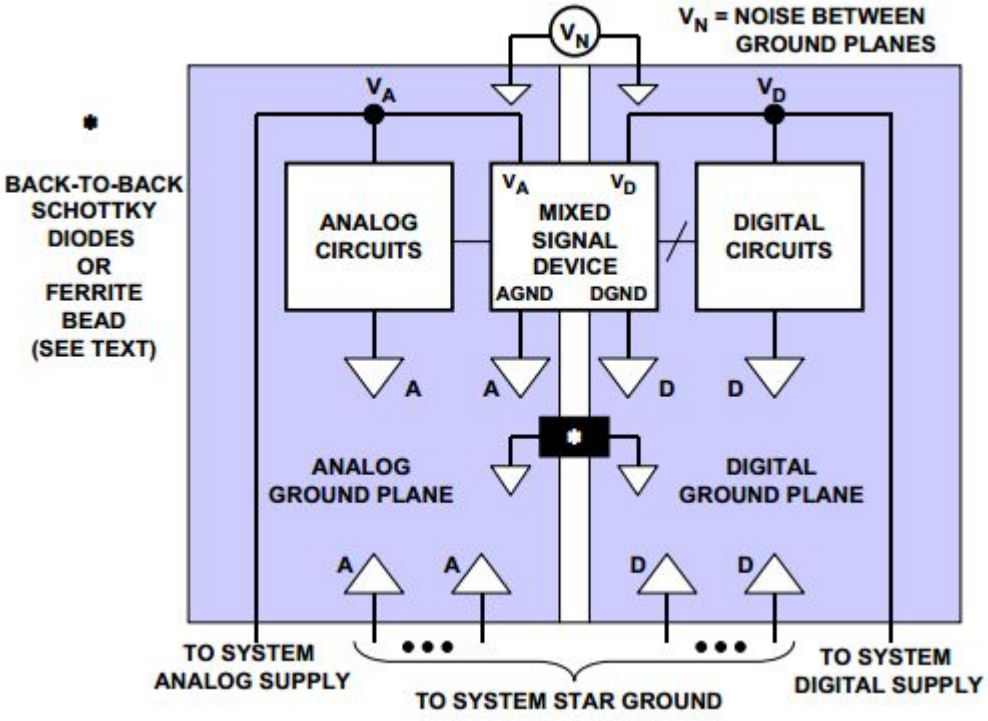
- Small digital currents:



http://www.analog.com/en/content/mixed_signal_dsp_design_book/fca.html

Mixed-signal grounding

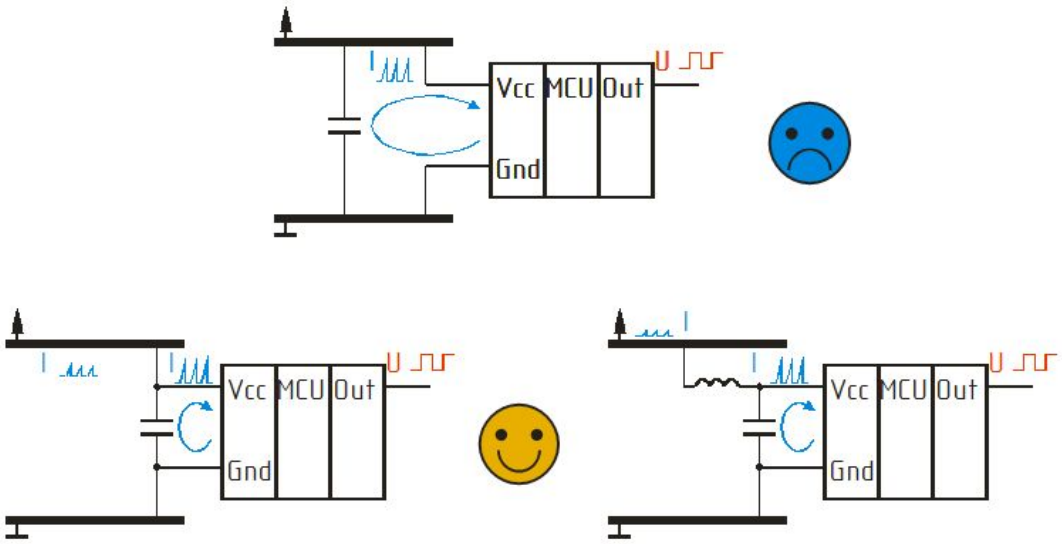
- High digital currents:



http://www.analog.com/en/content/mixed_signal_dsp_design_book/fca.html

Bypass Capacitors

- Noise on power line caused by switching digital components is shunted through the bypass capacitor, reducing the effect it has on the rest of the circuit.



Bypass Capacitors

- Bypass capacitor should be connected to the power pins of the digital components as close as possible!

Oscillator Layout Consideration

- Oscillator Circuit in common has the Highest operation frequency in whole design.